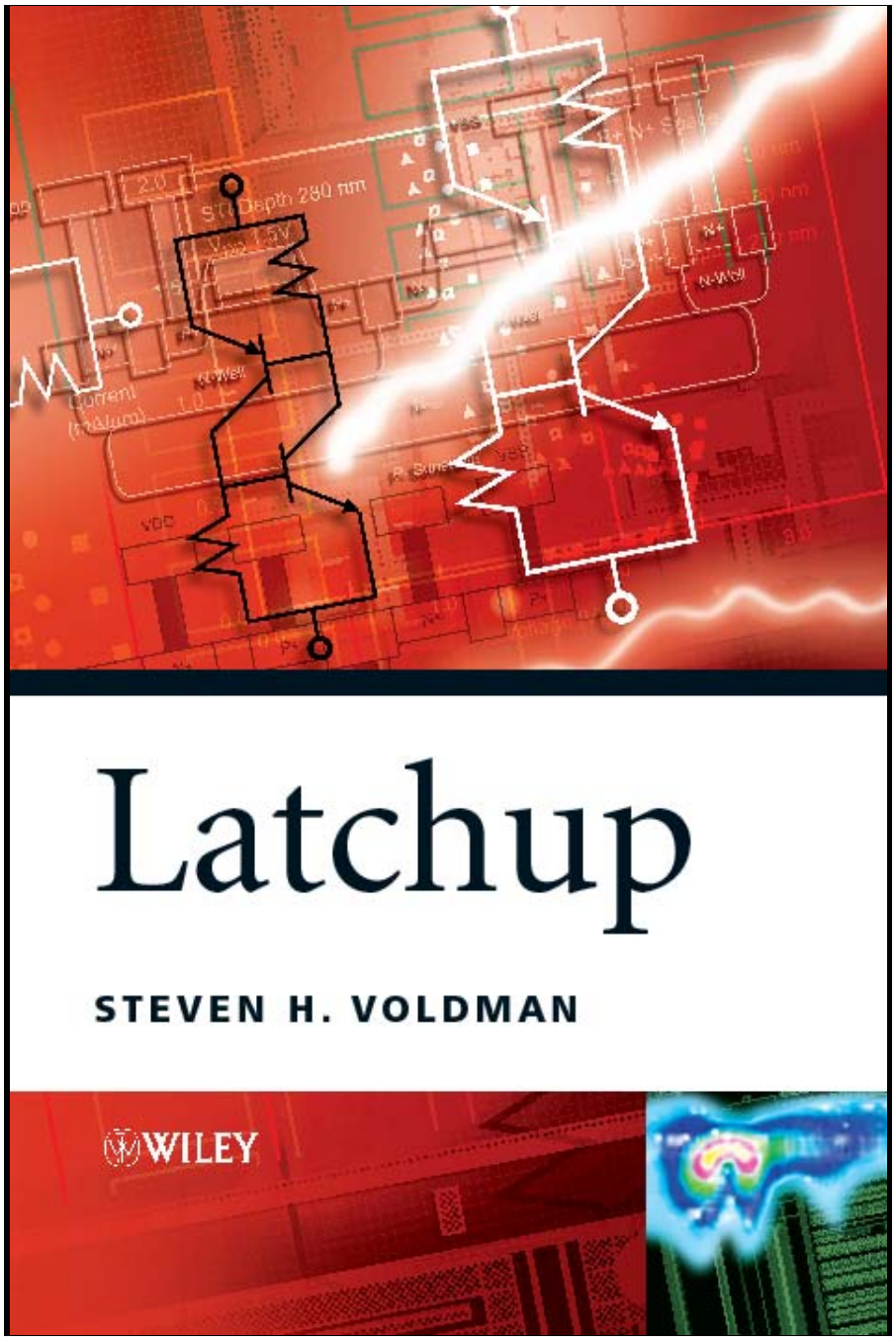
University of Central Florida

IEEE Electron Devices Colloqium
Feb 21-22nd 2008

Steven H. Voldman, **IEEE Fellow**

Latchup in Semiconductor Technology



It's Here !

Outline

- Latchup Basics
- CMOS Latchup Characterization
- Latchup Testing
- Latchup Computer Aided Design Concepts

CMOS Latch-up

- CMOS Concern increasing with Technology scaling and Integration
  - P+/N+ Scaling
  - STI Scaling
  - Substrate Concentration Scaling
  - Mixed Signal (RF, Analog, Digital)
  - System-on-Chip Integration
  - Non-native Power Supply Voltages

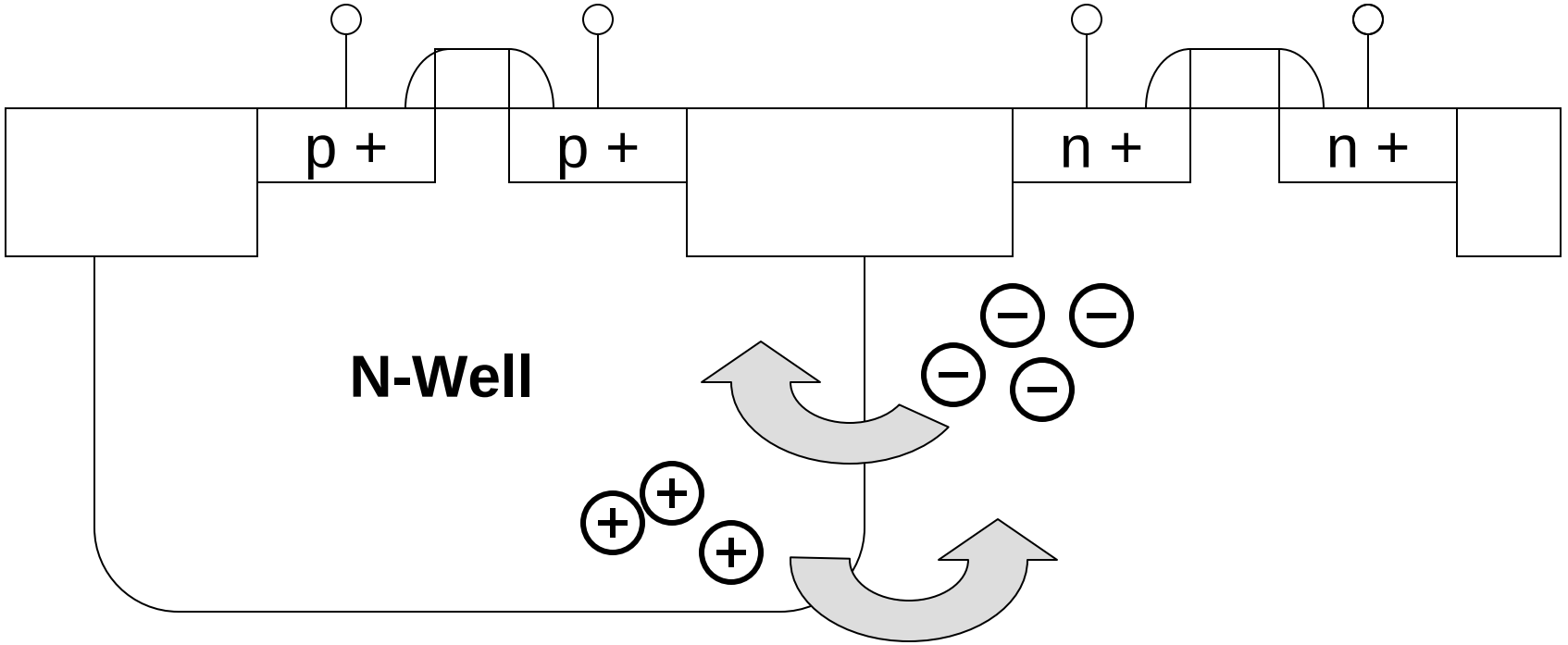
What is the fundamental problems today ?

- Testing
- Characterization
- Design Integration
- CAD Methods for Verification and Checking

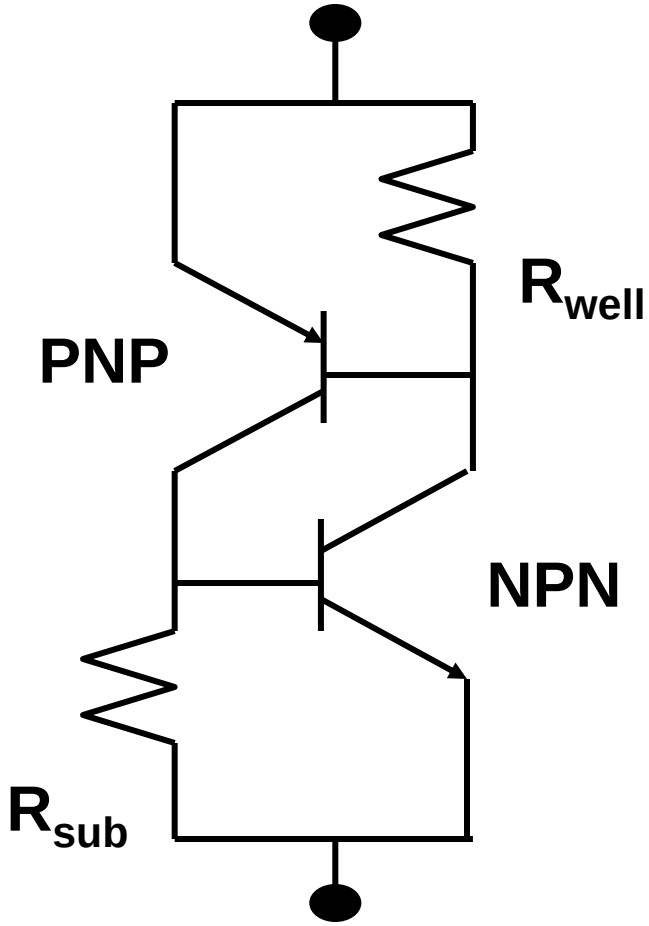
What is the CAD chip layout challenges ?

- Identifying parasitic PNPNs
- Identifying guard ring
- Evaluate sensitivity of latchup concern
- Design optimization
- Co-synthesis

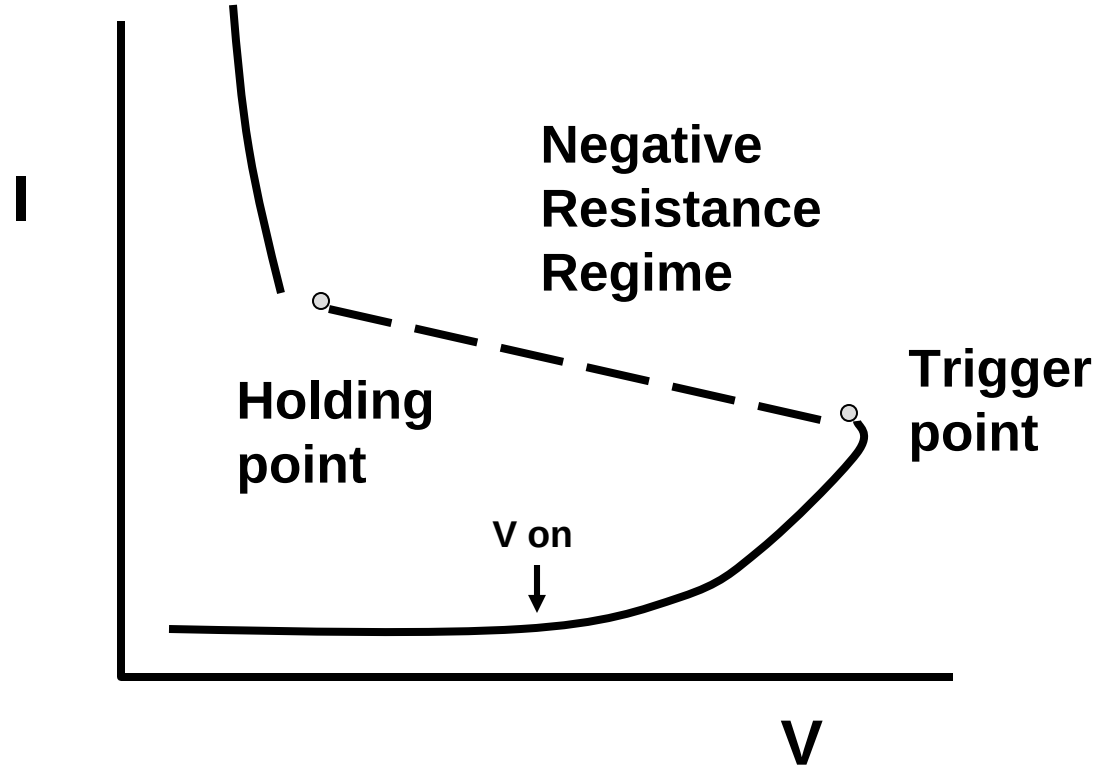
Latchup – How Does it Happen ?



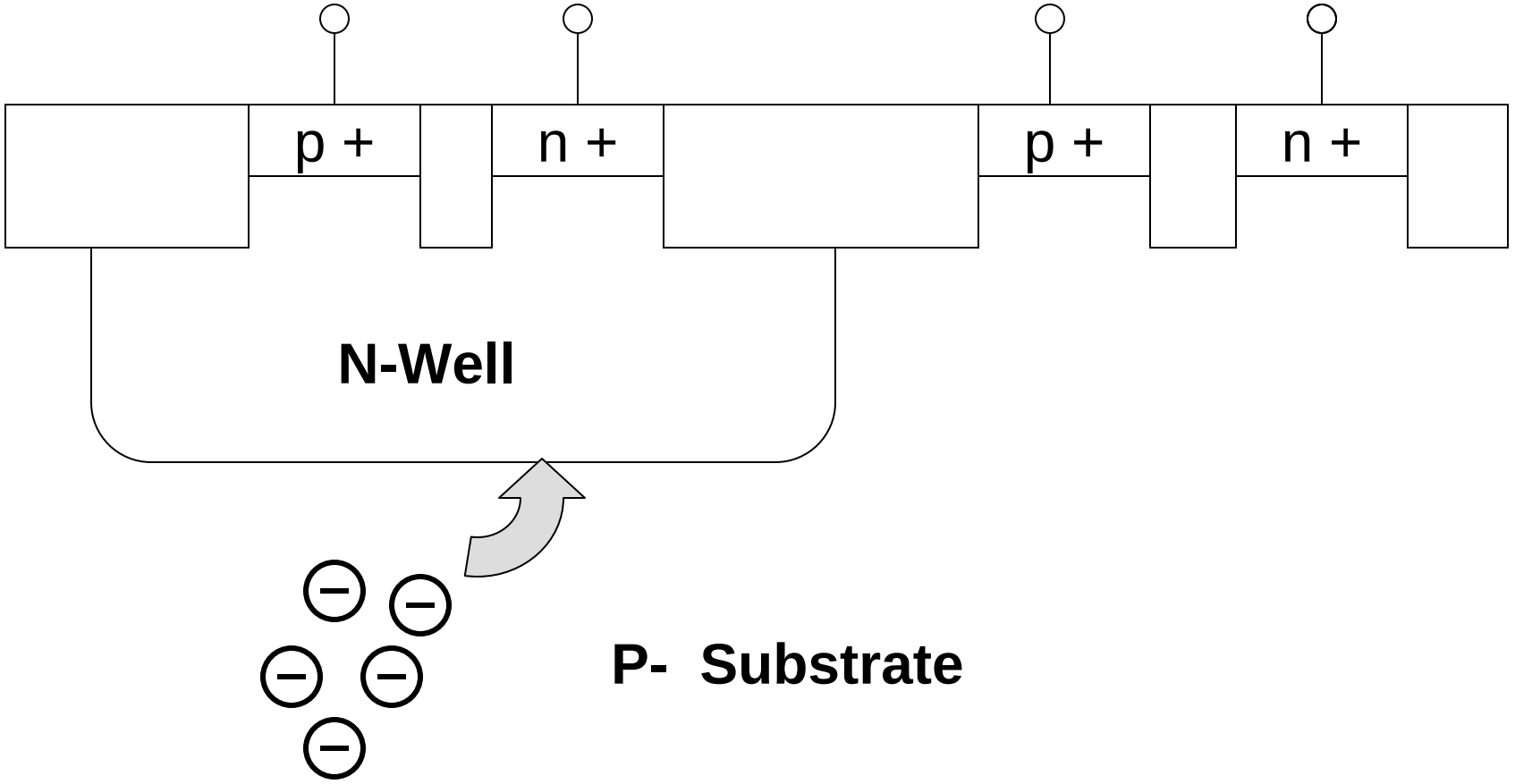
Latchup Network



Latchup I-V Characteristic

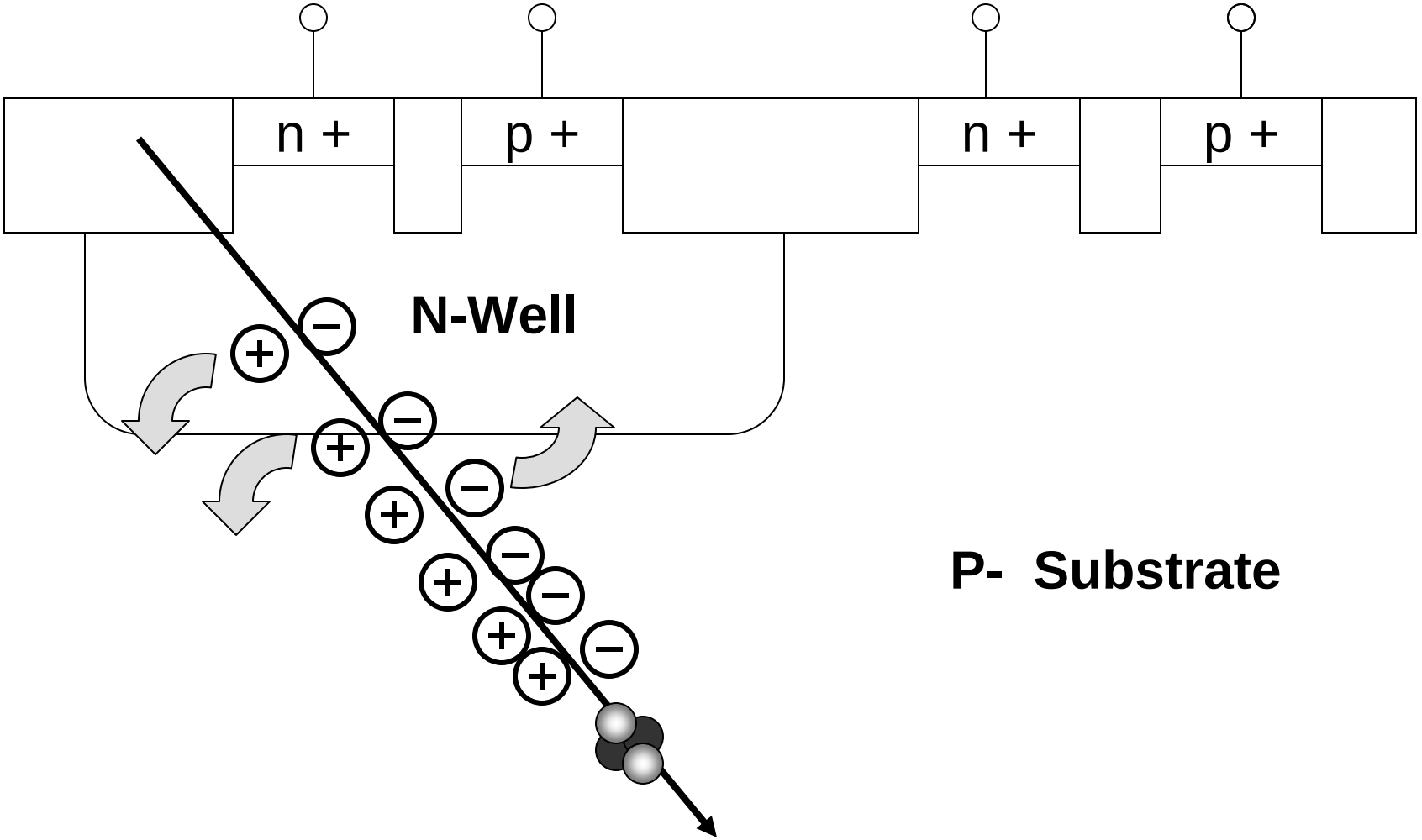


External Latchup - Substrate Injection



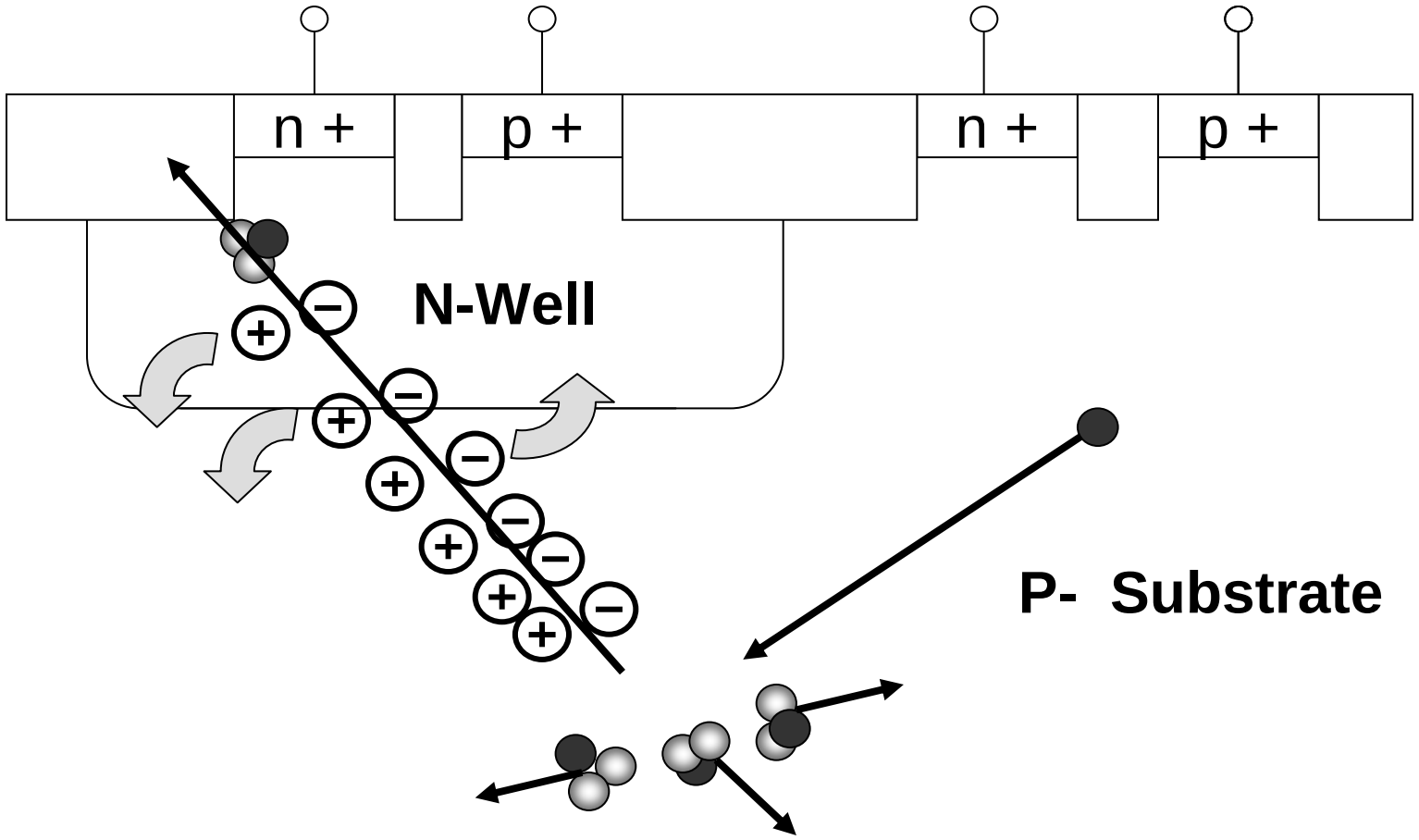
Voldman 2004

Alpha Particle Induced Latchup



Voldman 2005

Single Event Upset Induced Latchup

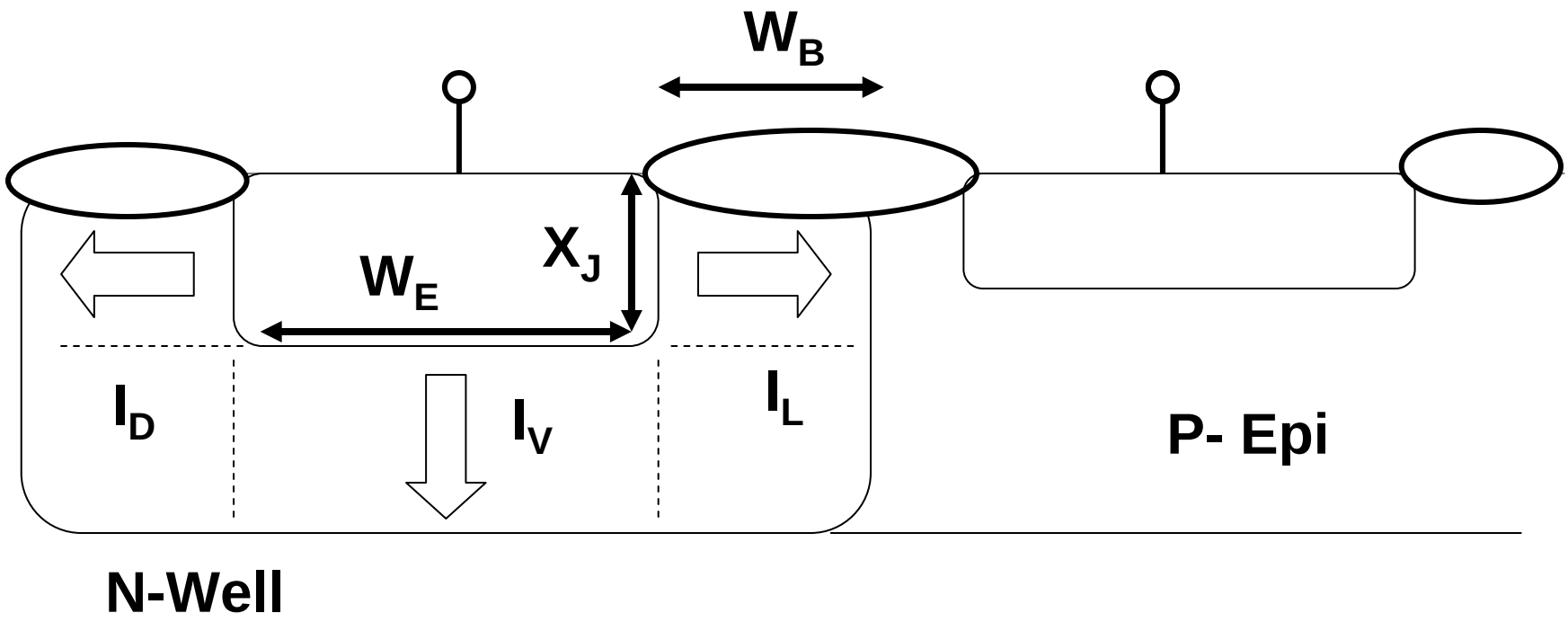


Voldman 2005

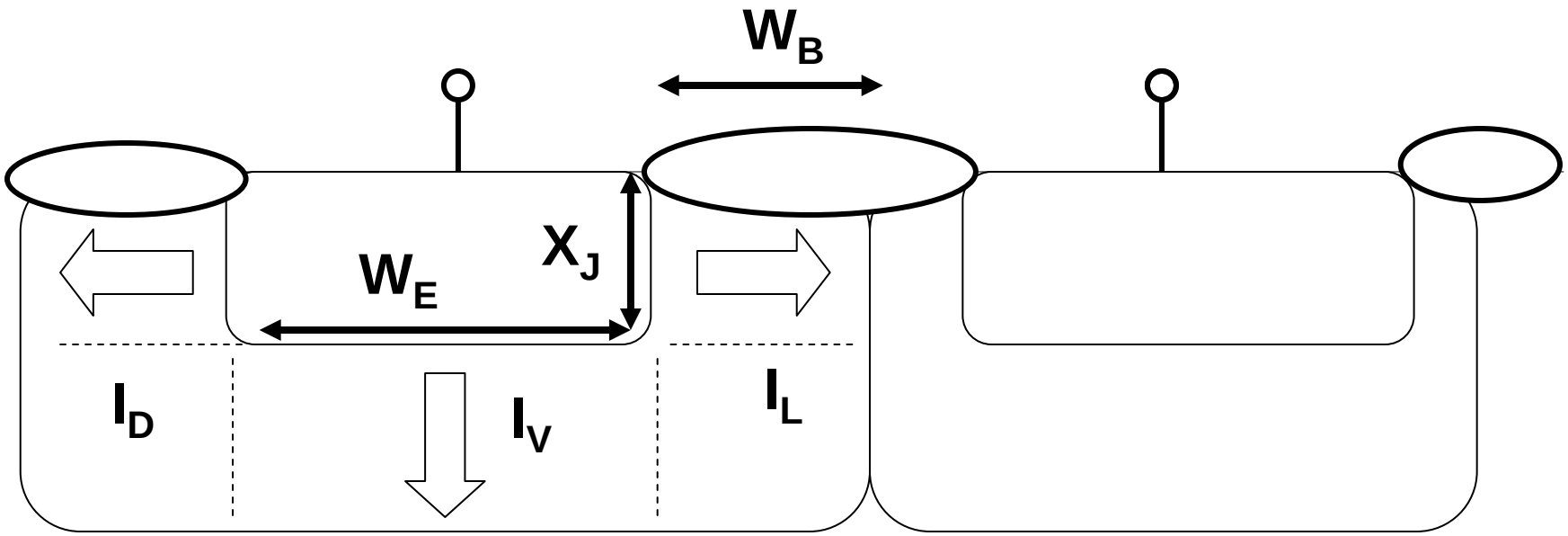
Lateral Bipolar Models

- Lindmayer-Schneider Model – Introduces lateral and vertical components
- Dutton/Whittier Step Junction – Introduces Vertical Step Junction N-/N++ or P-/P++
- D.B. Estreich Model - Lateral Electric field Model influences lateral and vertical transport

Lateral and Vertical Transistor



Lateral and Vertical Transistor

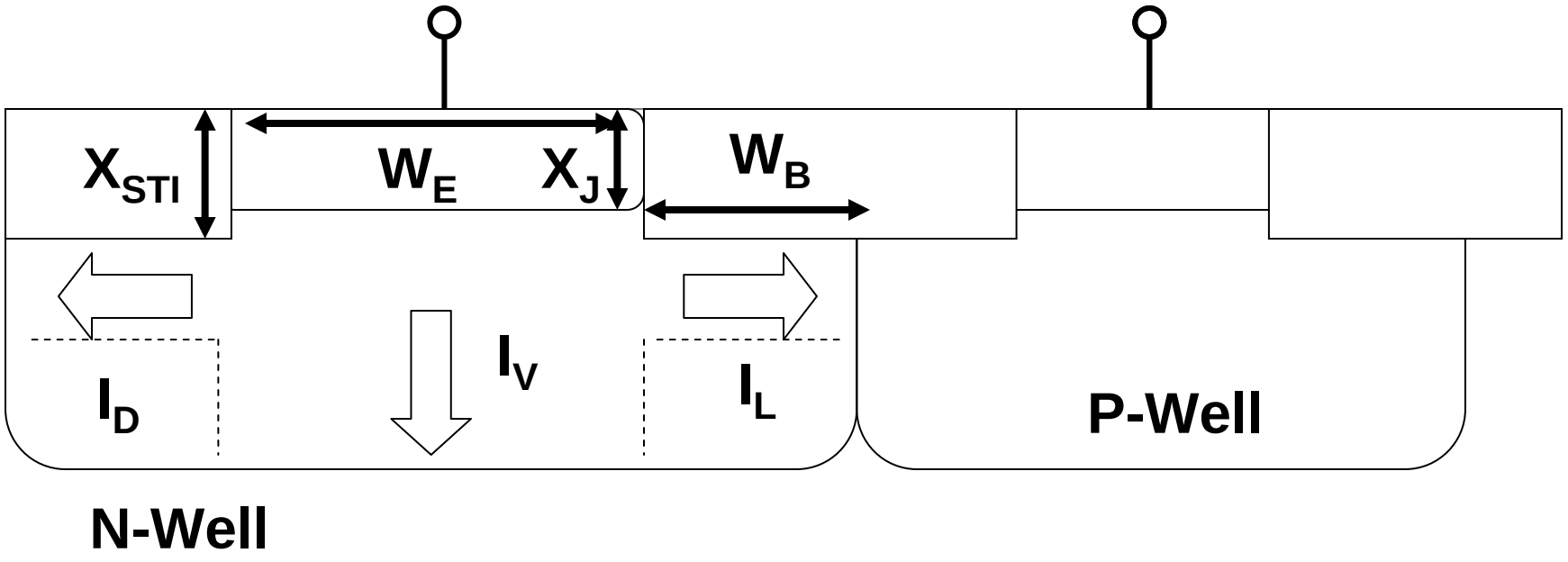


Model: Lindmayer and Schneider

- Lindmayer and Schneider representation assumes that vertical current does not contribute to the bipolar current gain

$$\beta = \frac{I_C}{I_B} = \frac{\alpha_l I_L}{(1-\alpha_l)I_L + I_D + I_V}$$

Lateral and Vertical Transistor with STI



Lateral Transistor: Non-field Assisted

- Early 1990's:

$$p'(x) = p_{no}\theta\left\{\exp(x/L_p) - \exp(W_B/L_p)\frac{\sinh(x/Lp)}{\cosh(x/Lp)}\right\} - p_{no}\left\{\frac{\sinh(x/Lp)}{\sinh(W_B/Lp)}\right\}$$

$$\theta = \exp(V/V_T) - 1$$

E-Field Assist Transport

- Lateral E field

$$\frac{d^2 p'(x)}{dx^2} - \frac{E}{V_T}\frac{dp'(x)}{dx} - \frac{1}{L_p^2}p'(x) = 0$$

$$p'(x) = Ae^{S_1 x} + Be^{S_2 x}$$

$$S_{1,2} = \frac{E}{2V_T} \pm \sqrt{\left(\frac{E}{2V_T}\right)^2 + \frac{1}{L_p^2}}$$

$$S_{1,2} = \lambda_1 \pm \lambda_2$$

Lateral Electric Field

- Carrier Distribution

$$p'(x) = p_{no}\left\{\theta - \frac{\exp(-\lambda_1 W_B) + \theta\exp(\lambda_2 W_B)}{2\sinh(\lambda_2 W_B)}\right\}\exp((\lambda_1+\lambda_2)x) +$$

$$+ p_{no}\left\{\frac{\exp(-\lambda_1 W_B) + \theta\exp(\lambda_2 W_B)}{2\sinh(\lambda_2 W_B)}\right\}\exp((\lambda_1-\lambda_2)x)$$

$$S_{1,2} = \lambda_1 \pm \lambda_2$$

$$S_{1,2} = \frac{E}{2V_T} \pm \sqrt{\left(\frac{E}{2V_T}\right)^2 + \frac{1}{L_p^2}}$$

Electric field Assisted α_l

- Lateral Current Gain with E-field Assist

$$\alpha_l = \frac{\lambda_2 \exp(W_B \lambda_1)}{\lambda_1 \sinh(W_B \lambda_2) + \lambda_2 \cosh(W_B \lambda_2)}$$

H-L and L-H Step Junctions

- Early latchup models pre-1980 did not address the influence of the p- / p+ substrate on the transport of the vertical transistor.
- Models developed by Gunn, Low, Dutton and Whittier addressed the “step junction” influence on the carrier transport in a p- / n- / n+ diode structure.
- D.B. Estreich included this effect into the CMOS latchup bipolar models.

Model: β with L-H Factor

- Lateral Bipolar Model with L-H Vertical Correction (Estreich)

$$\beta_{pnp} = \frac{\alpha_l I_L}{(1-\alpha_l) I_L + F_V I_V}$$

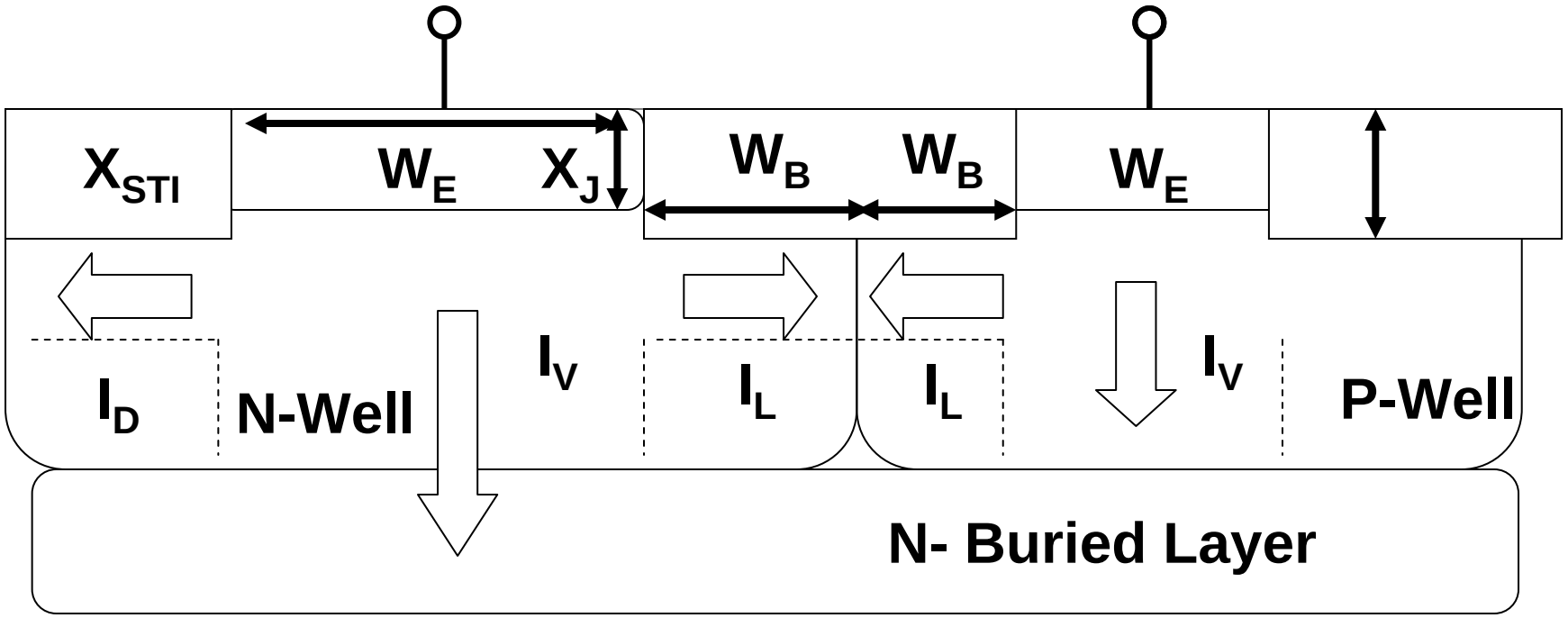
$$F_V = \frac{\sinh\gamma + \xi\cosh\gamma}{\cosh\gamma + \xi\sinh\gamma}$$

$$\xi = \frac{Dp_{sub}}{Dp_{epi}} \frac{L_{D_{epi}}}{L_{D_{sub}}} \frac{N_{D_{epi}}}{N_{D_{sub}}} \qquad \gamma = \frac{W_{epi}}{L_{D_{epi}}}$$

Triple Bipolar Model Issues

- Lateral and Vertical Components
- Buried Layer Extension
- Vertical Bipolar Transistor Step Junctions
- Separation of Currents

Triple Well


X_{STI}
W_E
X_J
W_B
W_B
W_E
I_D
N-Well
I_V
I_L
I_L
I_V
P-Well
N- Buried Layer
P- Substrate

LATCHUP

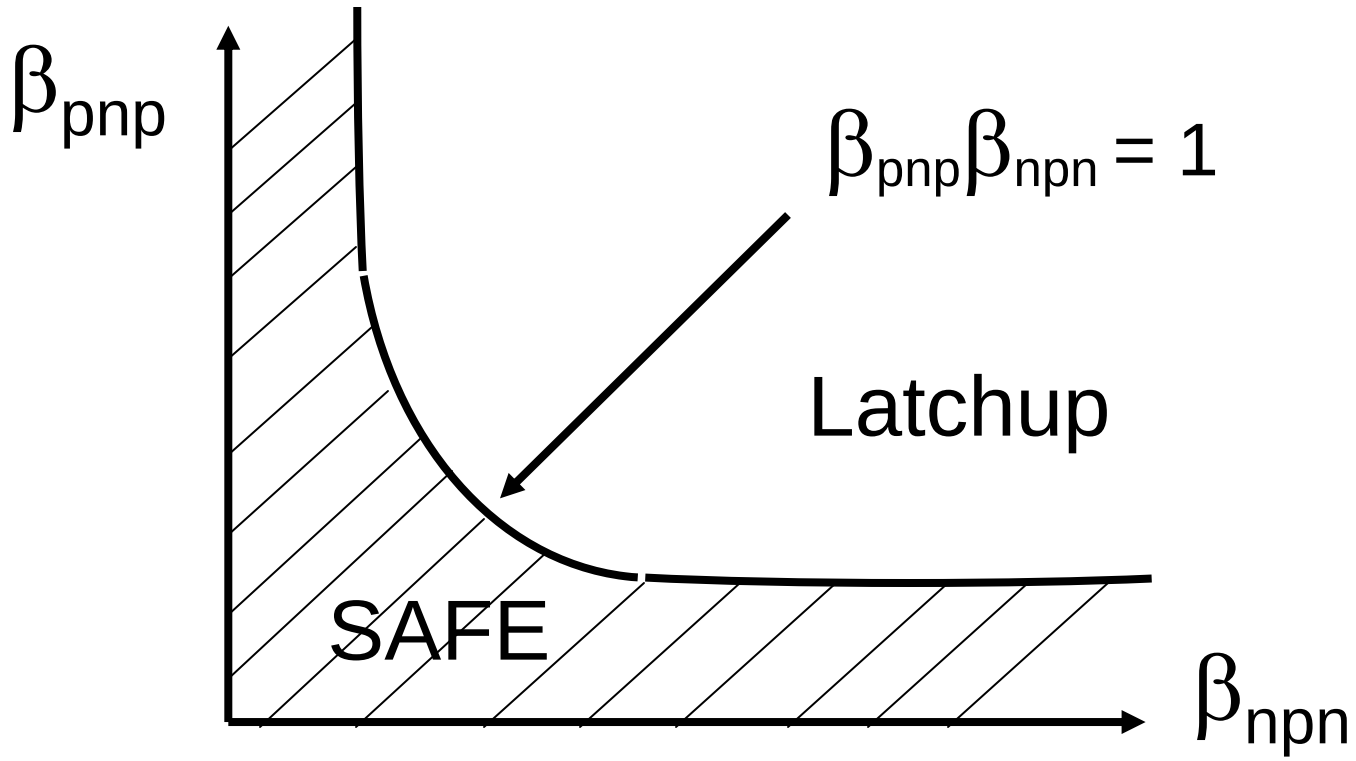
LATCHUP CRITERIA

Beta-Product Latchup Criterion

$$\beta_n \beta_p \geq \frac{I_{DD} + I_{RSX}\beta_n}{I_{DD} - I_{RSX} - I_{RNW}\left(\frac{\beta_n + 1}{\beta_n}\right)}$$

$$I_{RSX} = \frac{(Vbe)_n}{(R_{sx})} \qquad I_{RNW} = \frac{(Vbe)_p}{(R_{nw})}$$

Beta Product Space



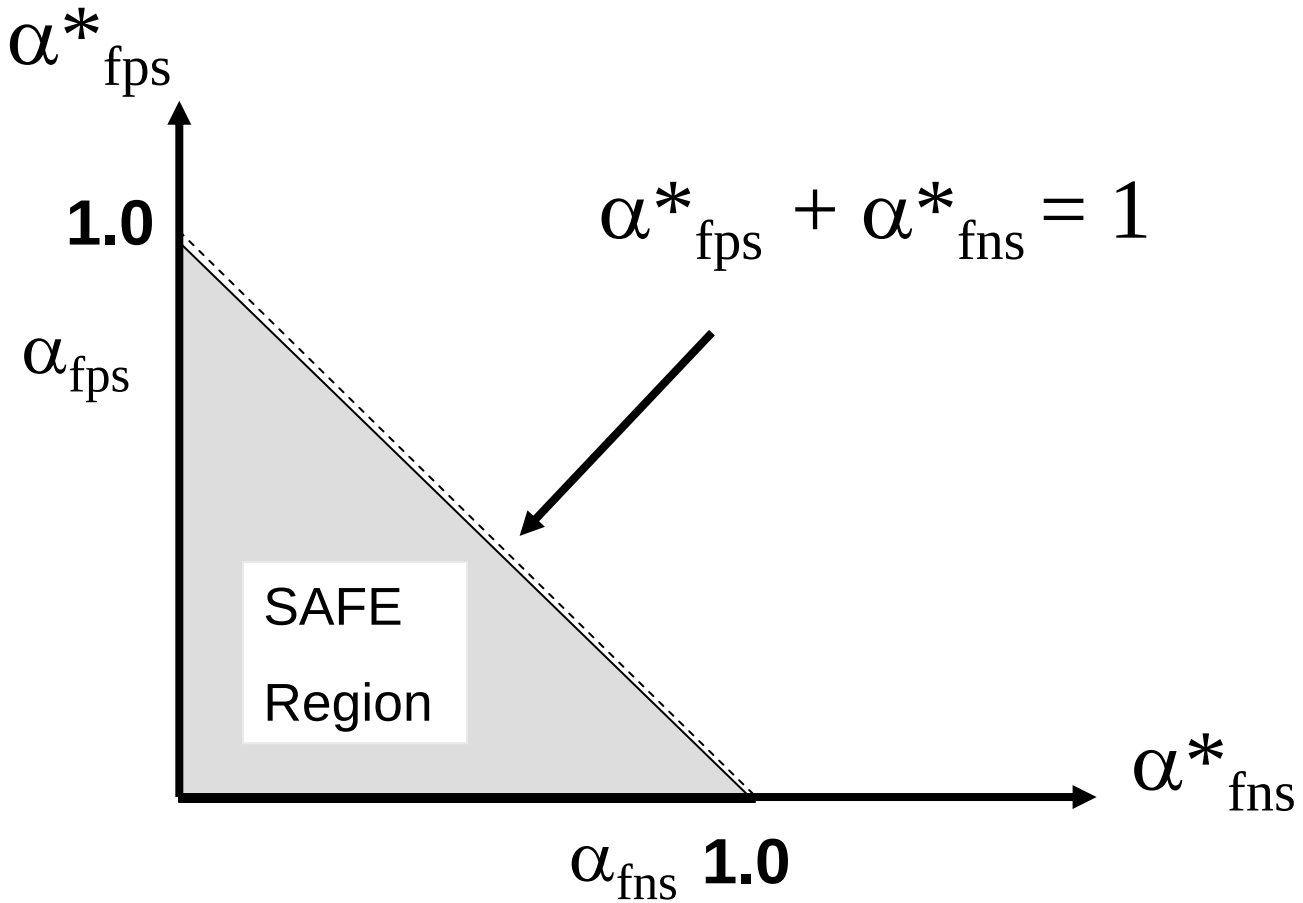
Differential Latchup Criterion

General Tetrode Condition – Alpha Sum Form

$$\alpha^*_{fns} + \alpha^*_{fps} \geq 1$$

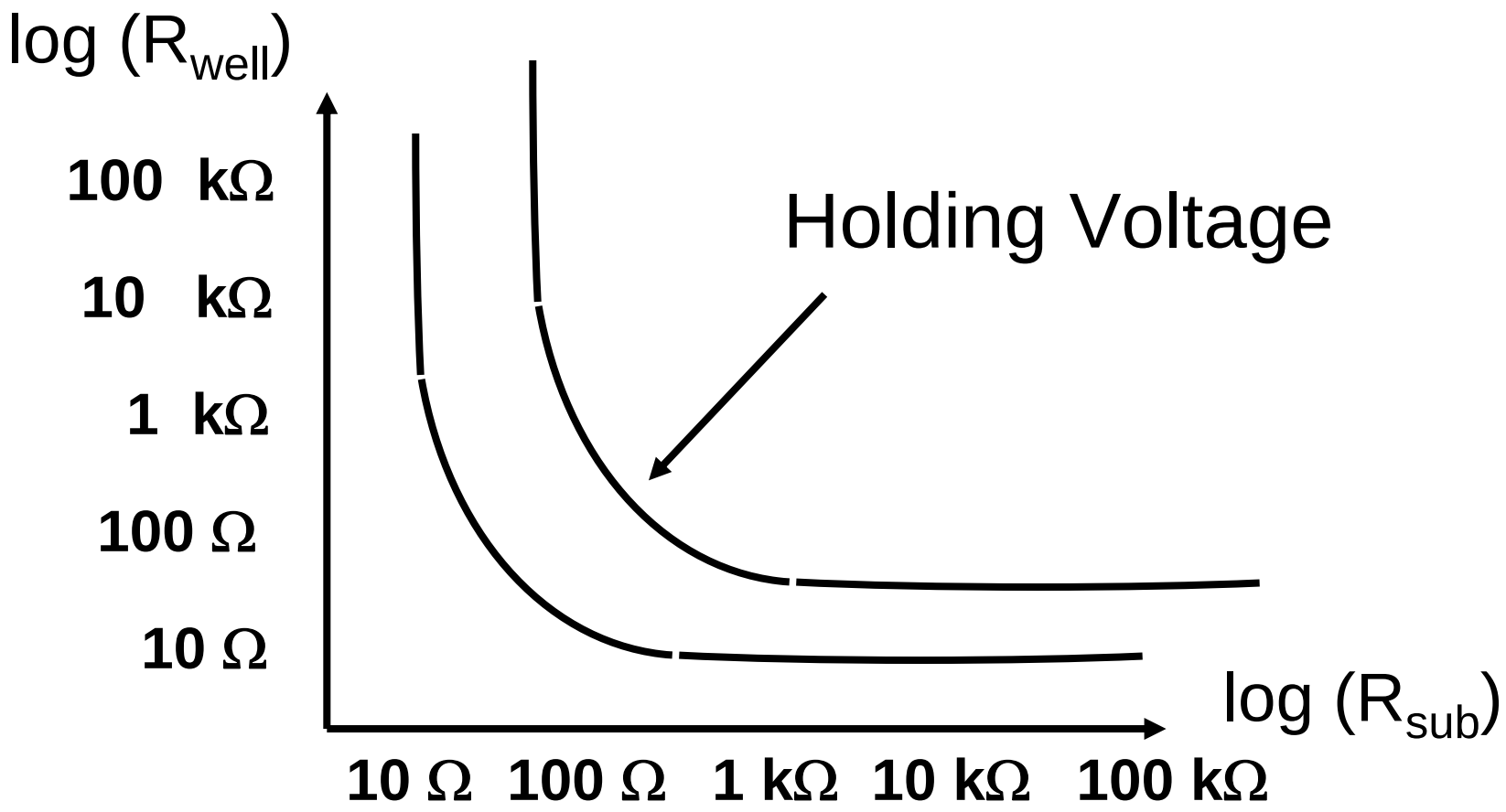
$$\alpha^*_{fns} = \frac{\alpha_{fns}}{1 + \frac{r_{en}}{R_S}} \qquad \alpha^*_{fps} = \frac{\alpha_{fps}}{1 + \frac{r_{ep}}{R_W}}$$

SAFE Region



Troutman 1984

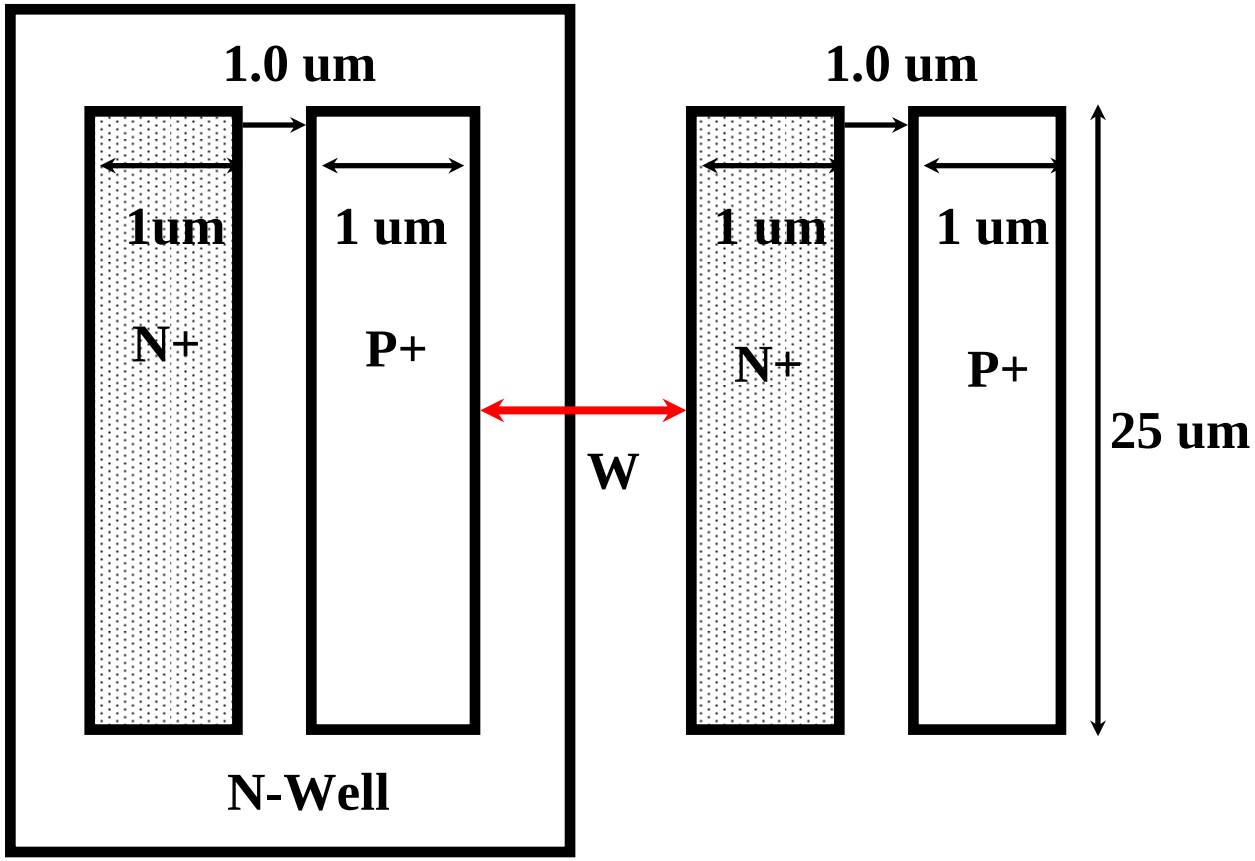
$R_{nw}R_{sx}$ Resistance Space



LATCHUP

CHARACTERIZATION

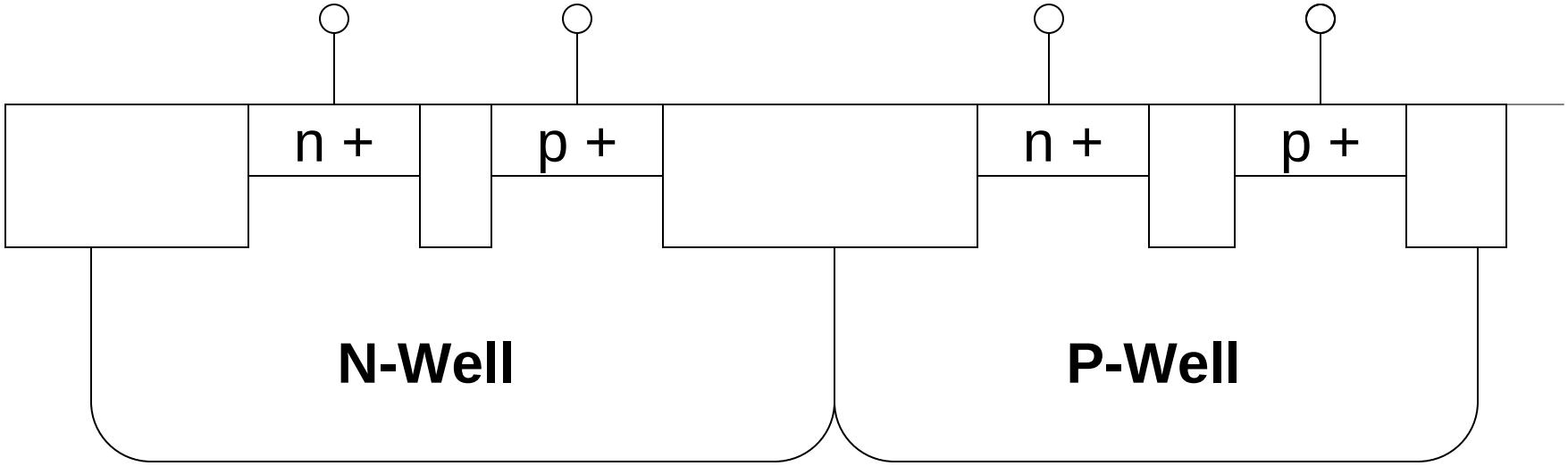
Latchup Test Structures: PNPN



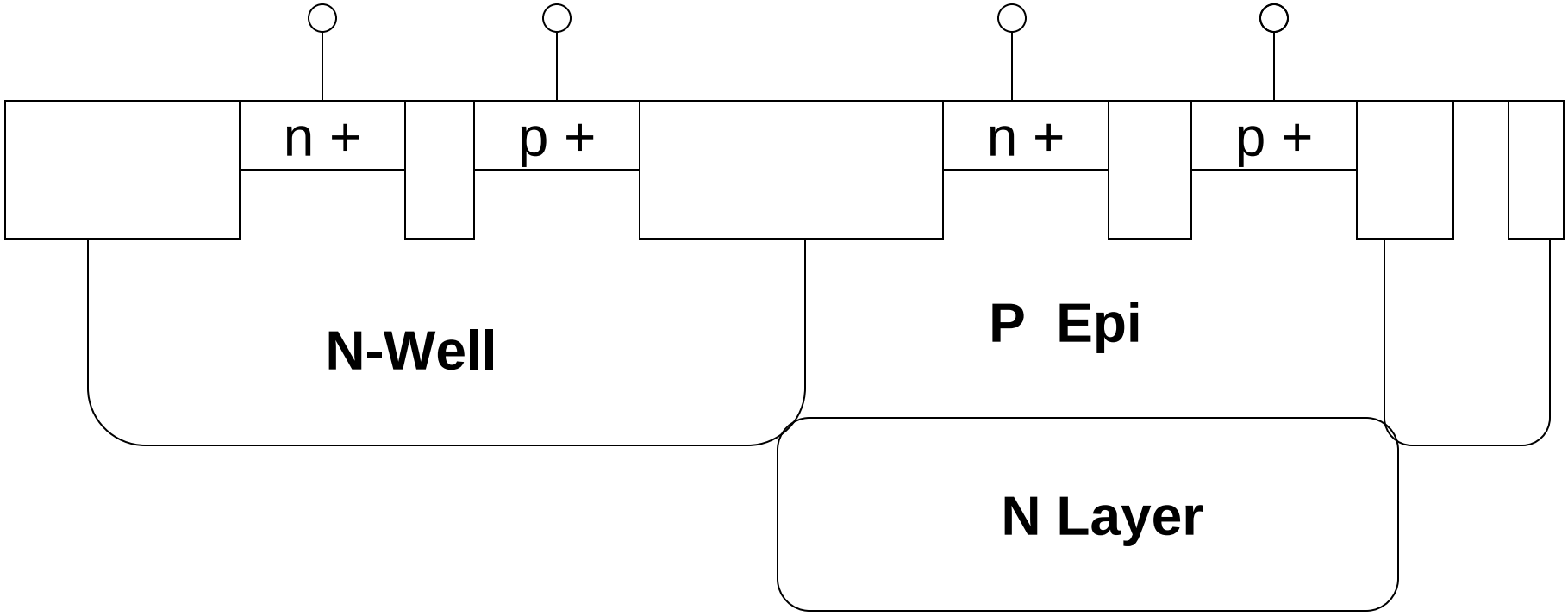
Troutman 1982

Latchup 2007

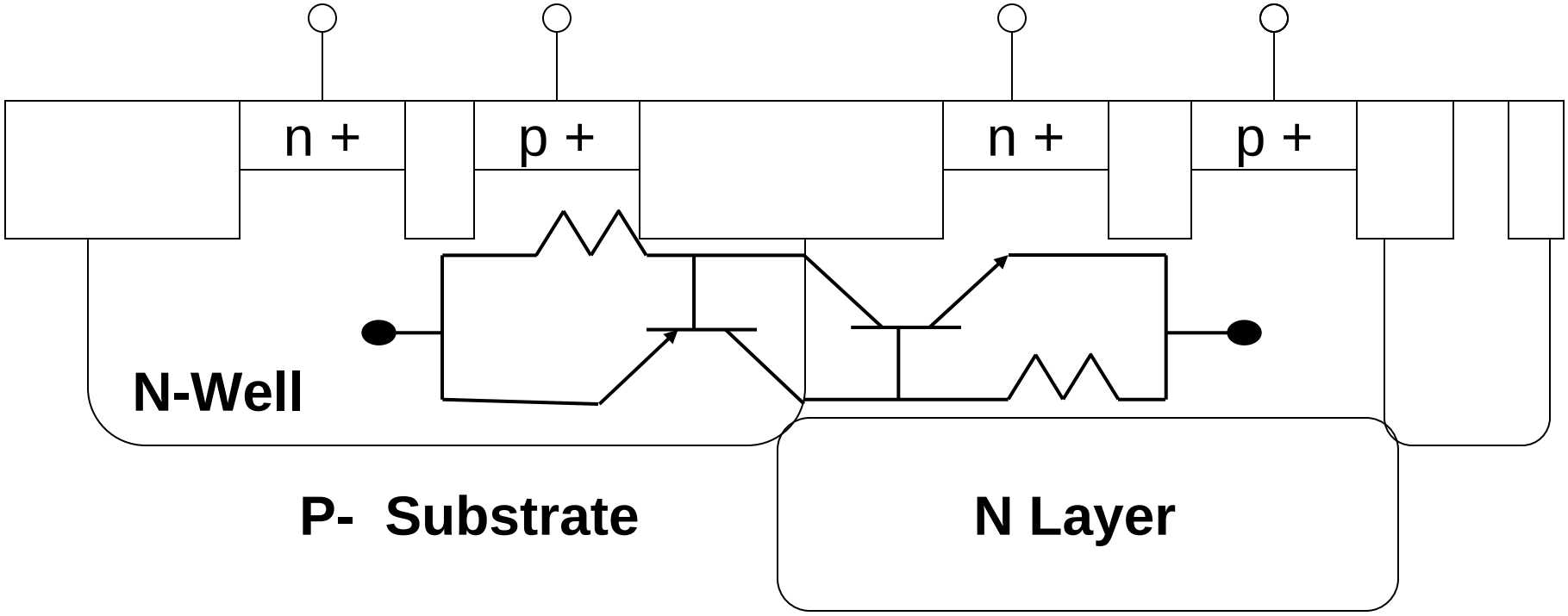
Dual Well Latchup Structures



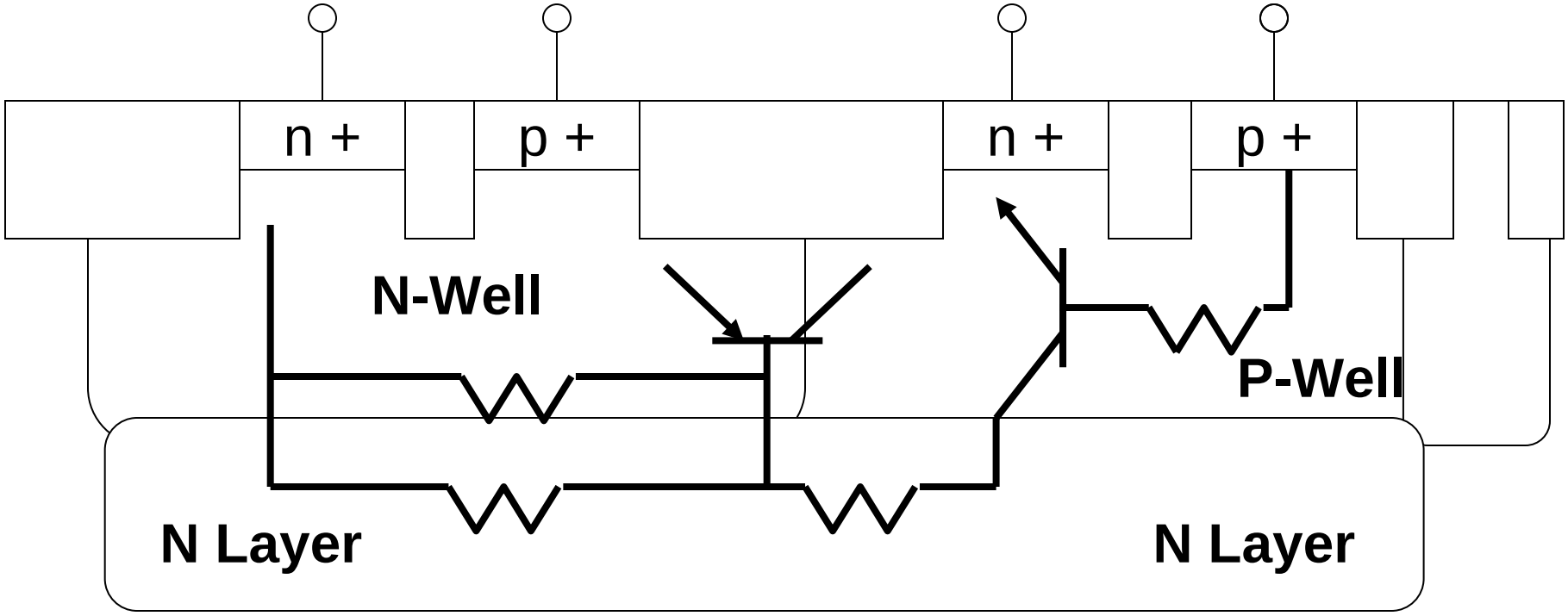
Merged Triple Well Latchup Structures



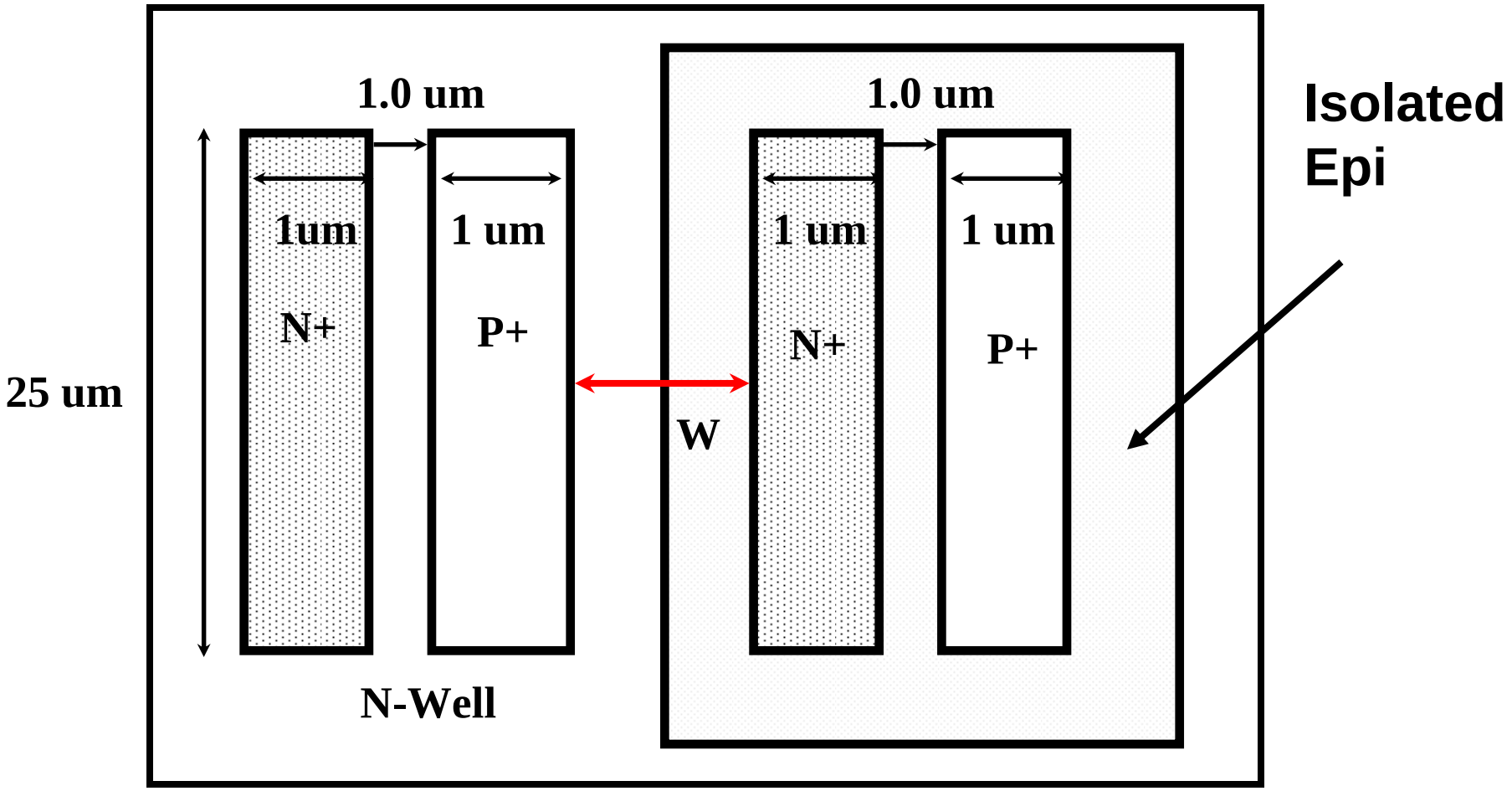
Merged Triple Well Latchup Structures



Merged Triple Well – Vertical NPN



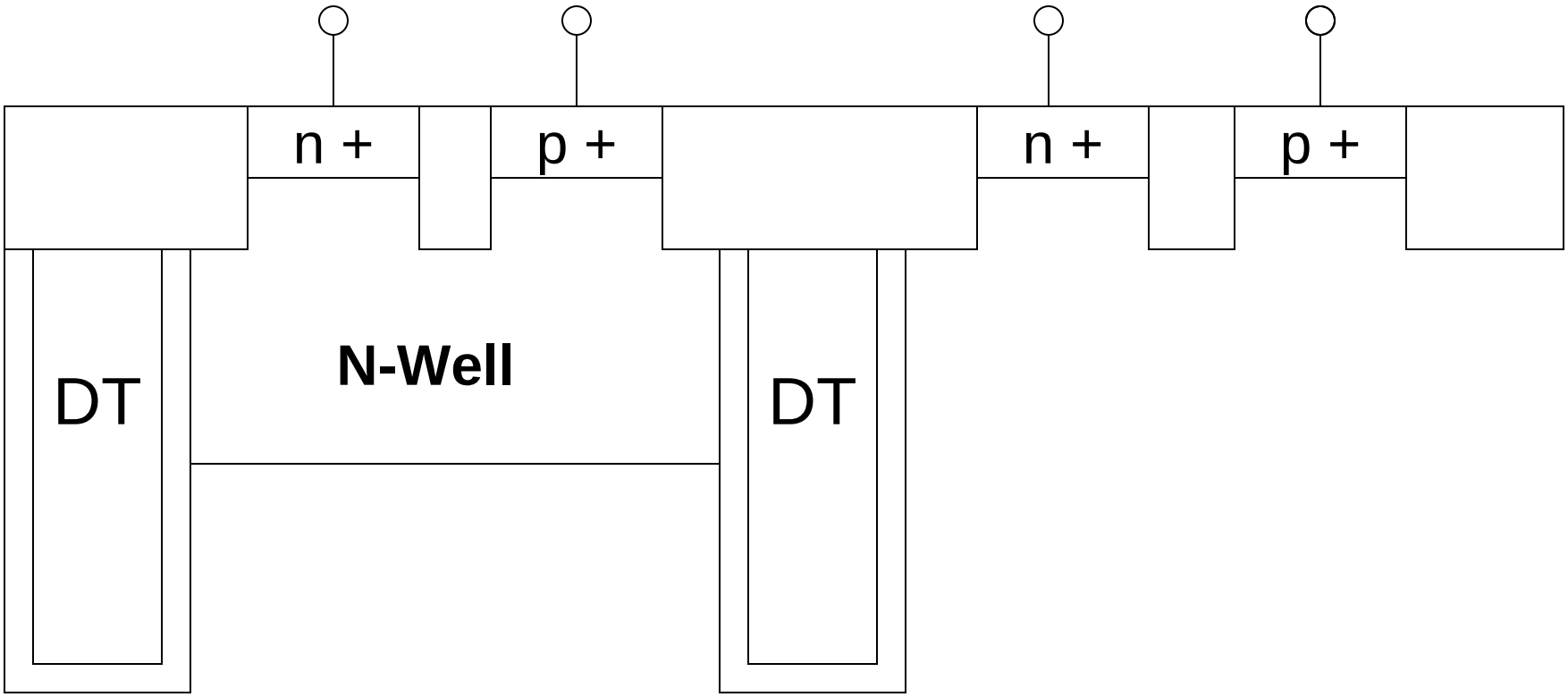
Latchup Test Structures: Triple Well



Voldman 2003

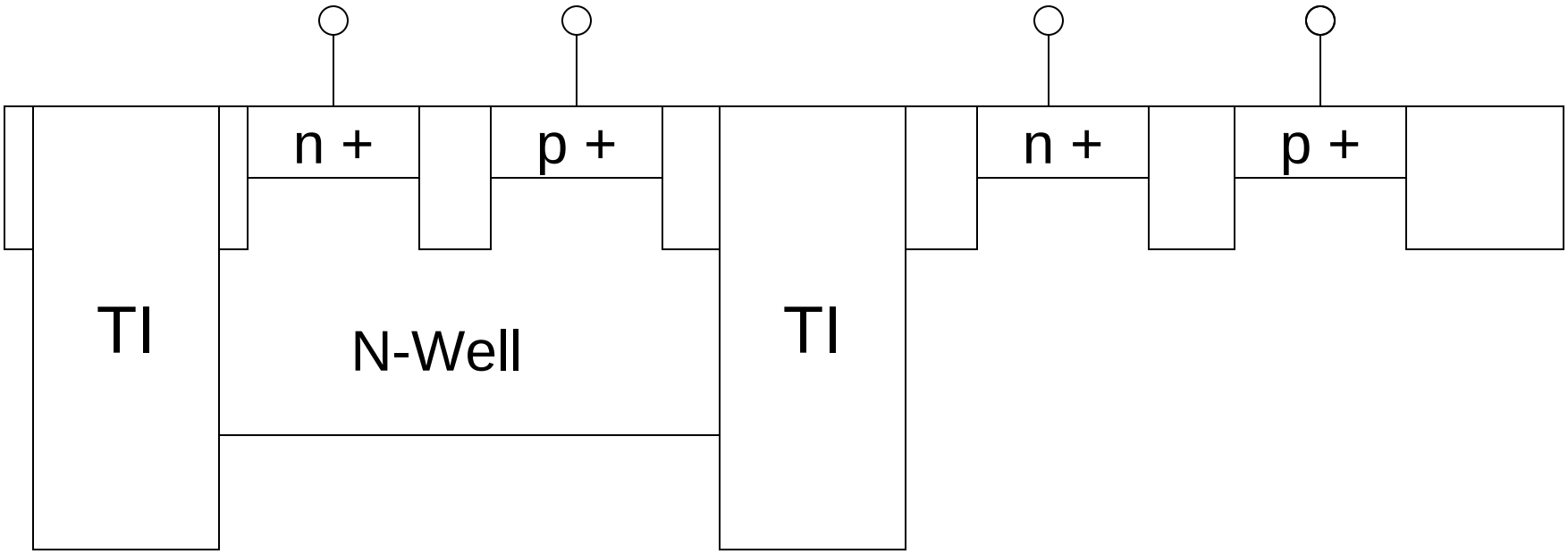
Latchup 2007

Latchup Structures – Deep Trench



Watson, Voldman IRPS 2004

Latchup Structures – Trench Isolation

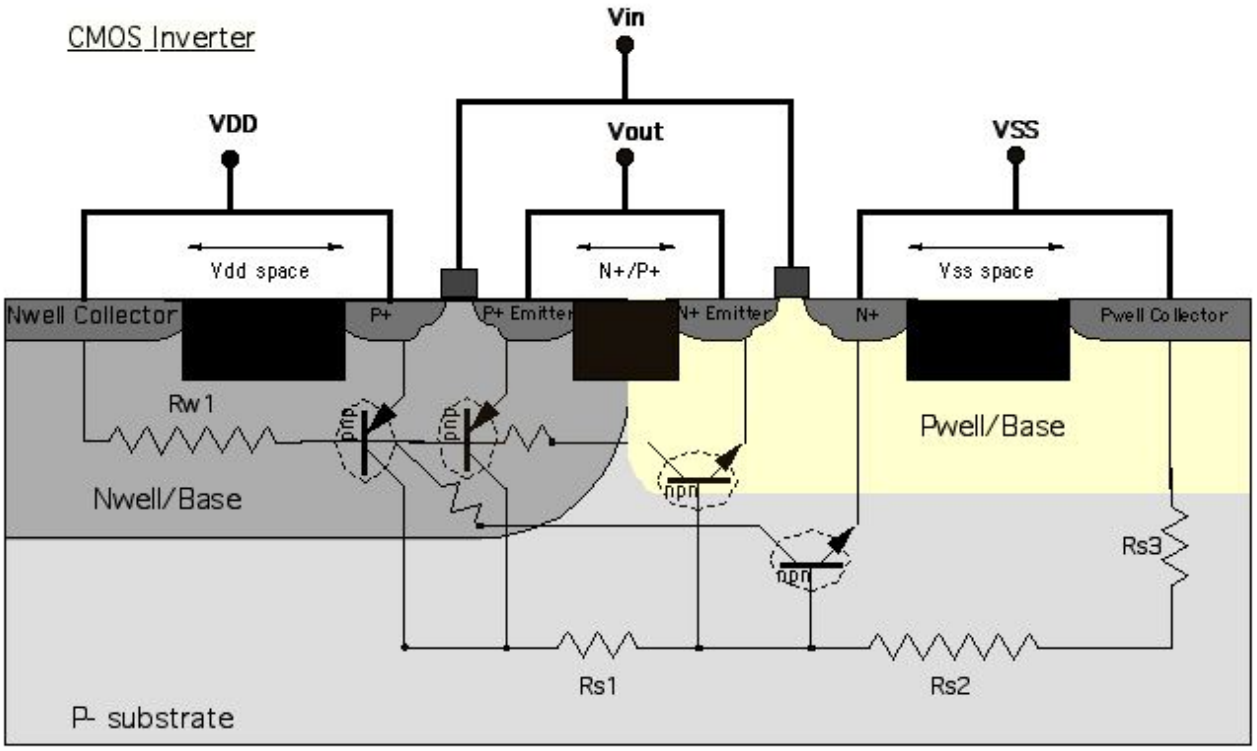


LATCHUP

SIMULATION

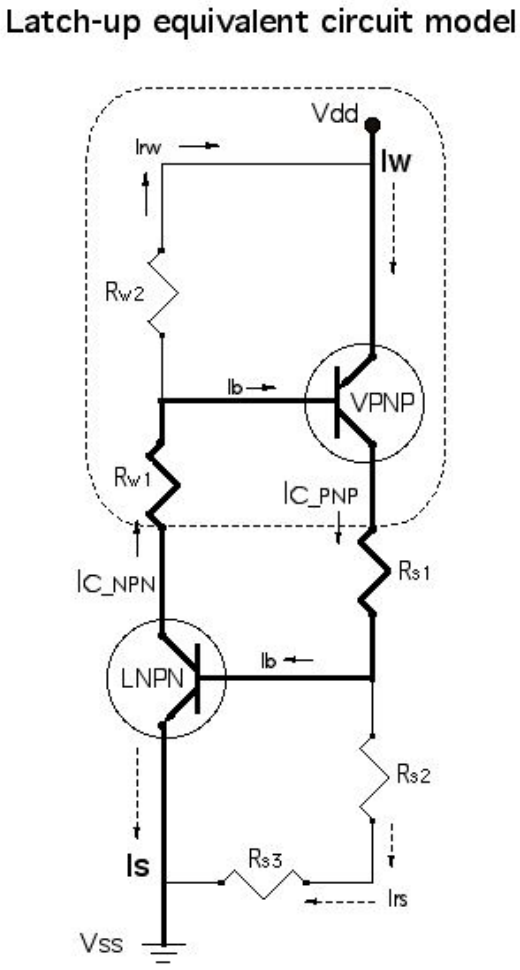
***Latchup* 2007**

Latchup Simulation Structure



***Latchup* 2007**

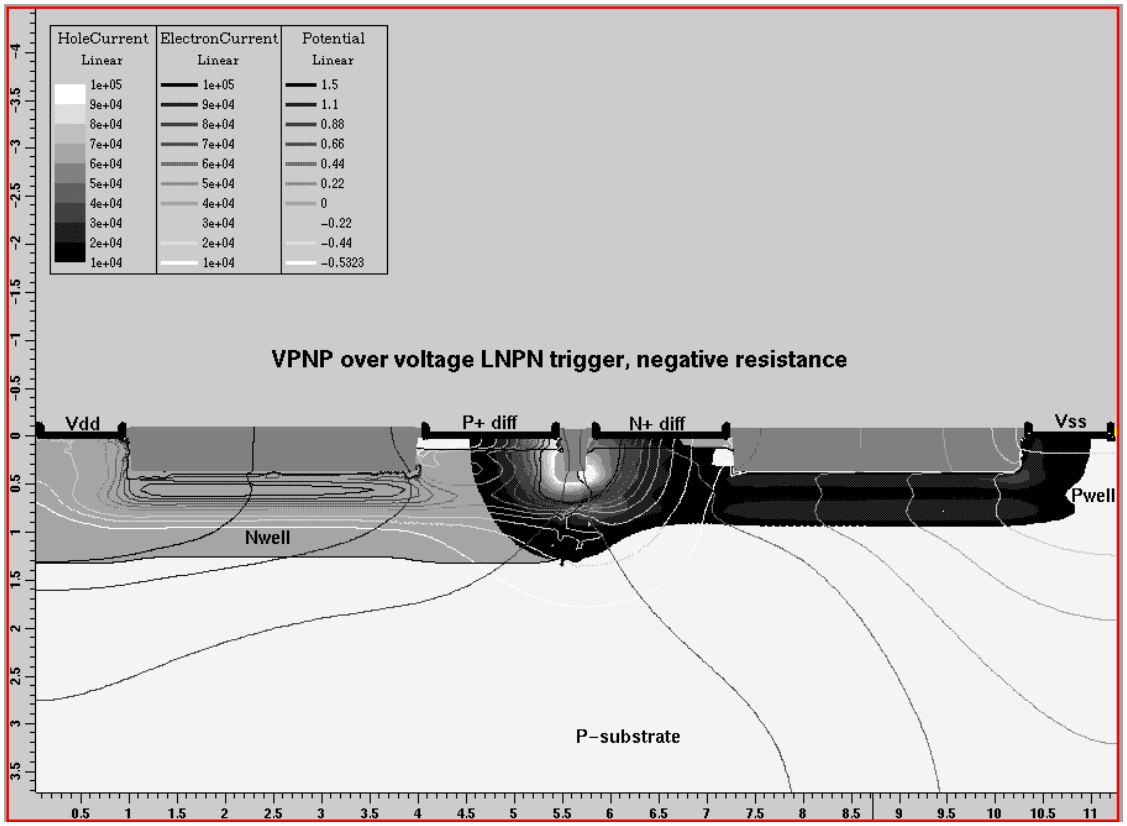
Latchup Equivalent Circuit Model



Morris IRPS 2003

Simulation: PNP Overshoot

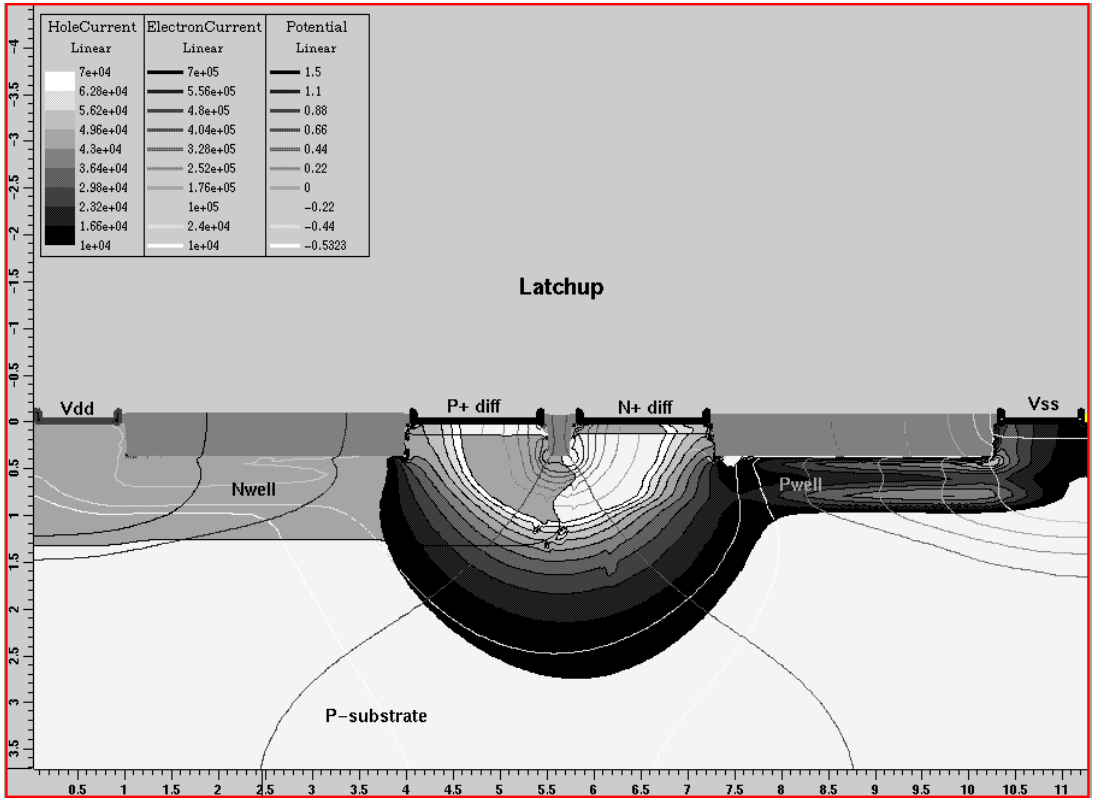
Negative Resistance Regime



Morris IRPS 2003

Latchup 2007

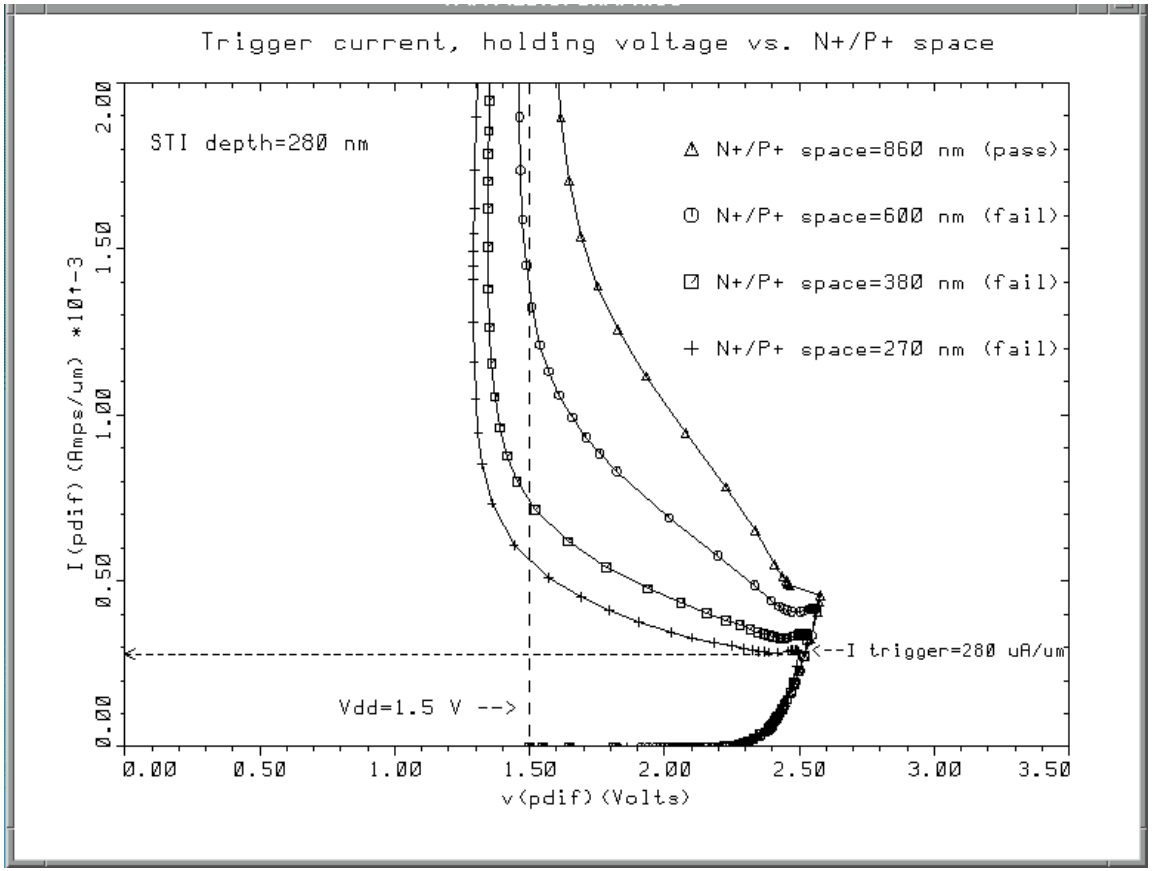
Simulation: Latchup State



Morris IRPS 2003

***Latchup* 2007**

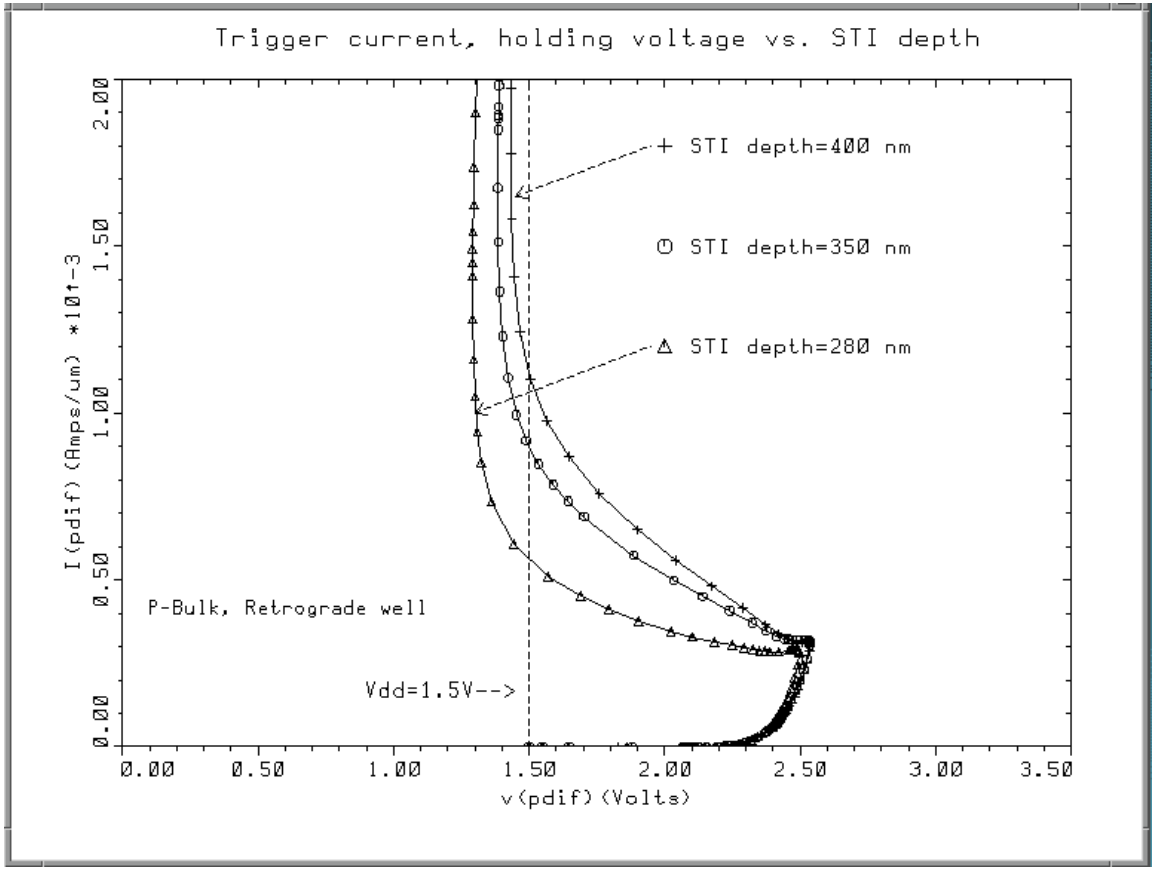
Simulation: N+/P+ Study



Morris IRPS 2003

***Latchup* 2007**

Simulation: STI Scaling



Morris IRPS 2003

***Latchup* 2007**

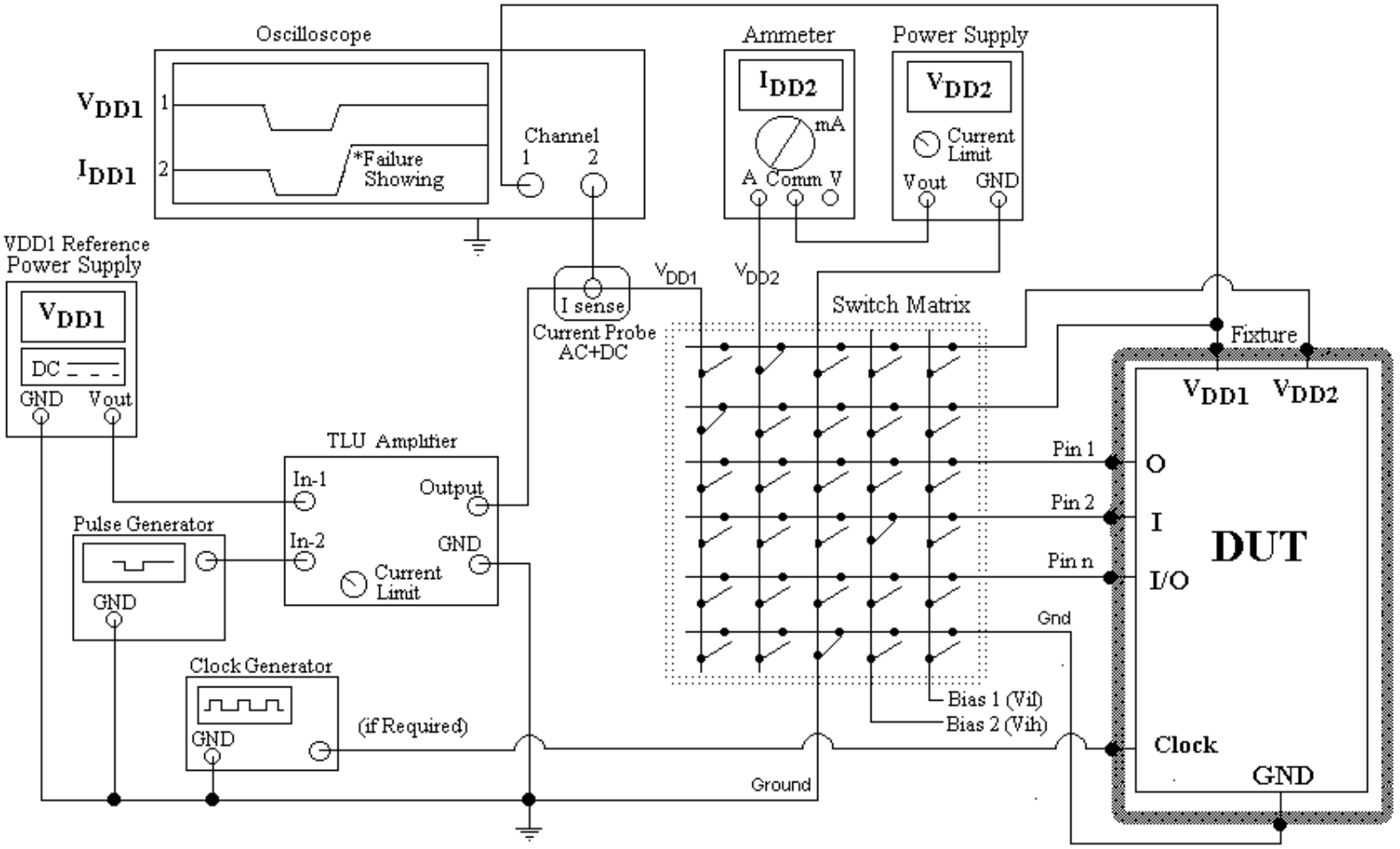
LATCHUP

LATCHUP PRODUCT TESTING

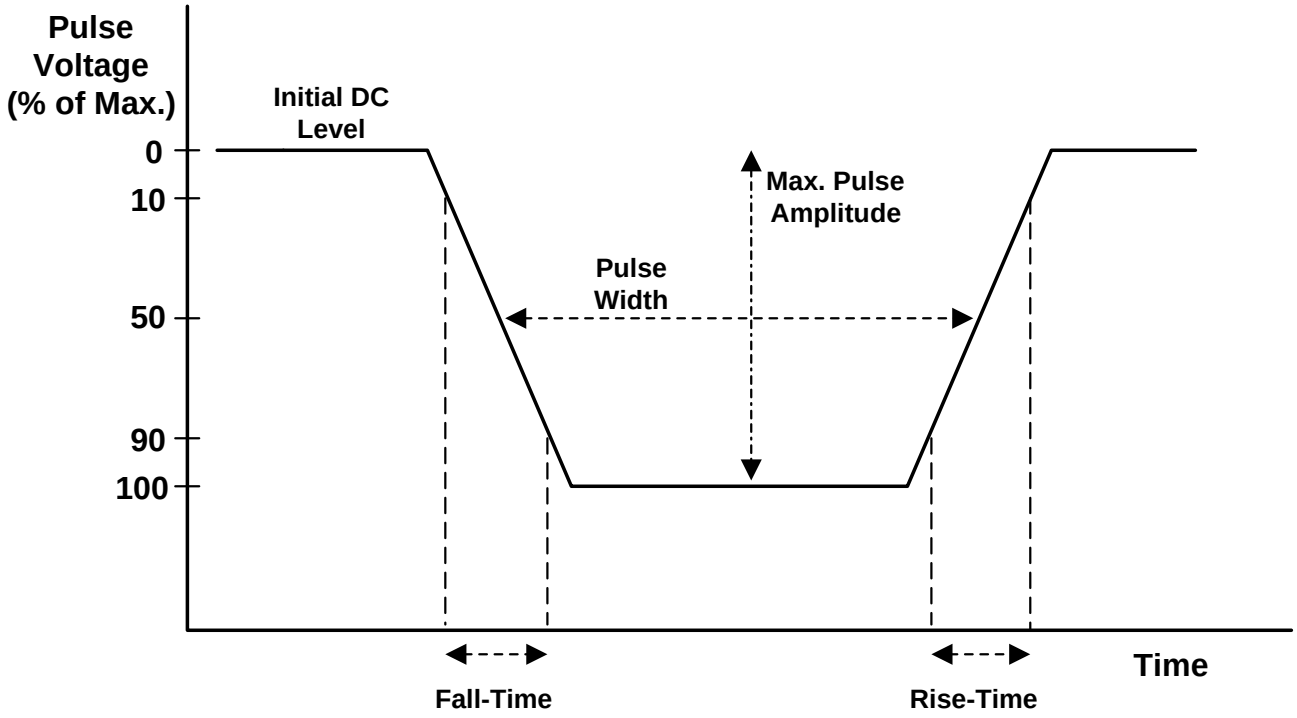
Transient Latchup Standard

- *ESD Association Standard Practice for Protection of Electrostatic Discharge Susceptible Items: Transient Latchup Testing – Component Level Supply Transient Simulation*
- Transient Latchup Test determines the response to different waveforms using a TLU Amplifier

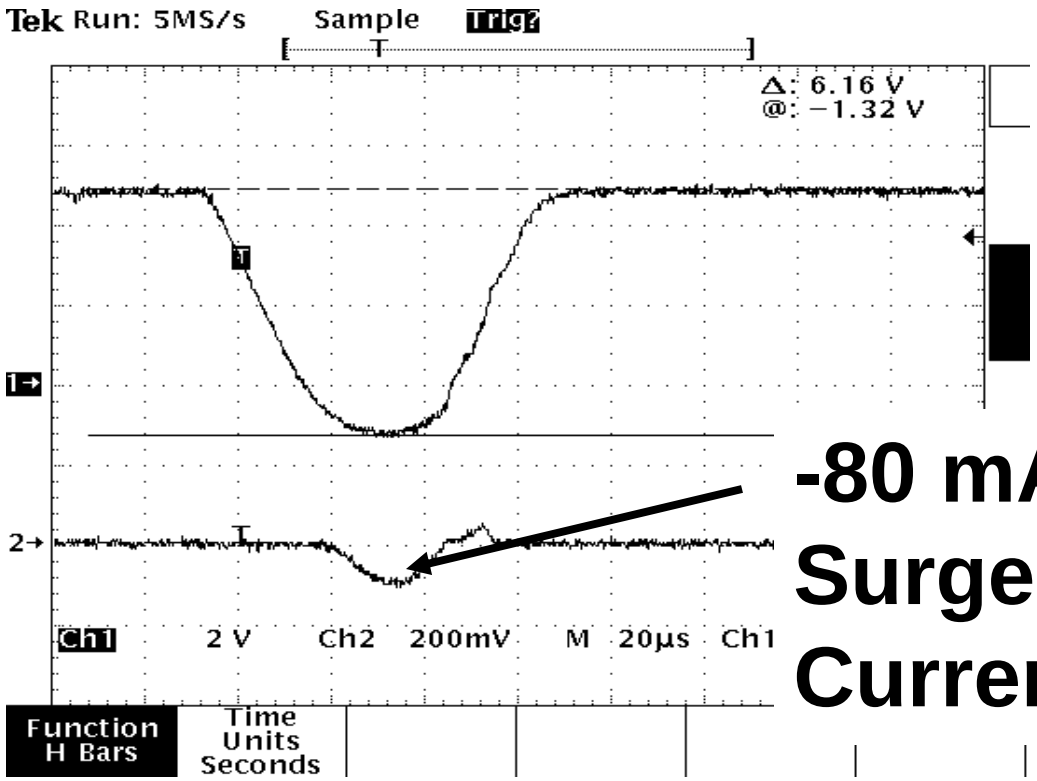
TLU Test Set up



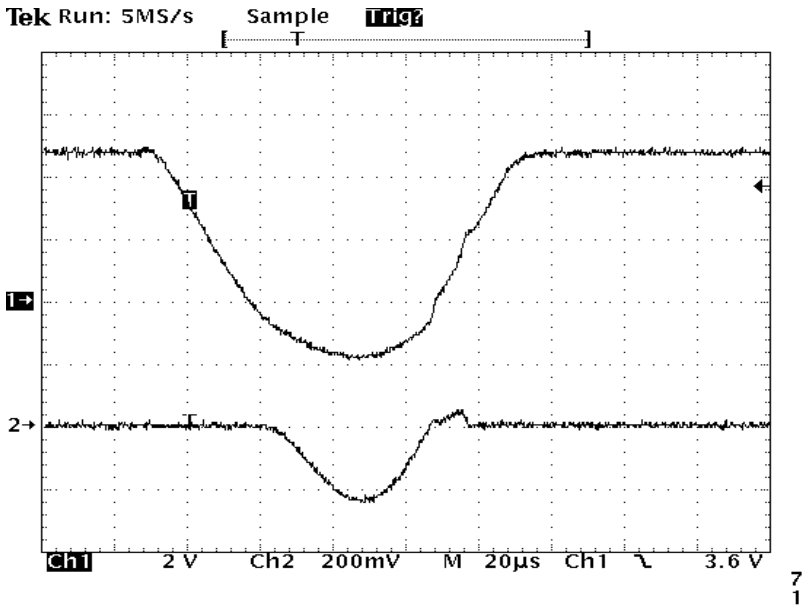
TLU Pulse Waveform

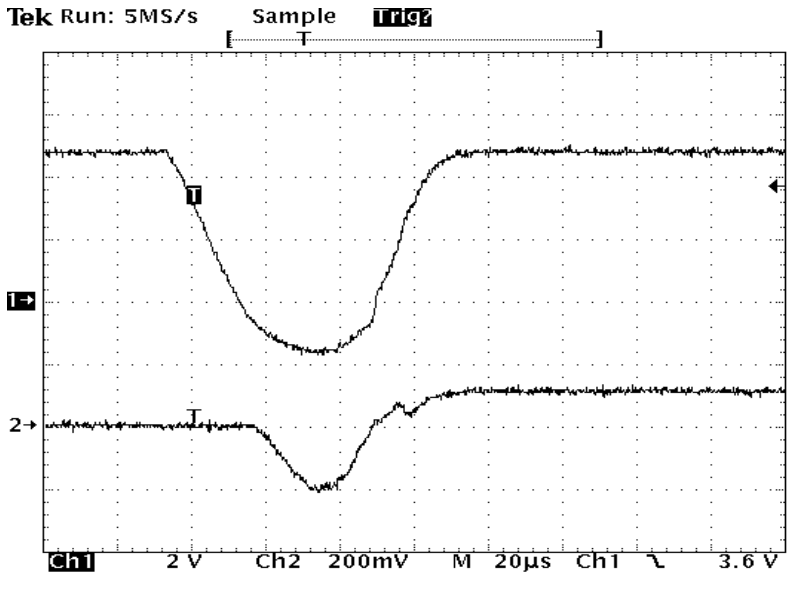


TLU Latchup Test: - 1.32 V Undershoot



TLU Pulse Width Dependence





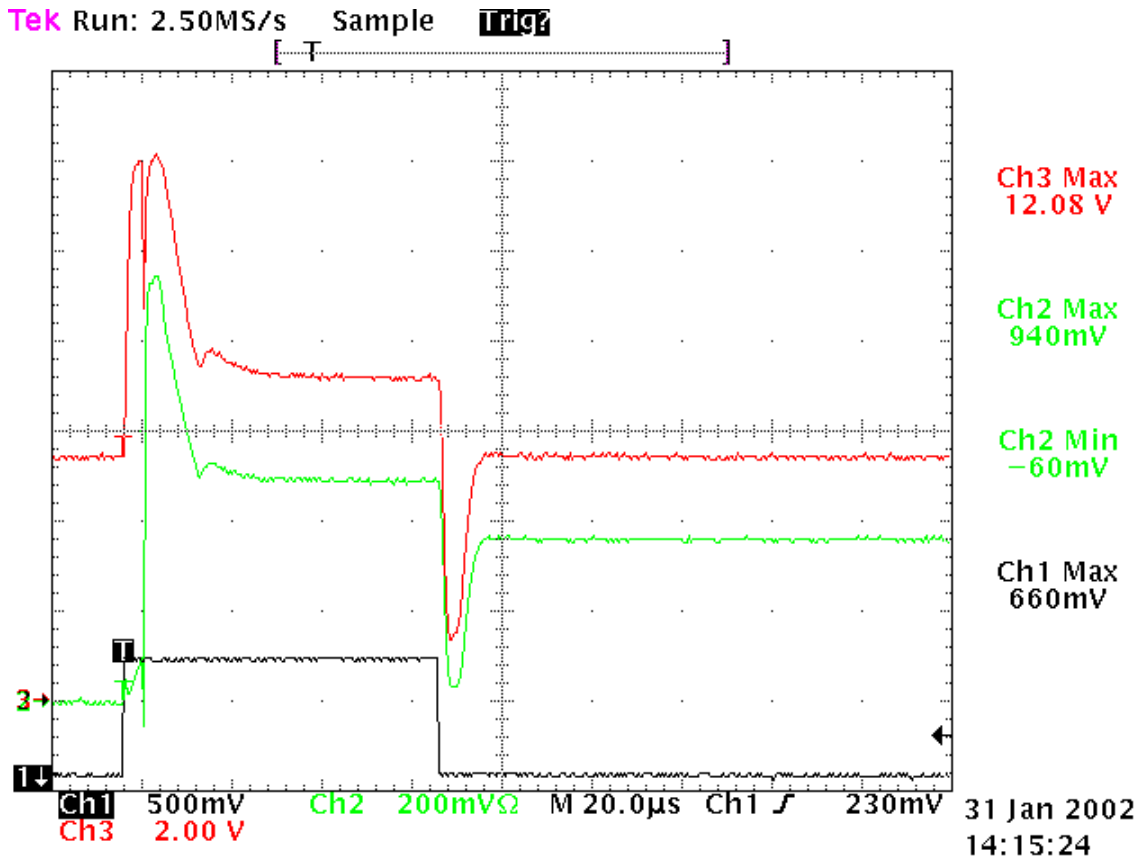
No Latchup

75 us

Latchup

62 us

Overshoot Latchup Sensitivity



Product sensitive to overshoot and undershoot phenomena

Smart Power and HVCMOS

- CMOS Concern increasing with Integration
  - Smart Power integration of 20-120 V applications with low voltage CMOS 0-5V
  - Integration Issues between DMOS, CMOS, and Bipolar Transistors

Smart Power and HVCMOS

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  - Smart Power integration of 20-120 V applications with low voltage CMOS 0-5V
  - Integration Issues between DMOS, CMOS, and Bipolar Transistors

Lateral and Vertical Issues

- Lateral and vertical transistors form in CMOS technology
- Dual Well - Lateral npn and pnp BJT
- Triple Well - Introduces vertical npn BJT

LATCHUP

CIRCUIT SOLUTIONS

Circuit Solutions

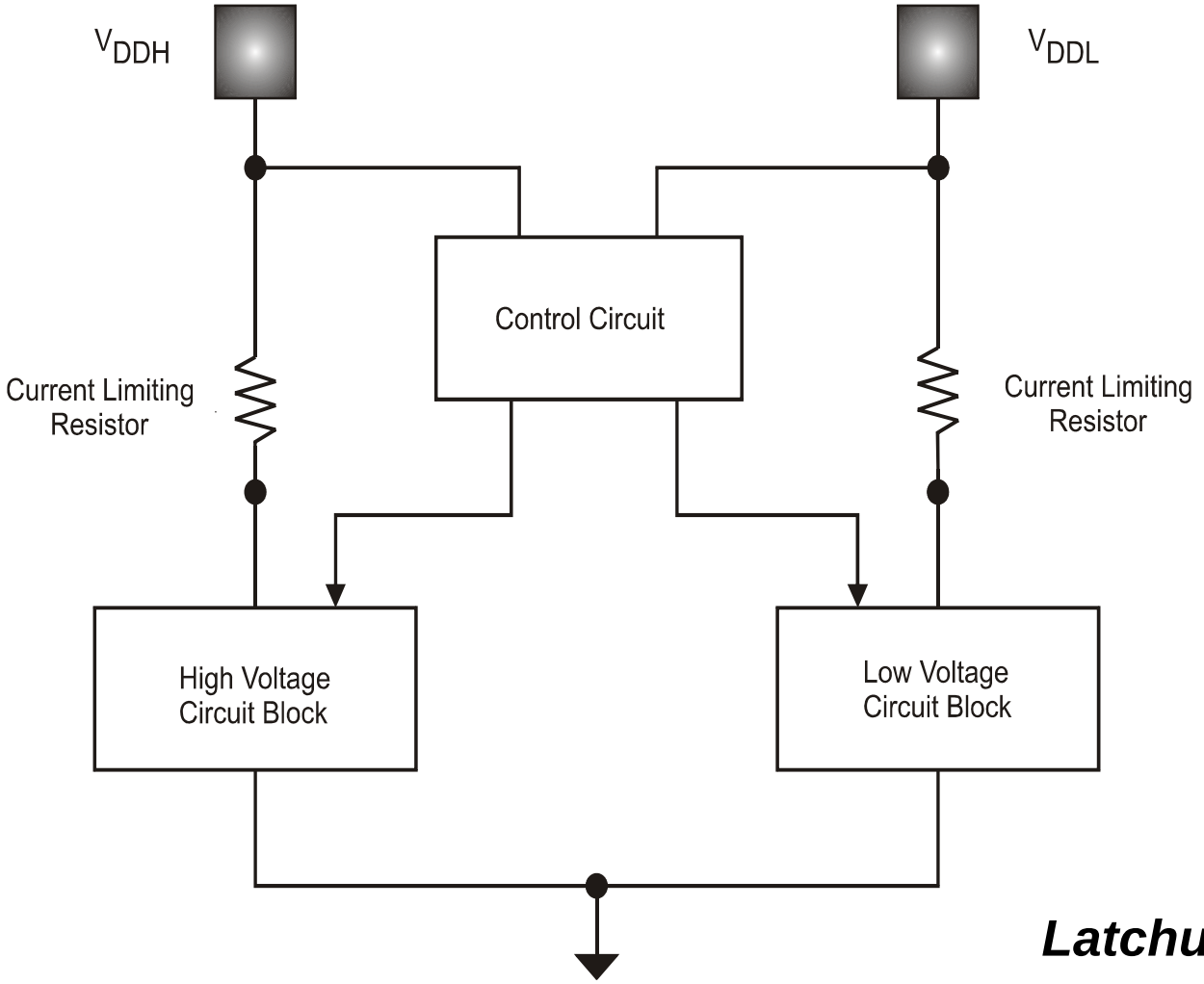
- Power Supply Current Limit
- Power Supply Voltage Limit
- Multiple Power Supply Sequencing Circuitry
- Anti-Overshoot Circuit
- Anti-Undershoot Circuit
- Active Guard Rings
- Compensating Active Guard Rings

LATCHUP

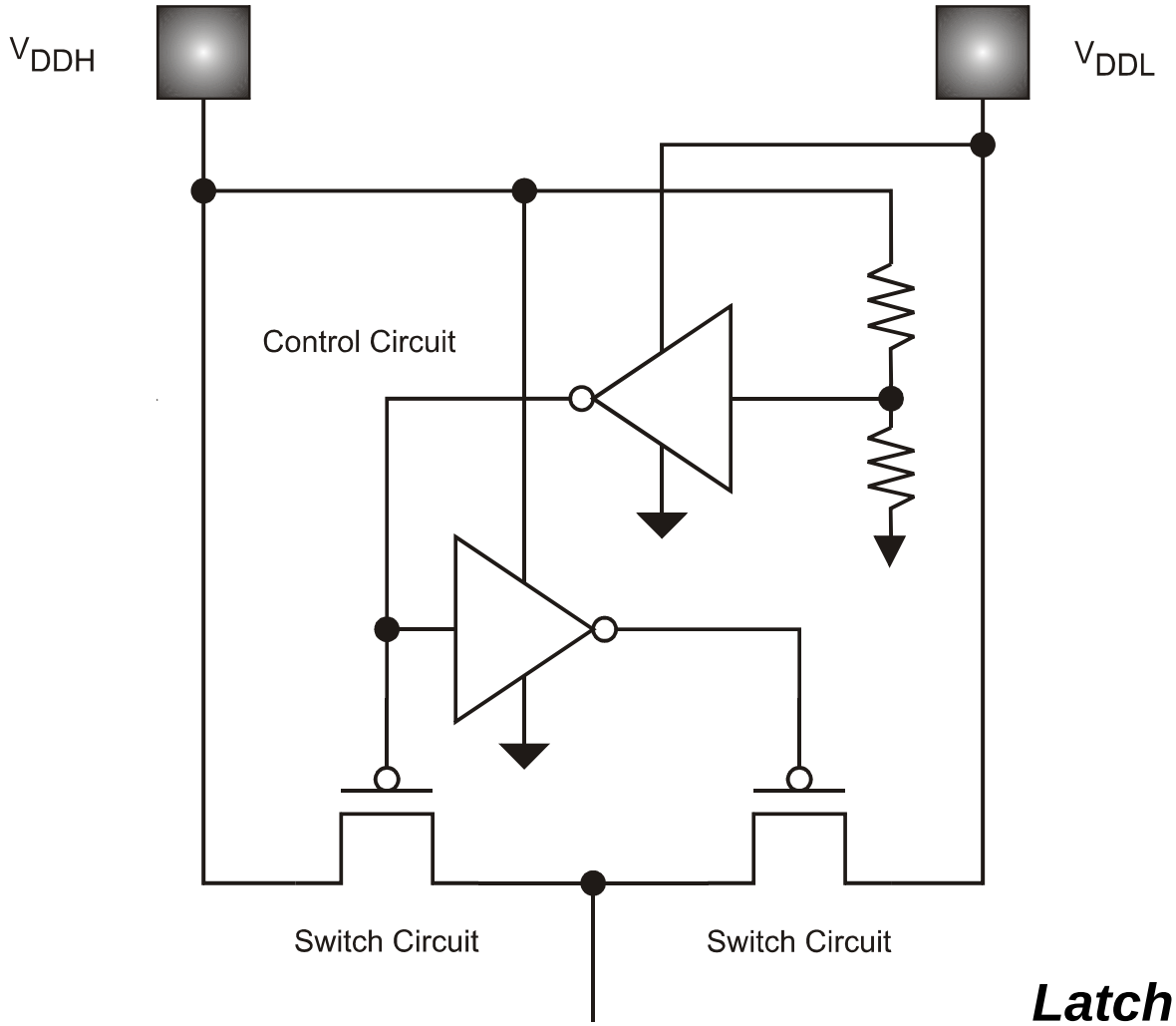
MULTIPLE POWER SUPPLY SEQUENCING NETWORKS

***Latchup* 2007**

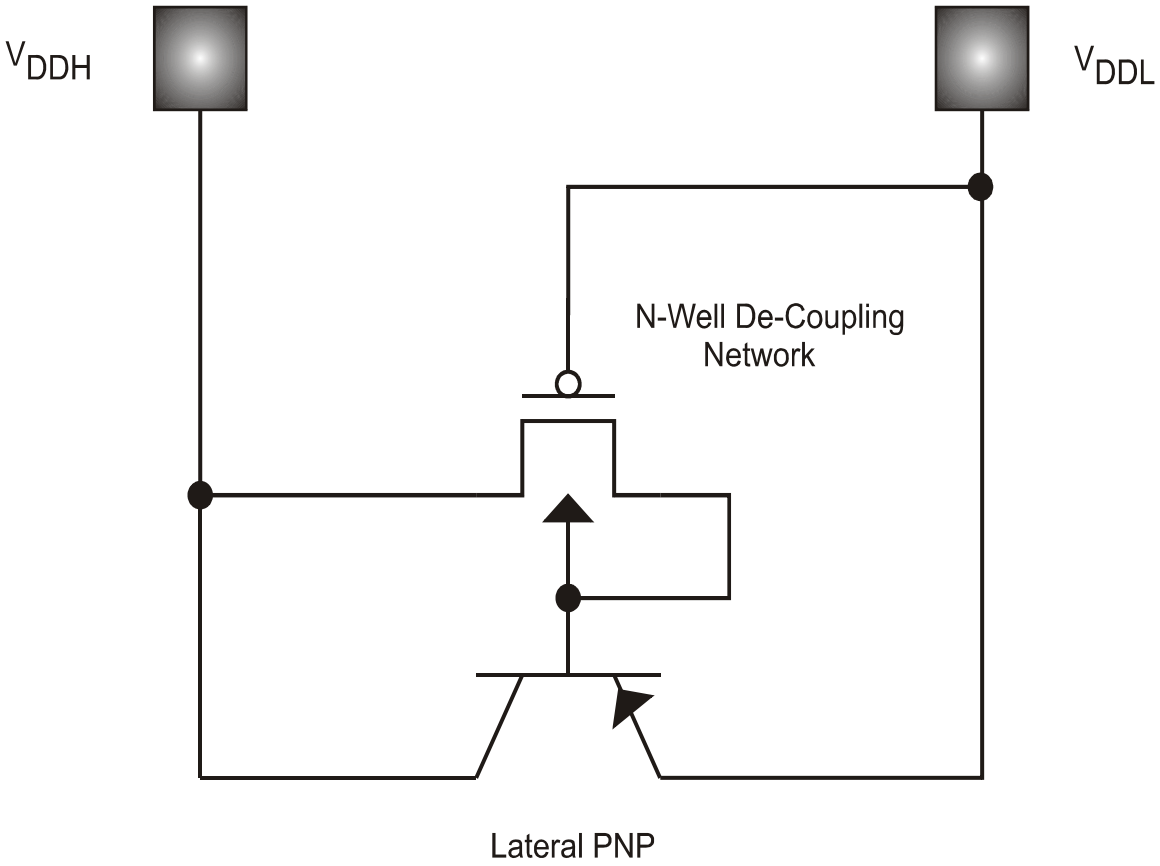
Current Control Network



Power Supply Sequencing System



Sequence Independent Network



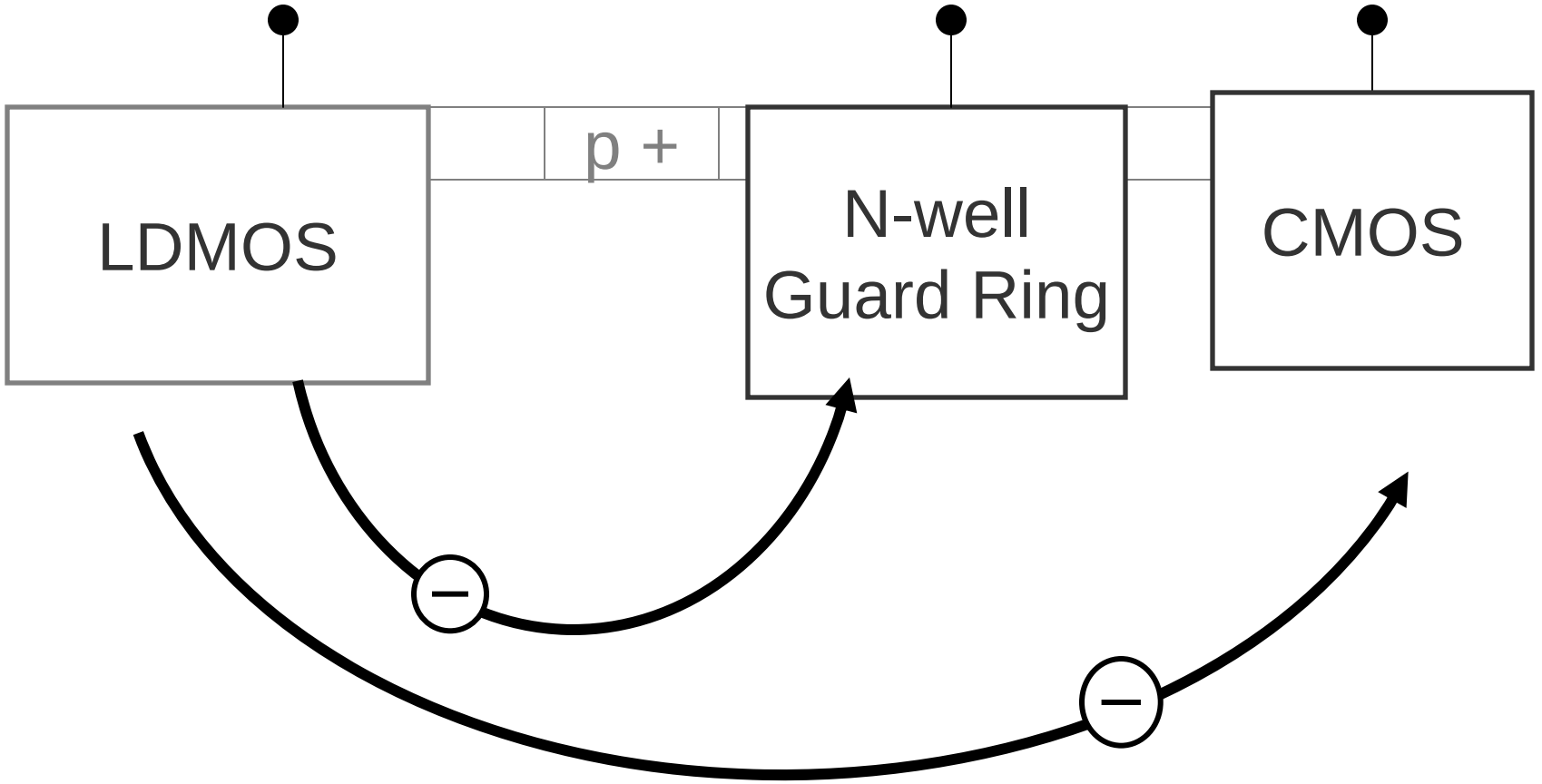
Switch Circuit

LATCHUP

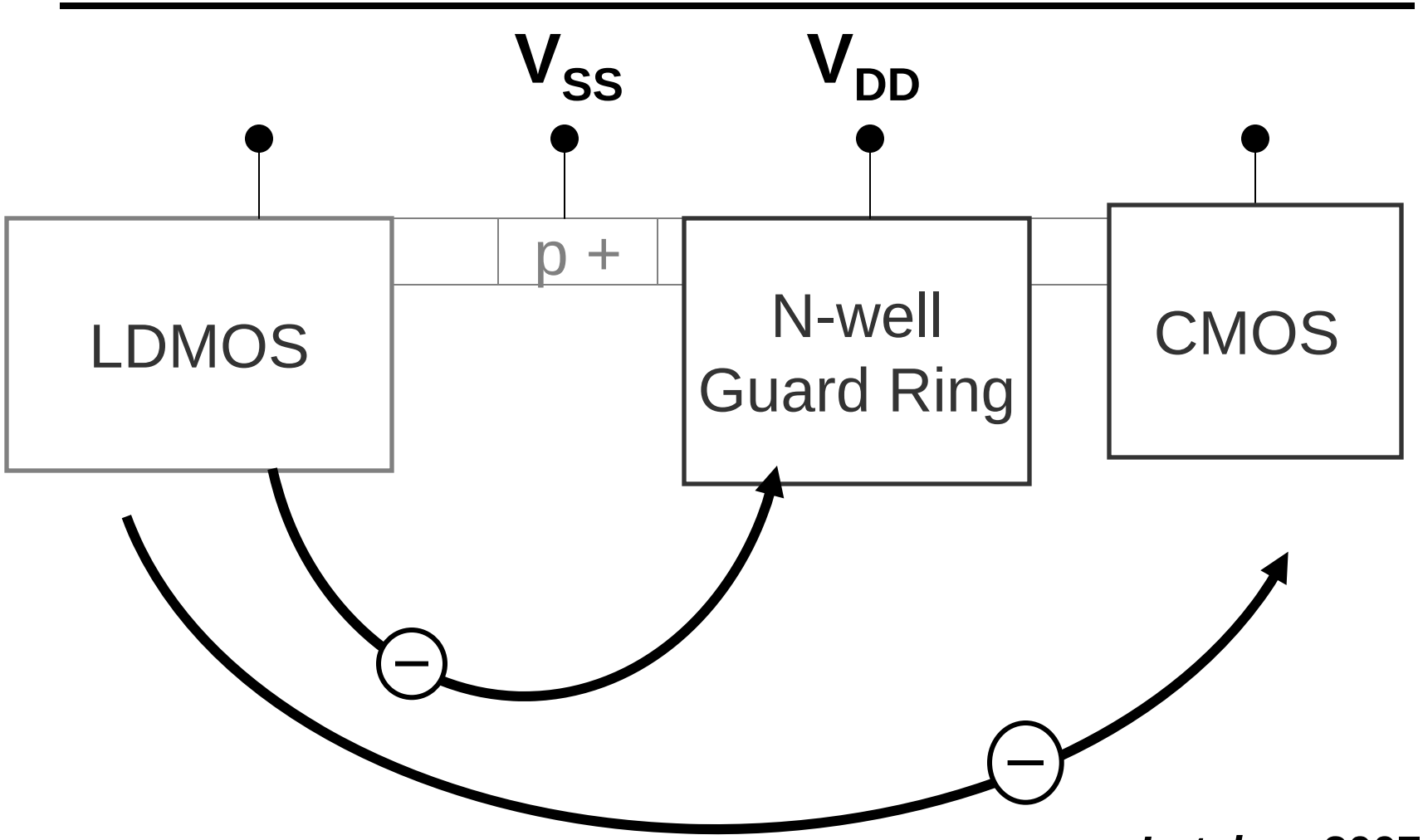
ACTIVE GUARD RINGS

***Latchup* 2007**

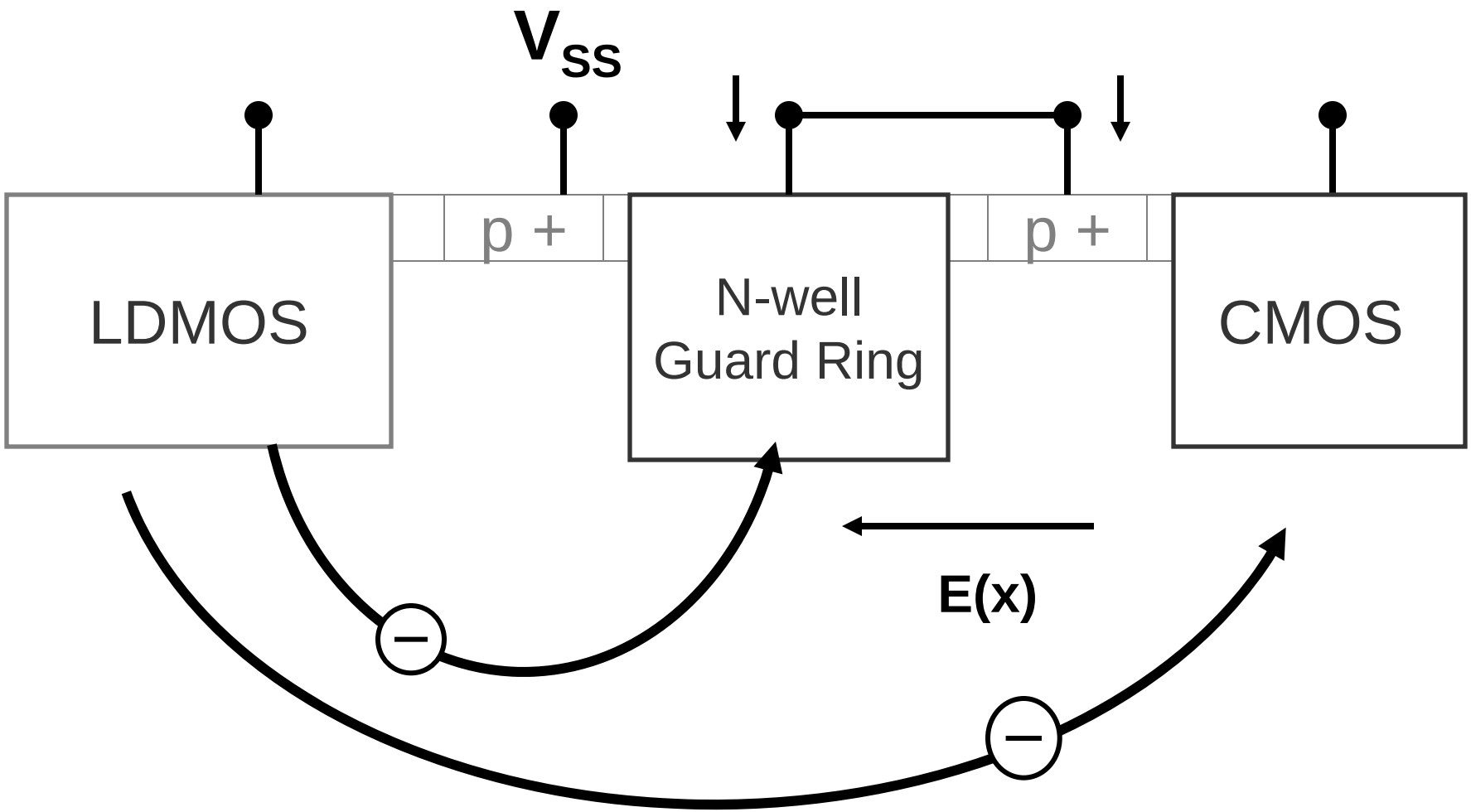
Guard Rings - LDMOS to CMOS



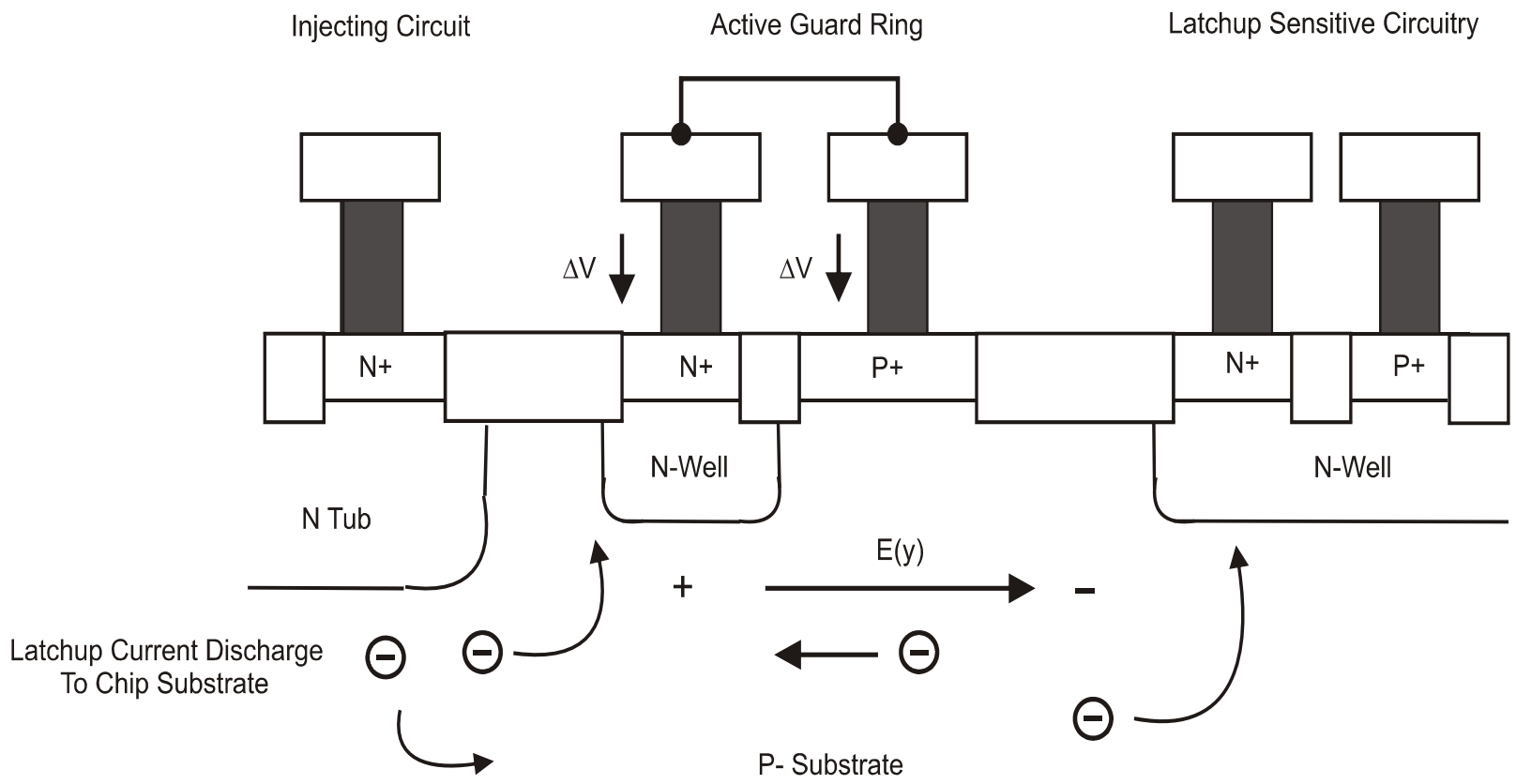
Passive Guard Rings



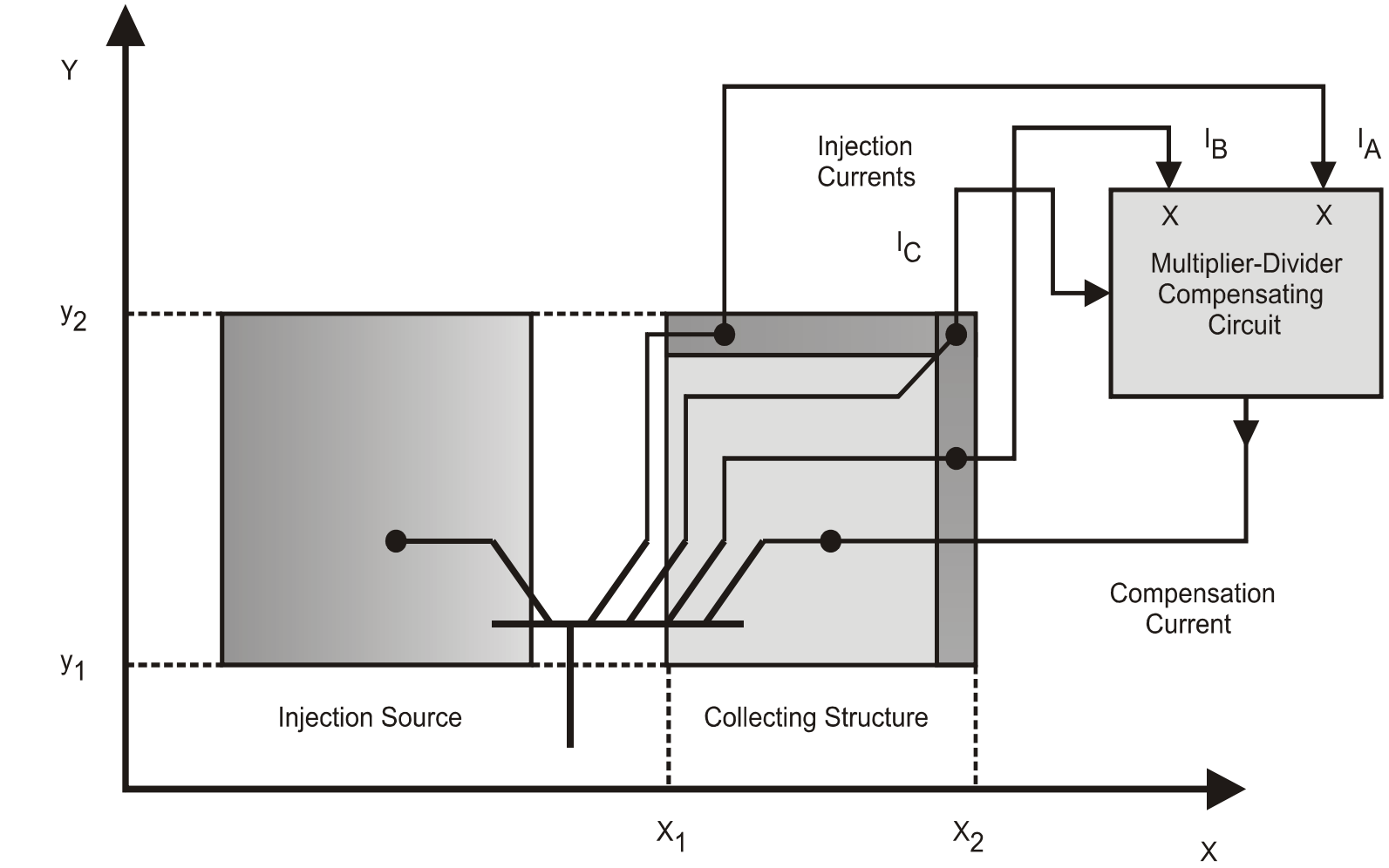
Active Guard Rings



Active Guard Rings



Active Compensation Guard Rings



Latchup Design System

- Latchup CAD methods are focused on the semiconductor device of PNPN and how the process affects it
- Latchup CAD layout/rules in the following areas:
- - PNPN Extraction
- - Inter-domain Latchup Interactions
- - Guard Ring Automation and Design
- - Internal Latchup Rules
- - External Latchup Rules

Latchup Computer Aided Design
Layout Extraction Techniques

***Latchup* 2007**

Latchup CAD Design Issues

- Identify PNPNs
- Identification of Guard Rings
- Improvement of Guard Rings
- Inter-domain parasitic problems
- Injection phenomena
- Satisfying ground rules

CAD – Extraction of PNPNs

- Extraction of PNPN
- Sorting of PNPNs and Rules
- Integration with Circuit Schematics

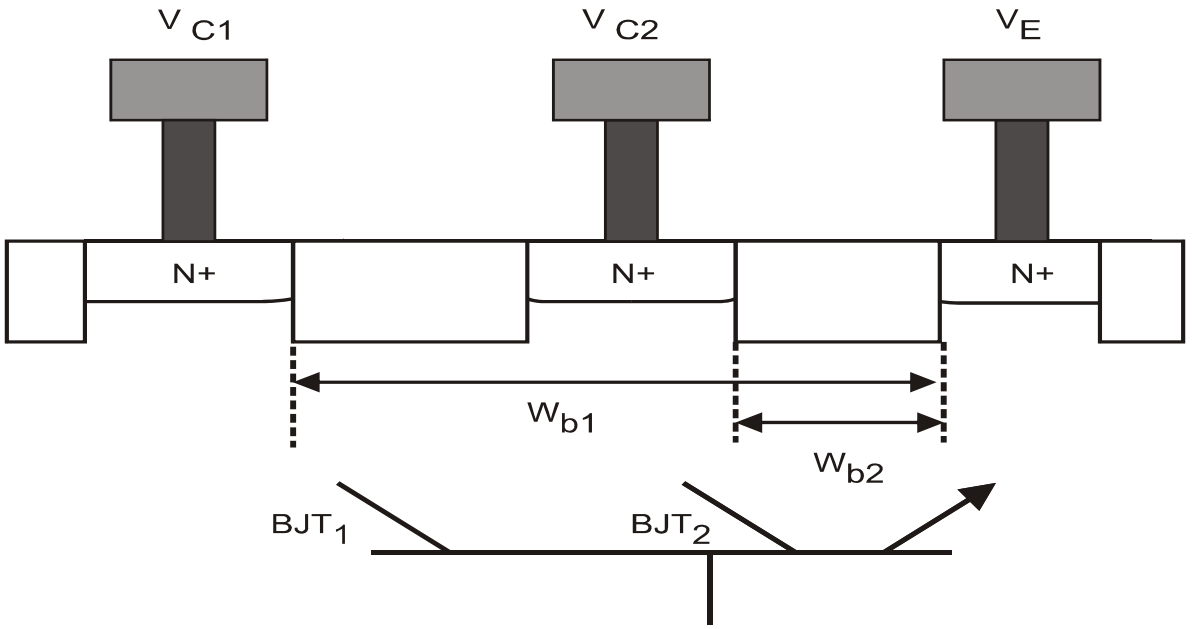
Tong Li Latchup CAD Method

- Methodology useful for Latchup:
- Device Extraction - A method to extract actual devices.

- Stress Annotation - A method to determine the electrical potentials and classify the level of important stress conditions.

- Bipolar Junction Transistor Extraction - Extraction of parasitic bipolar transistors, and means to determine the “critical” transistors.

Extraction of Parasitic Bipolars



Reduction Rules

IF $V_{C1} < V_{C2}$ AND $\beta_1 < \beta_2$ Remove BJT_1

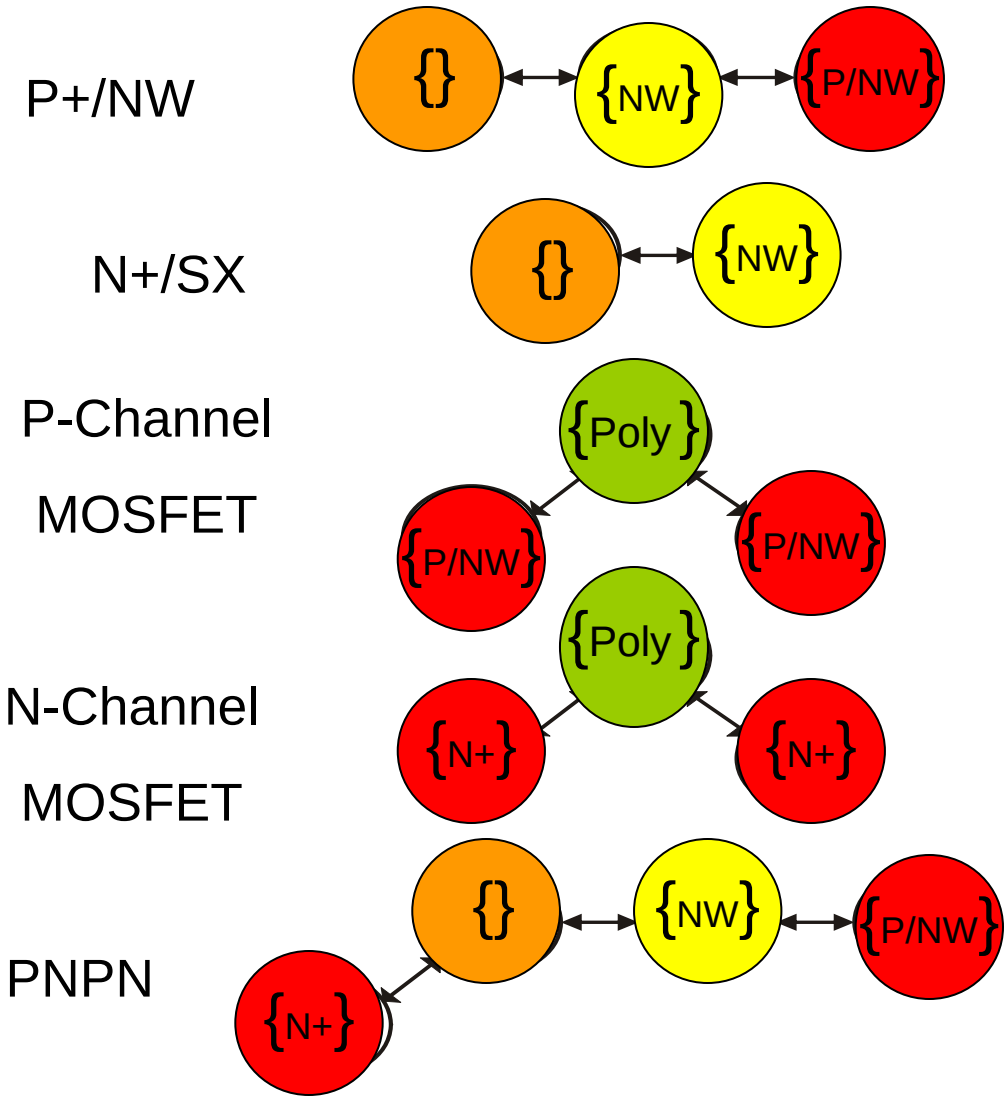
IF $V_{C1} < V_{C2}$ AND $\beta_1 = \beta_2$ Remove BJT_1

IF $V_{C1} = V_{C2}$ AND $\beta_1 < \beta_2$ Remove BJT_1

CAD Extraction Methodology (Zhan-Feng-Wu-Chen-Guan-Wang Method)

- Model Graphs (MG) formed for all devices
- Model Graphs formed for Parasitic PNPN Elements

Extraction Models

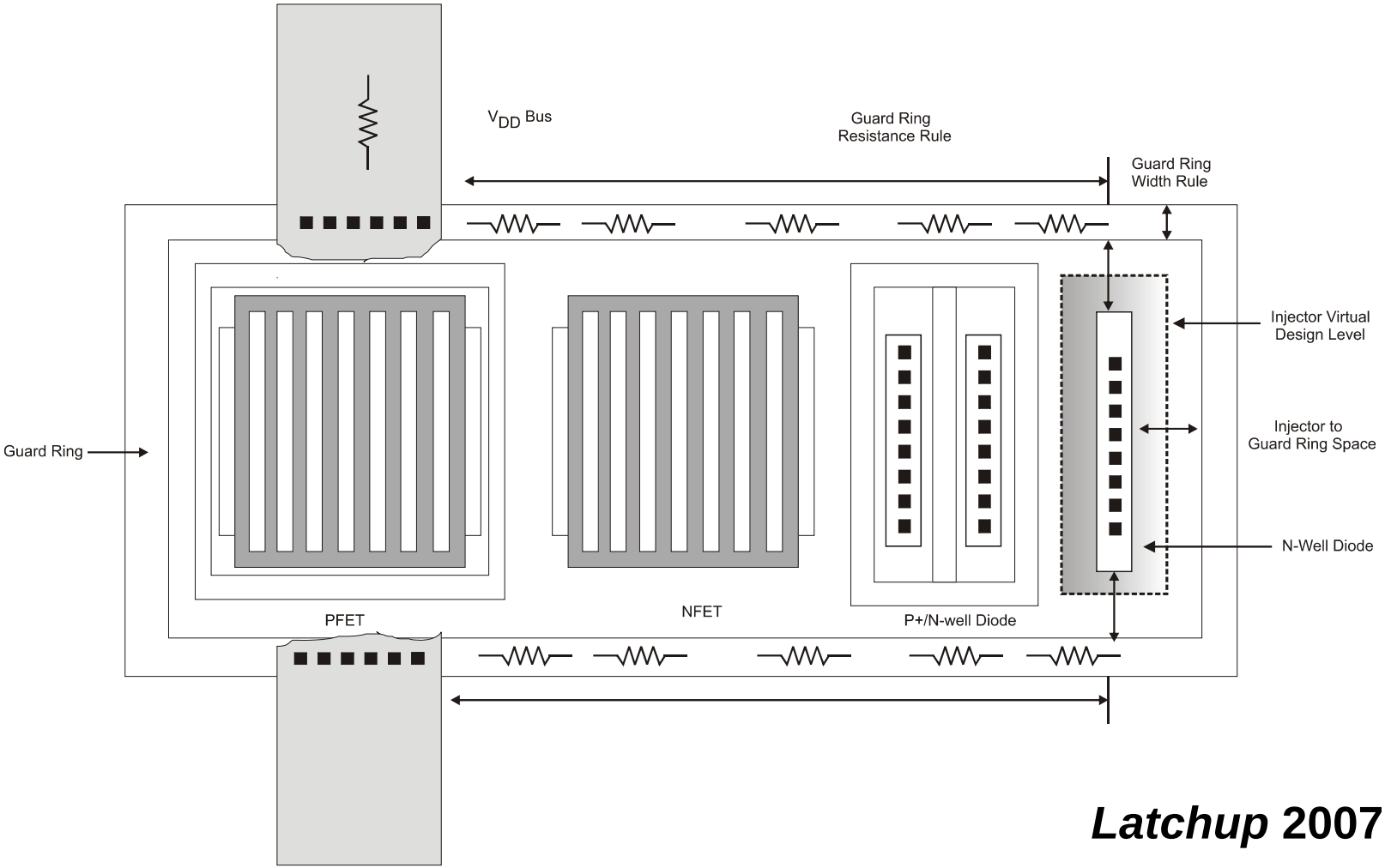


R.Y. Zhan, A. Wang

CAD – Guard Rings

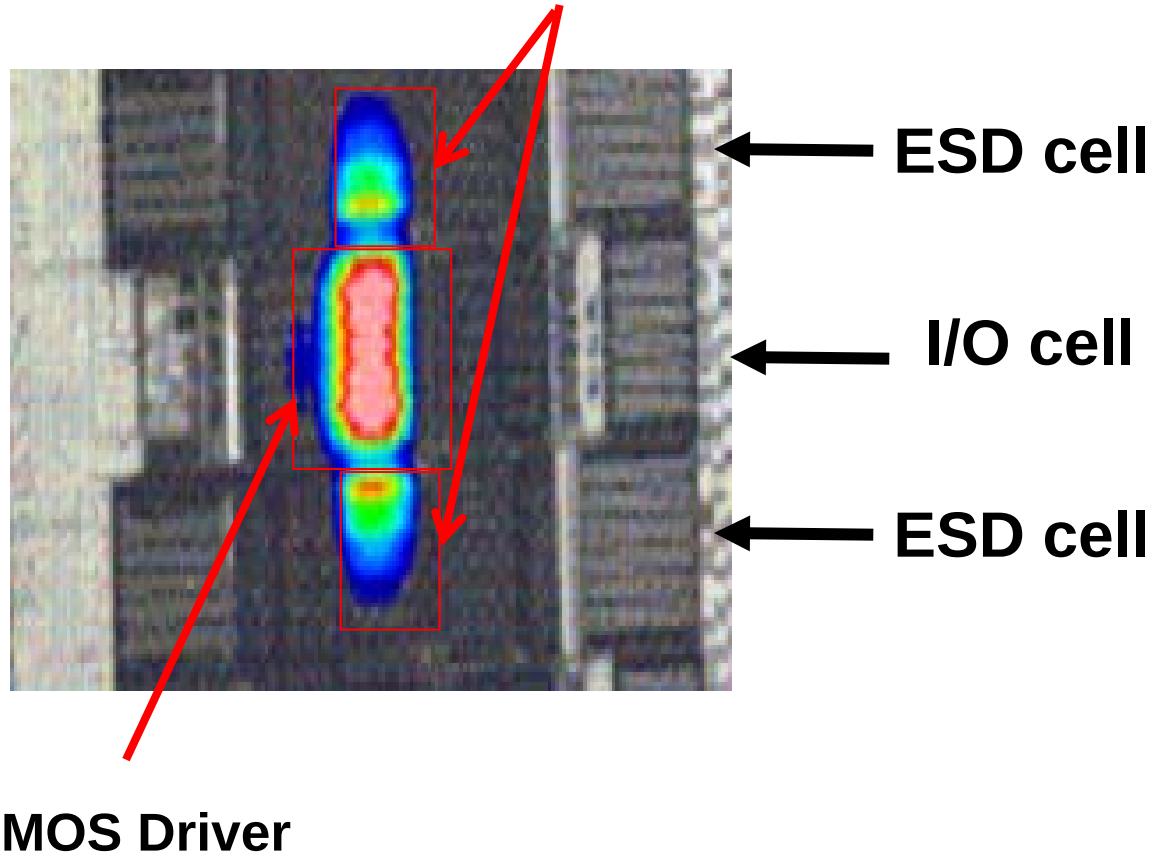
- Checking of Guard Ring Rules
- Verification of Guard Ring Rules
- Post-Processing Generation of Guard Rings
- Guard Ring Parameterized Cells (PCell)

Guard Ring Resistance



Intra- and Inter-Domain Latchup and Design Rule Development

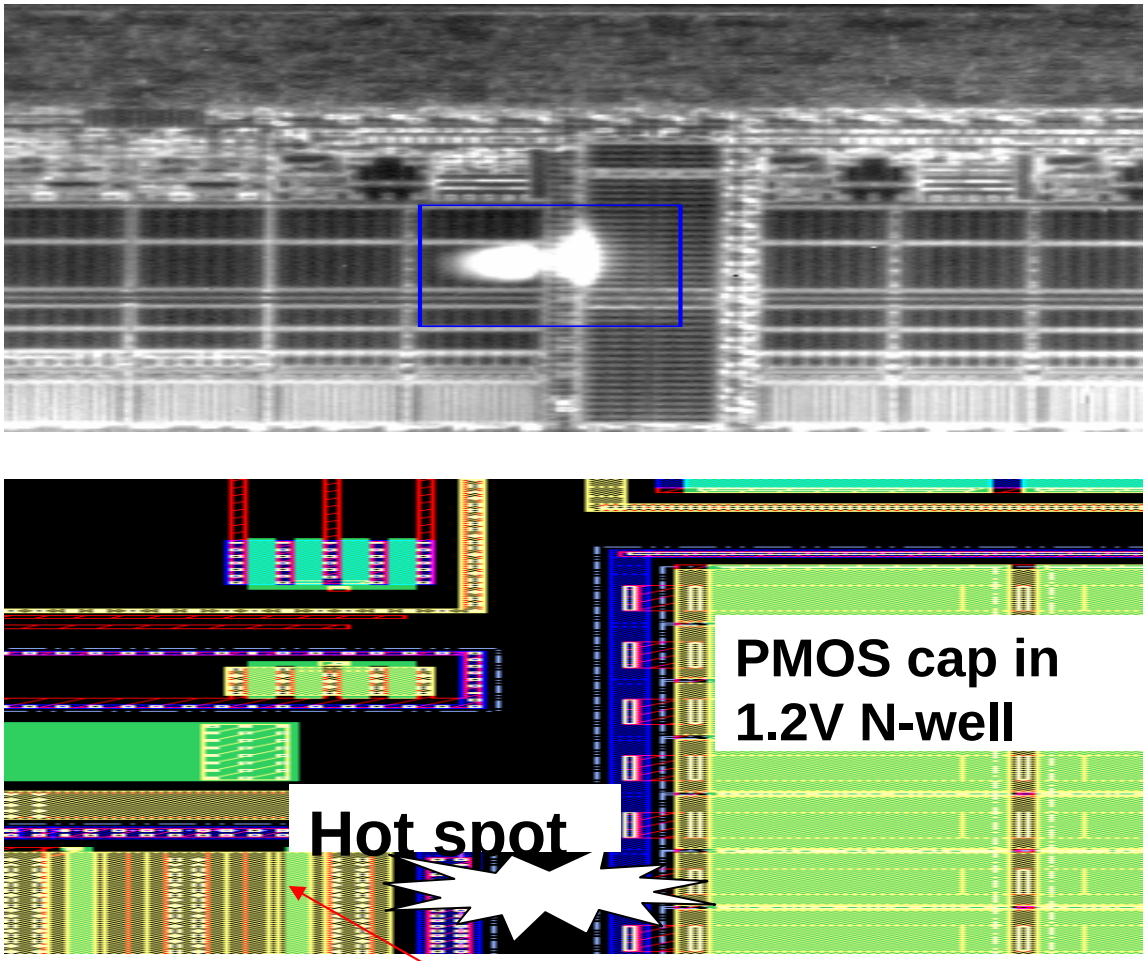
Inter-Circuit Latchup



Latchup 2007

Y. Huh EOS/ESD 2003

Inter-Circuit Latchup



Y. Huh EOS/ESD 2003

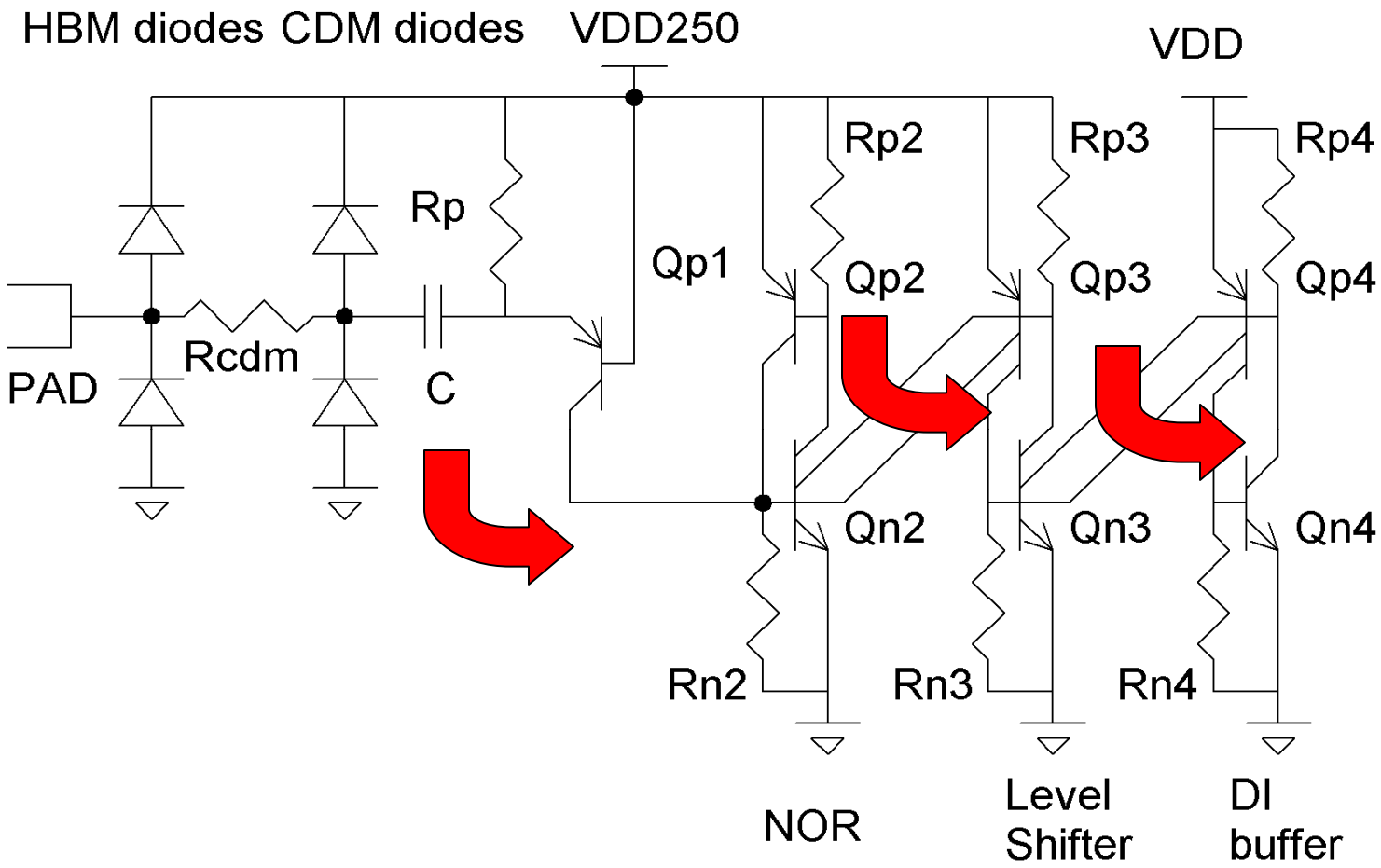
External Latchup
Design Rules and Automation

***Latchup* 2007**

Internal and External Latchup

- Internal Latchup - Injection phenomenon within the pnpn structure
- External Latchup – Injection phenomenon outside of the pnpn strucure
- Internal latchup driven by process and design spacings
- External latchup driven by both external stimuli, and internal latchup parameters (e.g. process and spacings)

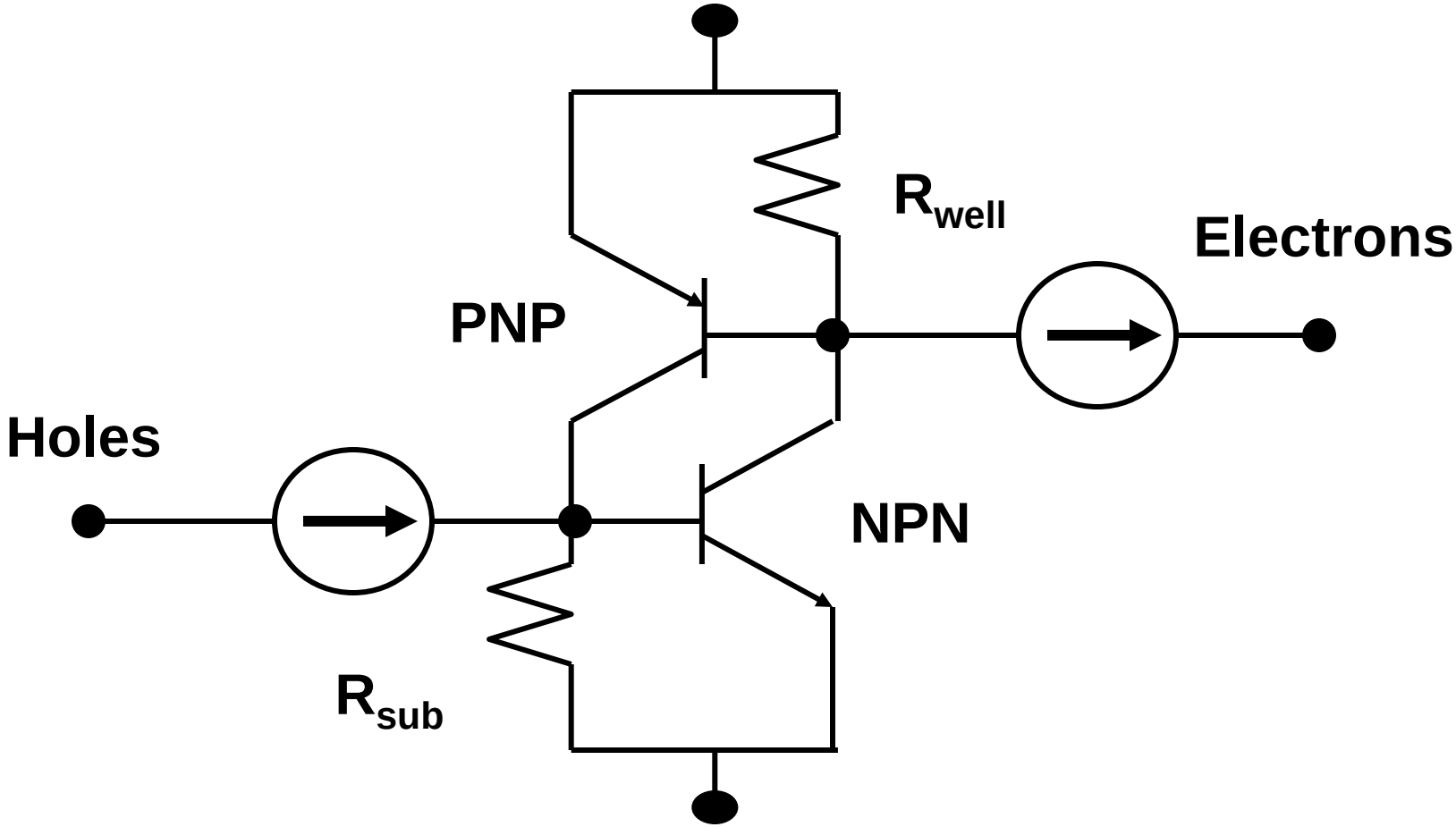
External Latchup: Domino Effect



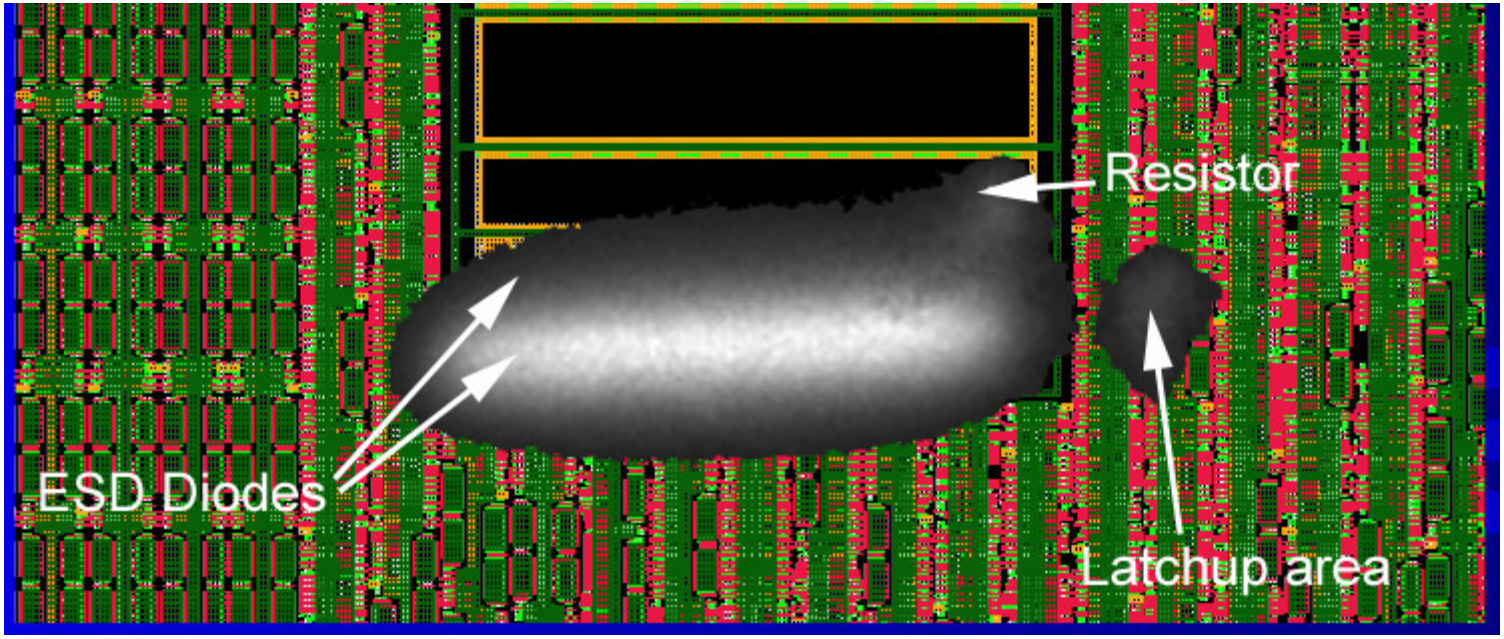
Mechler IRPS 2004

***Latchup* 2007**

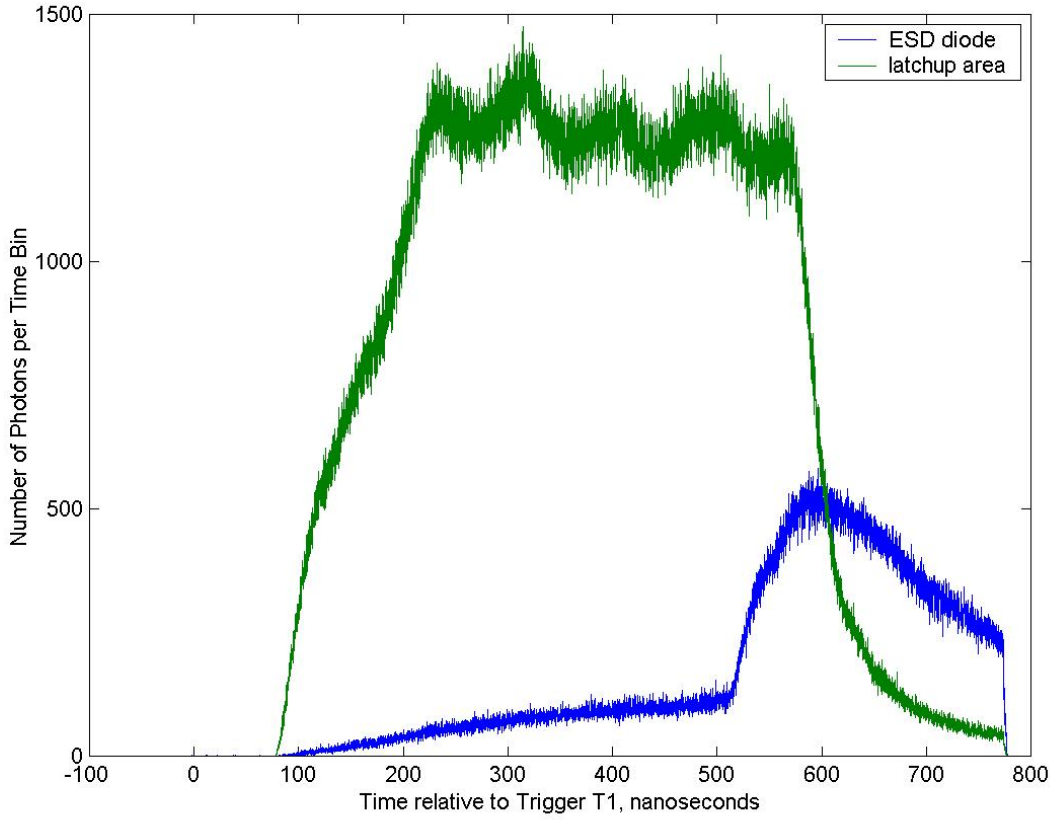
Latchup Network



Cable Discharge Event (CDE) Induced External Latchup



ESD-Induced Latchup



Weger IRPS 2003

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Latchup Characterization

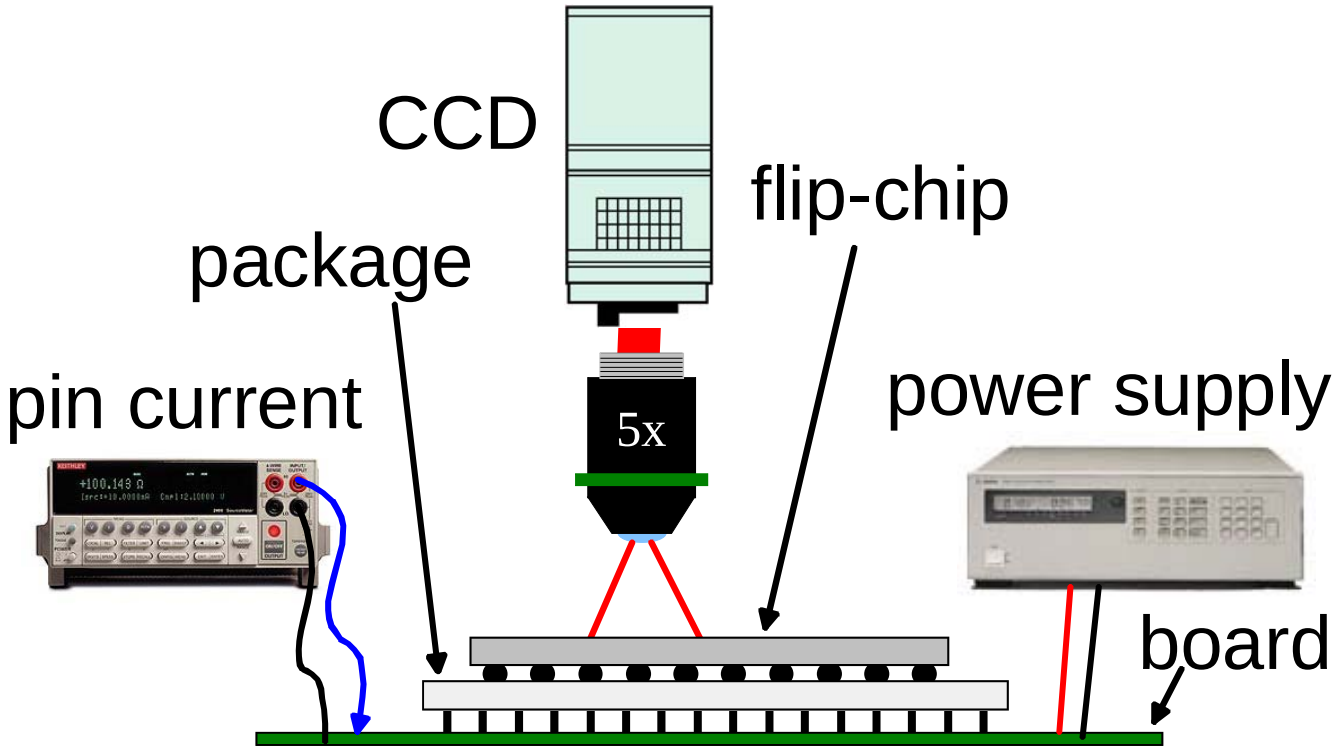
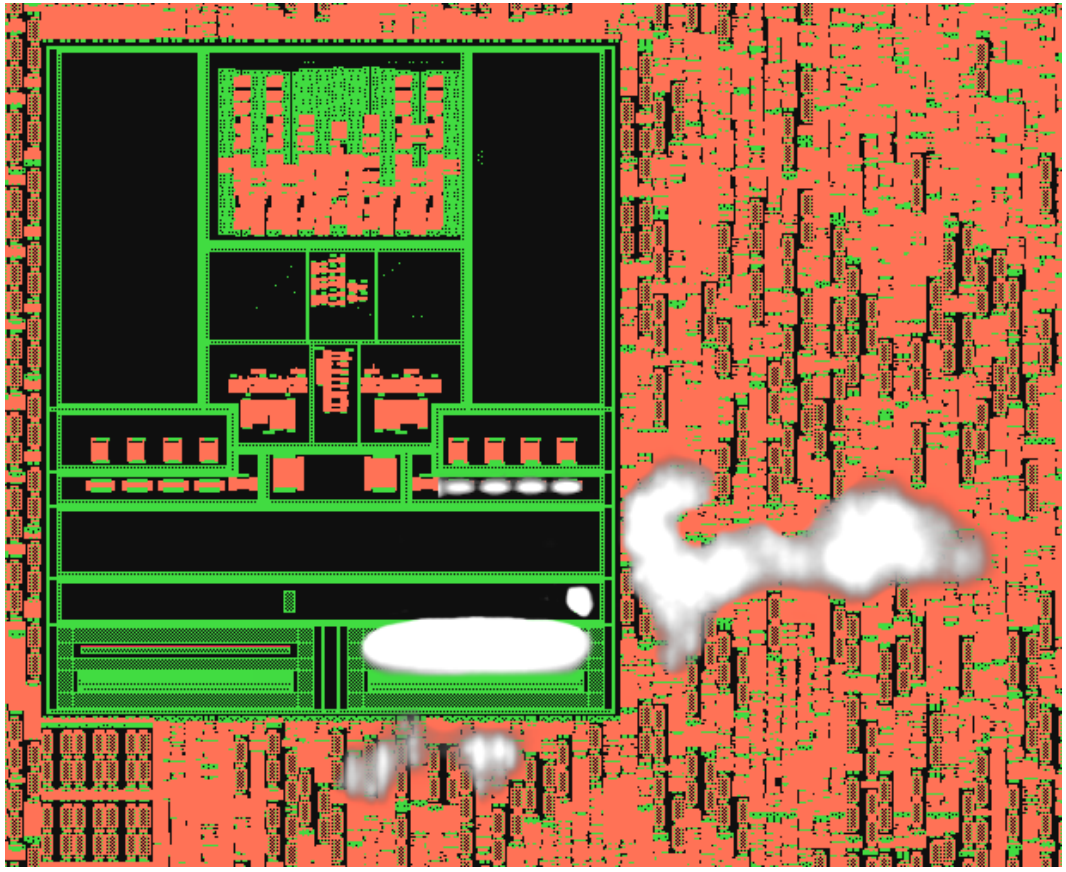


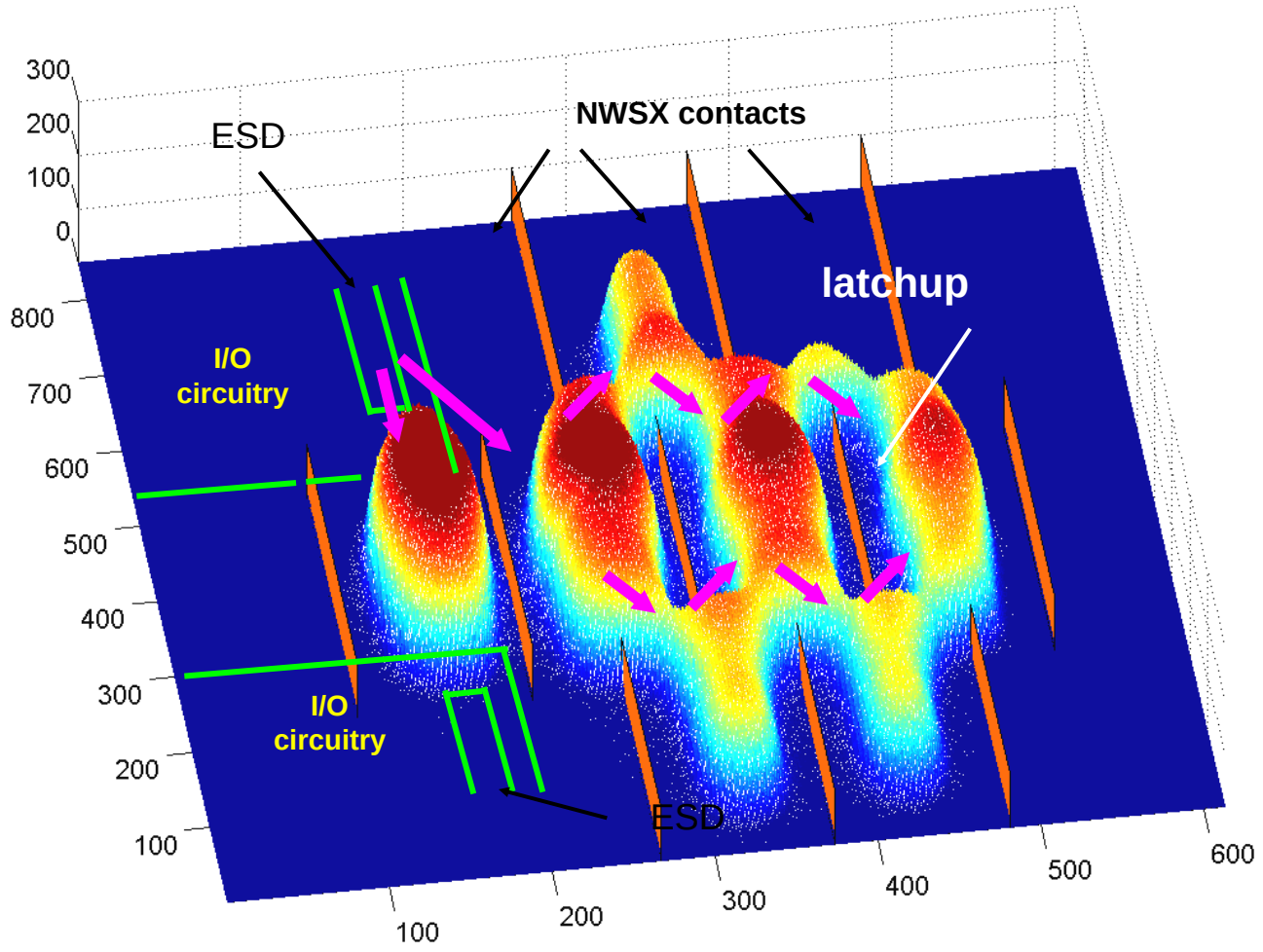
Photo-emission Studies



Stellari ITSFA 2003

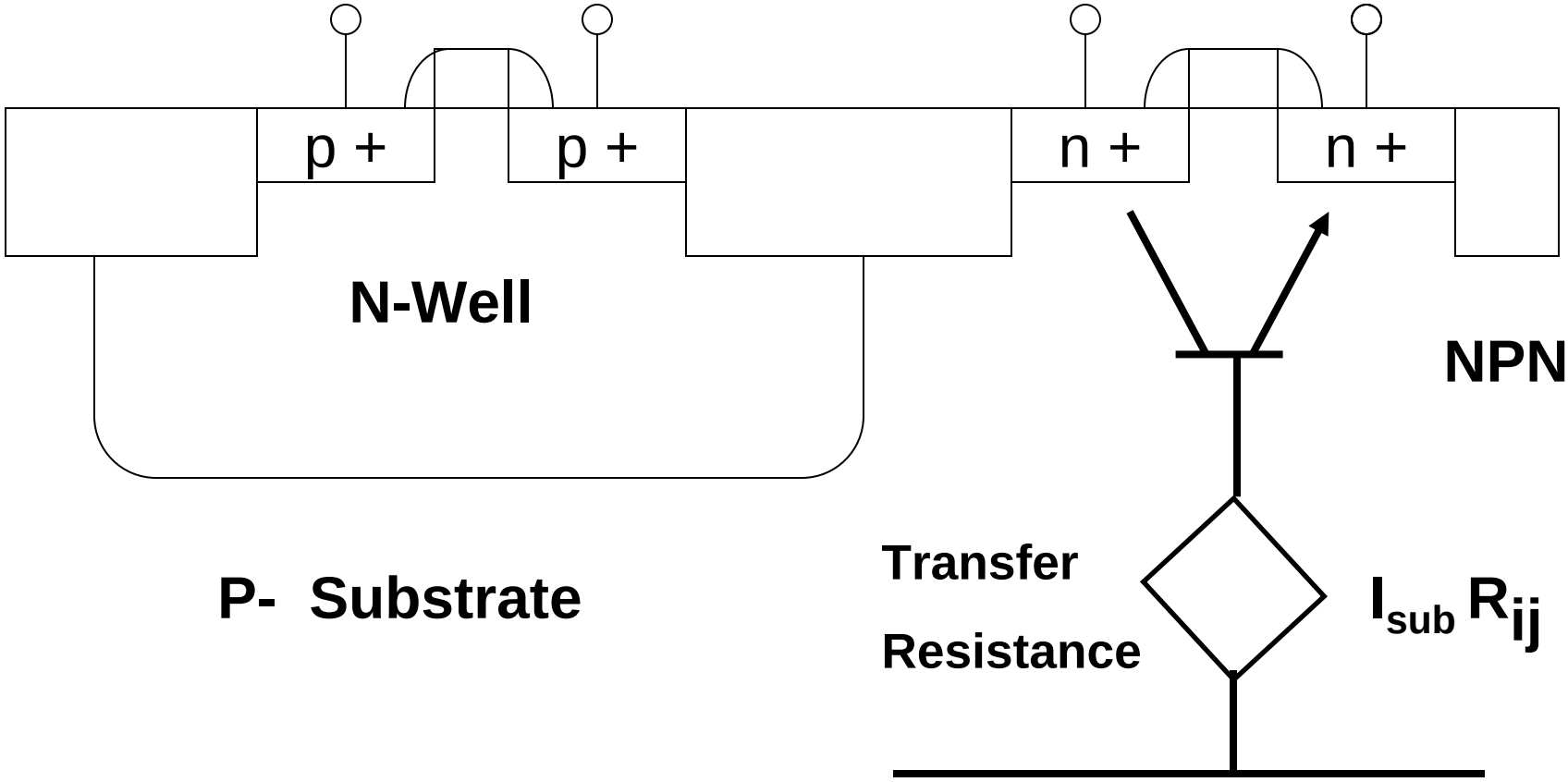
***Latchup* 2007**

Photon Emissions



F. Stellari ISTFA 2003

Transfer Resistance



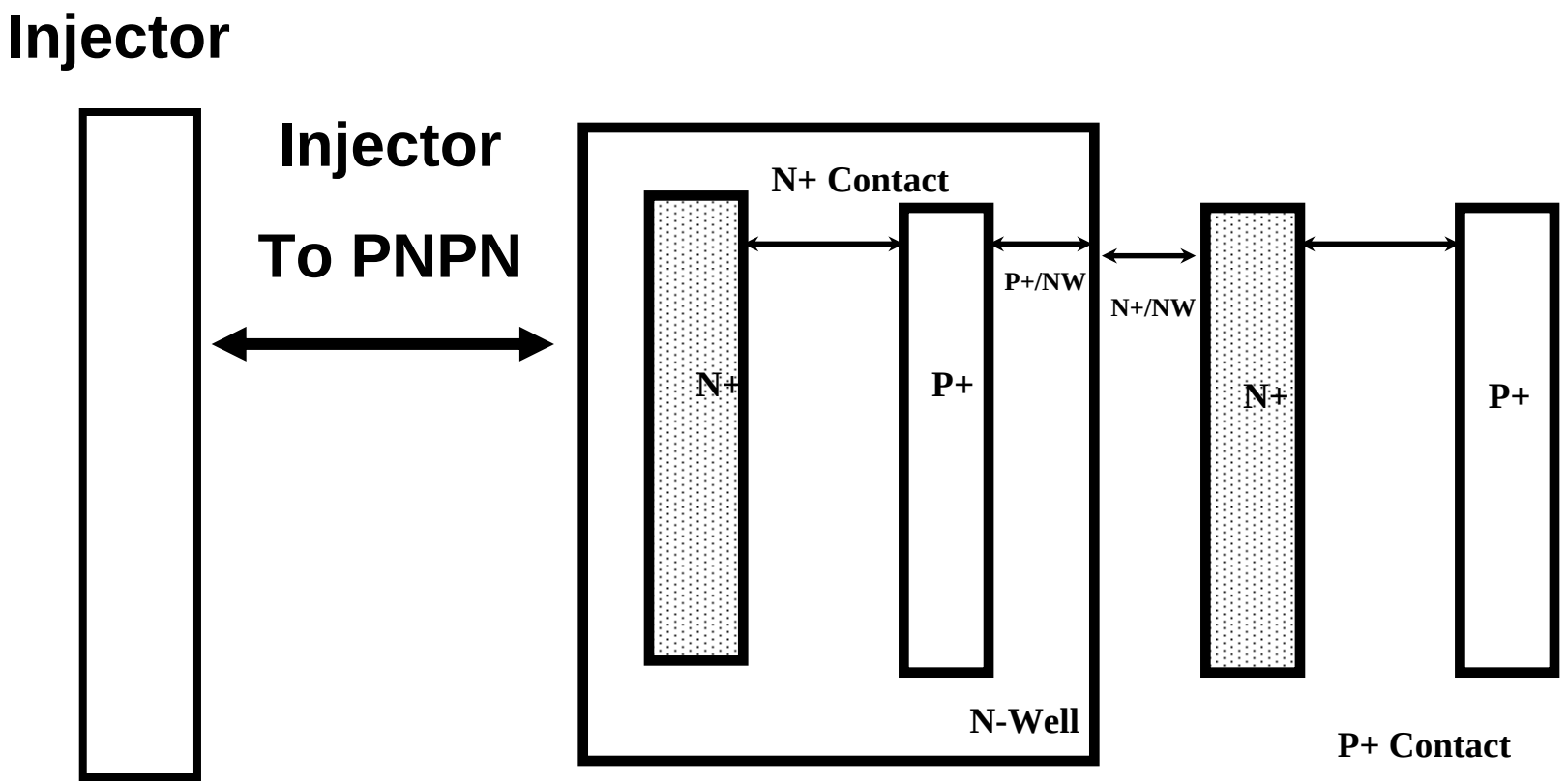
Troutman 1985

Latchup 2007

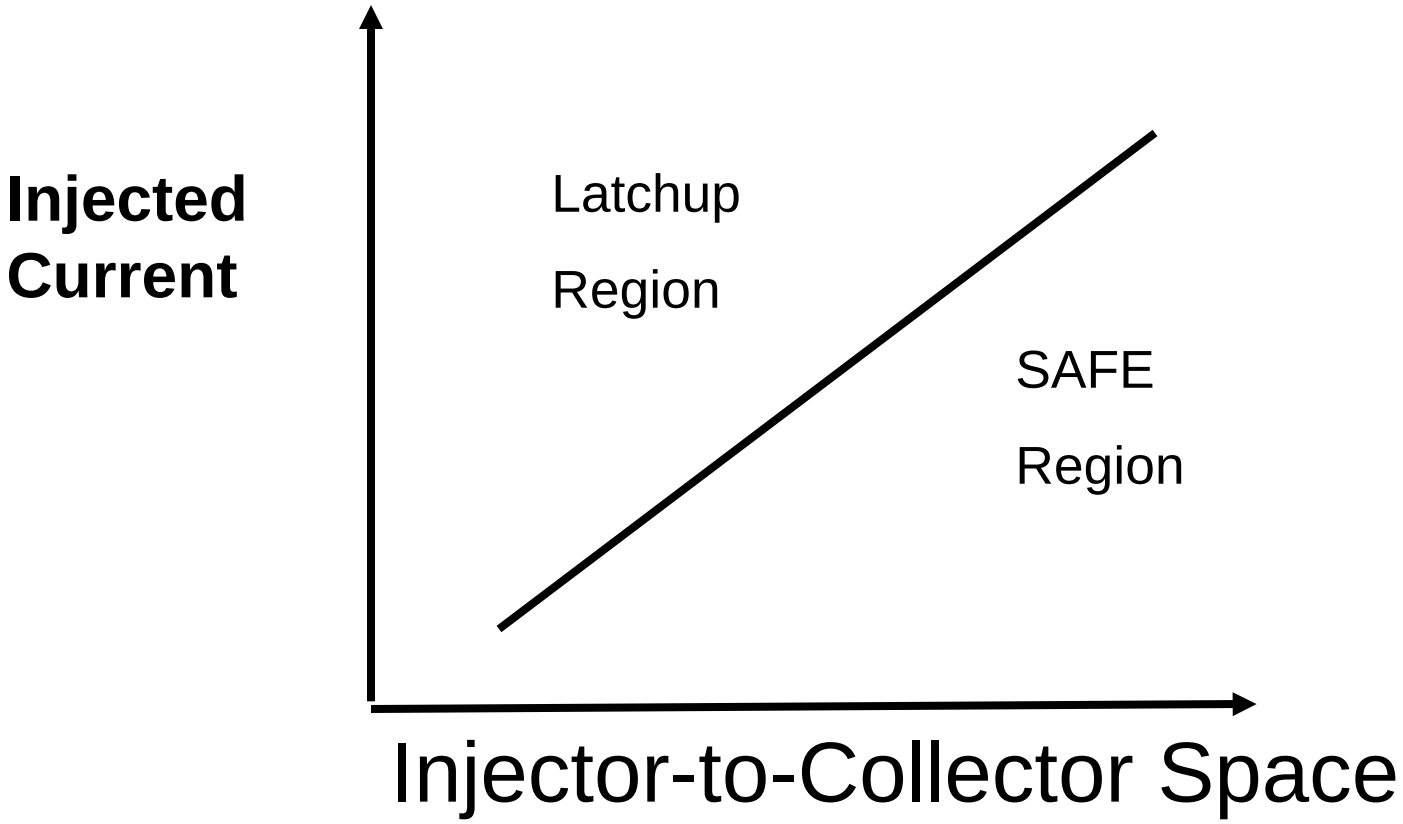
CAD – Placement

- Optimization of Latchup contacts with chip optimization using Cost functional algorithms
- Optimization of well and contact spacing based on injector-to-circuit spacing

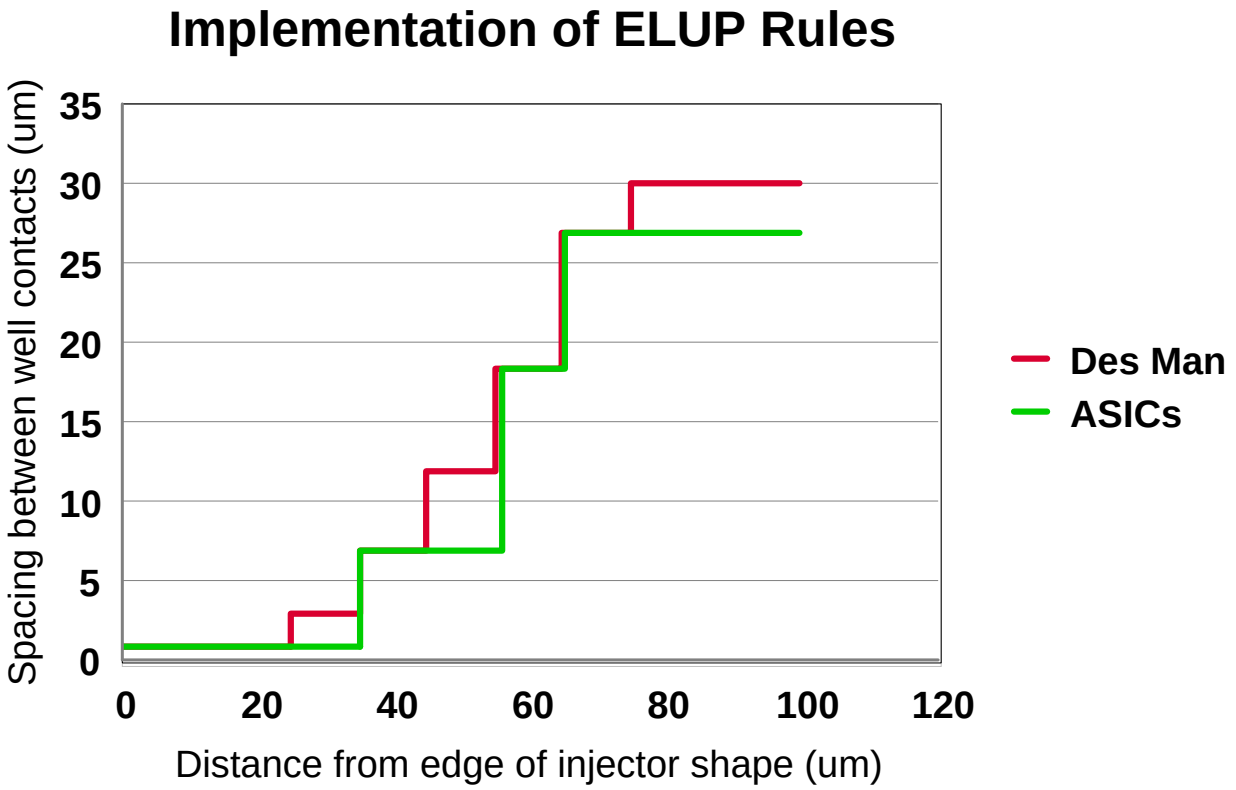
Latchup Ground Rules



External Latchup – SAFE Region



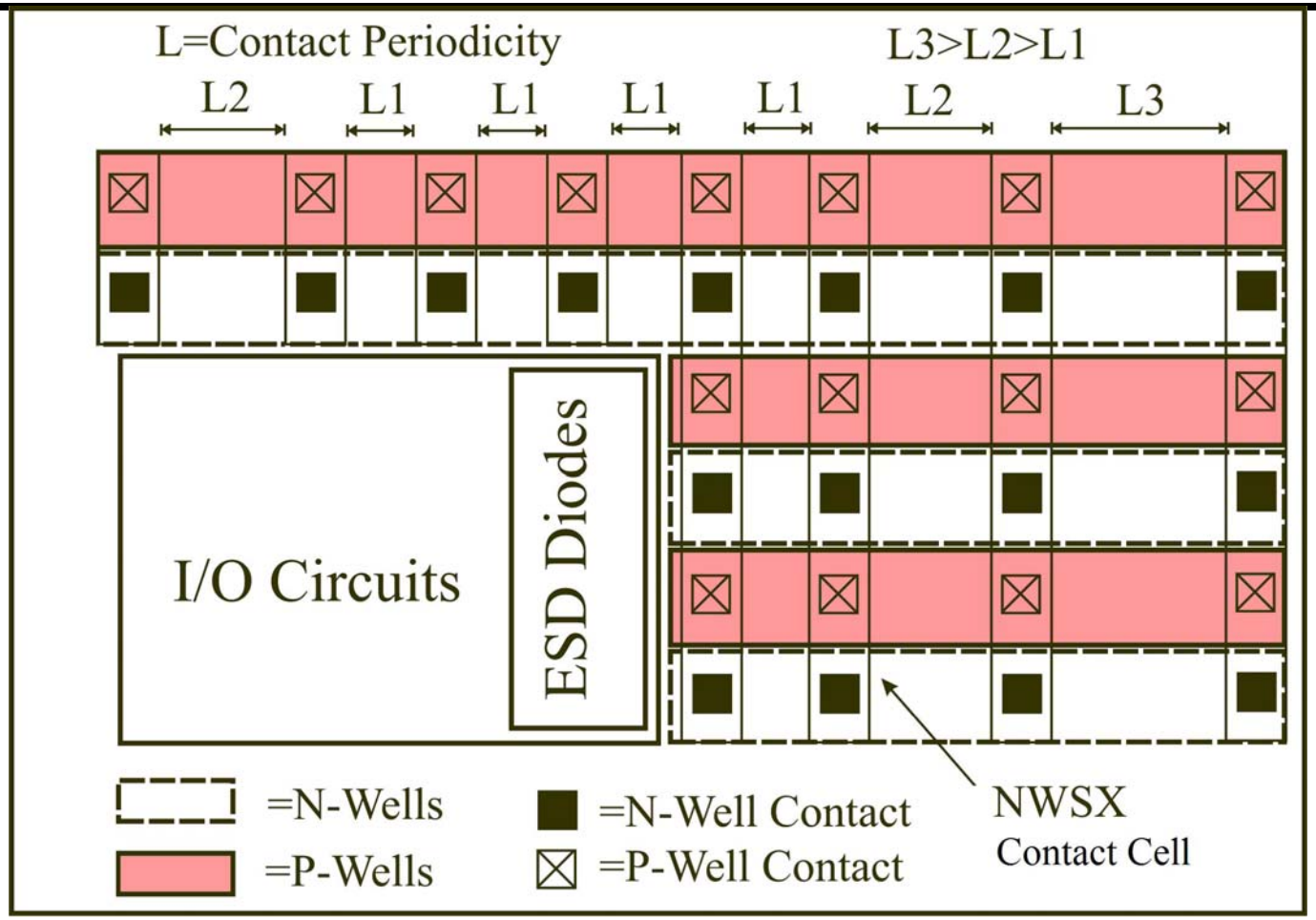
External Latchup Design Rules



Brennan EOS/ESD 2004

***Latchup* 2007**

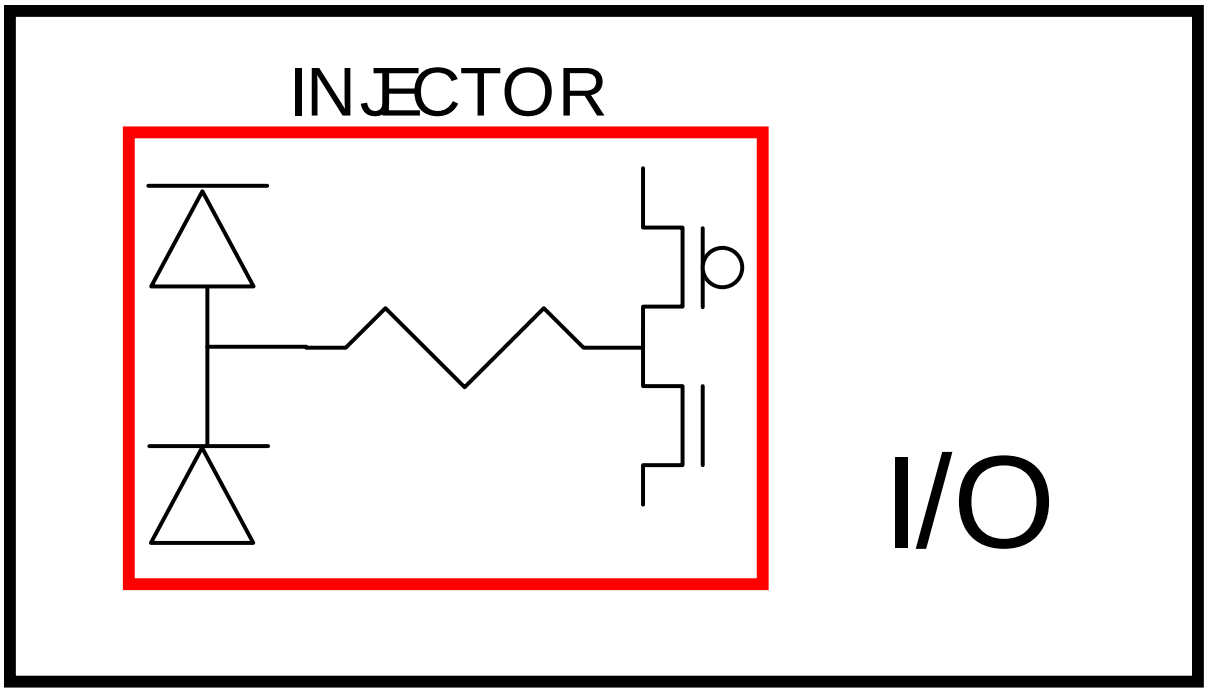
ASIC Array I/O



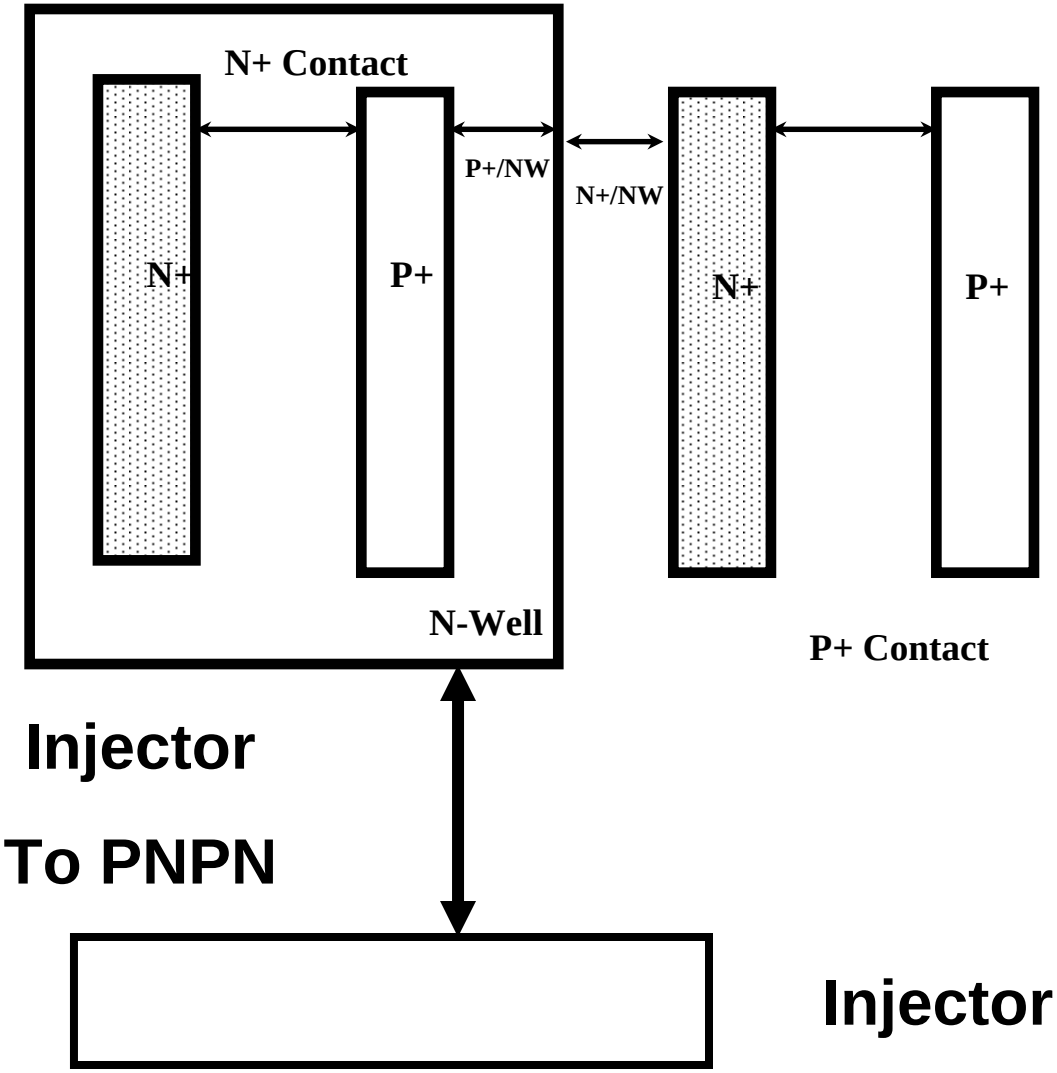
***Latchup* 2007**

Brennan EOS/ESD 2004

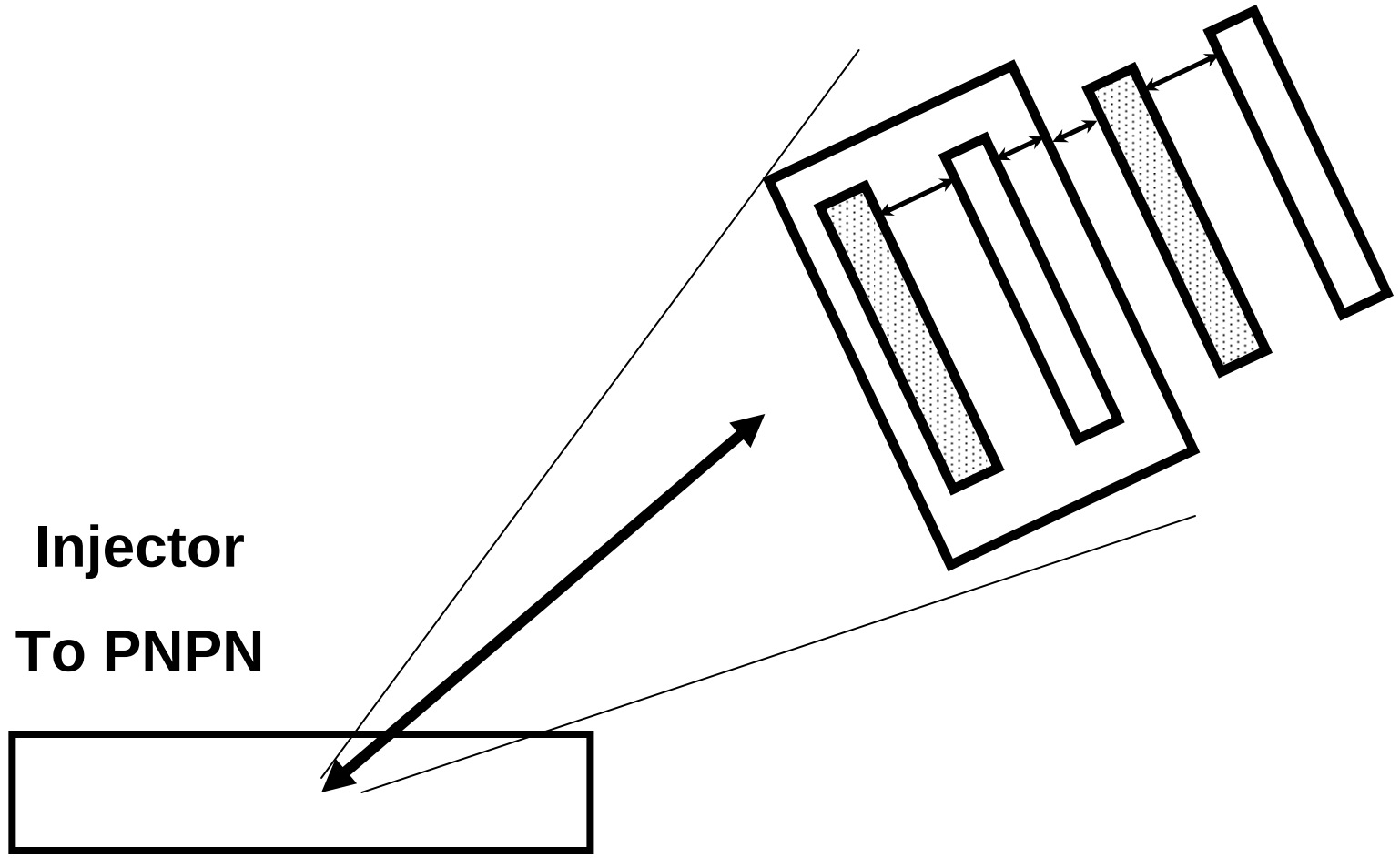
Injector Dummy Design Levels



Latchup Ground Rules - Orientation



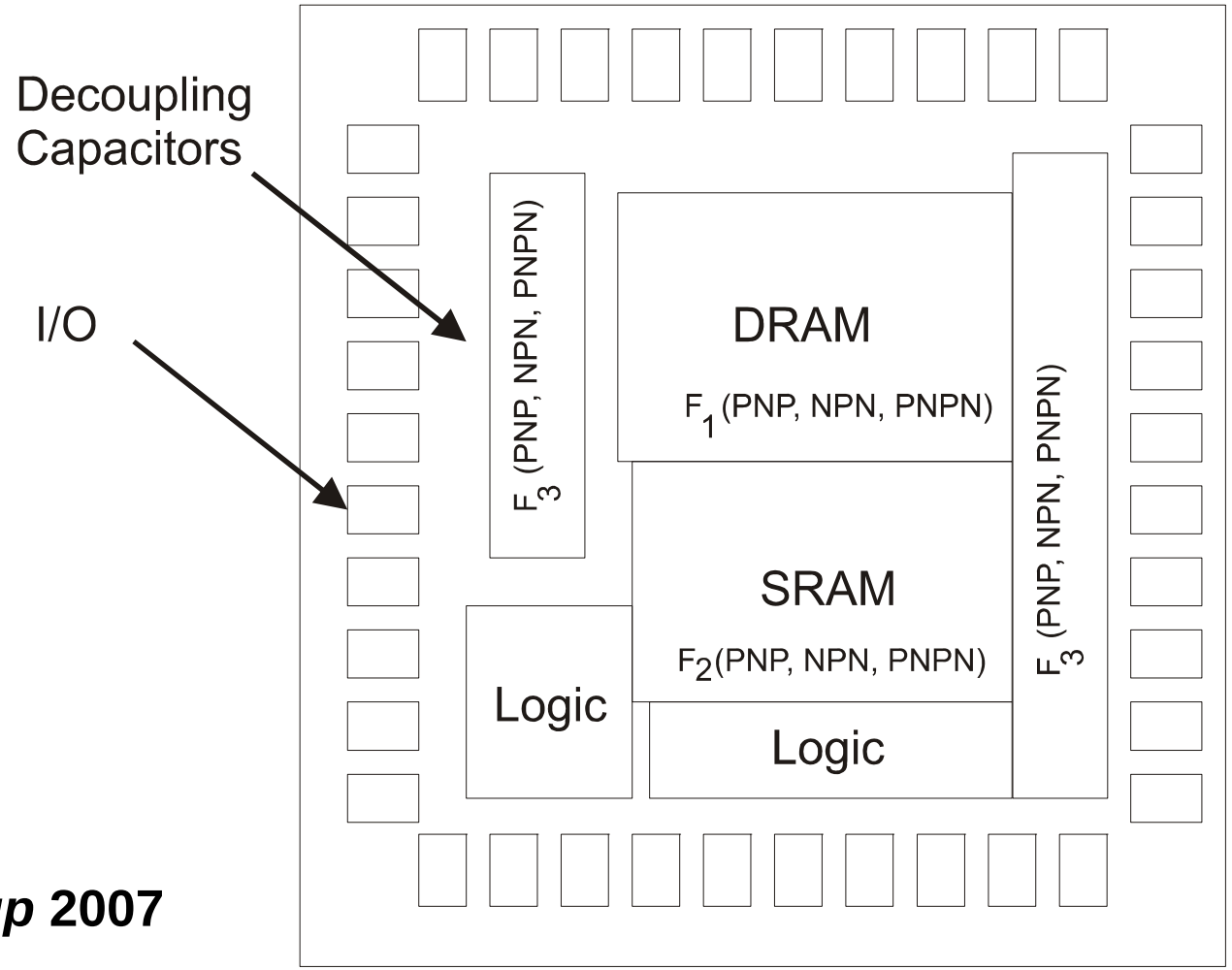
Latchup Ground Rules - Orientation



CAD – Global Placement

- Global placement based on PNPN density and circuit
- Latchup sub-function “boundary” evaluation methodology

Global Floor planning



CMOS Latch-up

- CMOS Concern increasing with technology scaling and Integration
- Solutions include
  - Test and Characterization
  - Circuit solutions
  - Design Synthesis and Integration
  - CAD tools for verification and checking
  - Circuit methodologies