THE NUMBER ONE SOURCE FOR HIGH PERFORMANCE ANALOG

Designing Electrical Overstress Robust Integrated Circuits

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HIGH PERFORMANCE ANALOG

Objective

- Introduce the concept of electrical overstress (EOS) showing why we in the semiconductor industry need to be concerned with it, how it occurs, and how parts can be designed more robust to its damaging effects

Outline

- The Design Process
- EOS Overview – Know your enemy
- EOS Sources
- Debugging EOS Damage
- Concluding Remarks

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The Design Process

The Design Process – Circuit Design

- Marketing Identifies a need in the market
- A set of features and objective specifications developed
  - Datasheet; Customer Drawing; etc.
- Suitable process/design group selected
  - Pick a technology (wafer and packaging)
- Cost estimates made to see if profitable
- Product designed (key circuit blocks)
  - Schematic capture and simulation to meet specs
- Circuit implemented in silicon and packaged
  - Layout, packing to smallest die size, placement for package
- Test and qualify product
  - Build material and stress it (HTOL, Temp Cycle, Storage, etc.)
- Release

The Design Process – EOS Robust

- Marketing Identifies a need in the market
- A set of features and objective specifications developed
  - What environment must this part survive?
  - Can we specify its EOS exposure risks?
  - Where do we draw the line (what risks are acceptable)?
- Suitable process/design group selected
  - Pick a technology (wafer and packaging) based on its EOS exposure
  - Do I need higher breakdowns? Special Structure for EOS?
  - Supply external components? Co-package EOS protection with a die?
- Cost estimates made to see if profitable
- Product designed (key circuit blocks)
  - Schematic capture and simulation to meet specs
  - Develop special EOS robust element in selected process
- Circuit implemented in silicon and packaged
  - Layout, packing to smallest die size, placement for package
- Test and qualify product
  - Build material and stress it (HTOL, Temp Cycle, Storage, etc.)
  - How do I quantify the EOS robustness?
- Release

Basic EOS Events

- All Circuits must meet these
- Electrostatic Discharge
  - Human Body Model (HBM, JEDEC JESD22-A114D)
    - 2000v ~ 1.3 amps peak current; 750ns duration
  - Machine Model (MM, JEDEC JESD22-A115-A)
    - 200v ~ 3.2 amps peak current; decaying sine wave
  - Charge Device Model (CDM, JEDEC JESD22-C101C)
    - 1000v ~11.5 amps peak current; 2-3ns duration
- Latchup Testing (JEDEC JESD78A)
  - 1.5x supply voltage (i.e. 5v supply stress at 7.5v)
  - 100mA current pulse into and out of each pin
  - Up to 1 second duration

Other EOS Environments

- Communications
  - Subject to Power surges on power lines
  - Lightning hits power or signal lines
  - Fault condition induces voltage spike
- Electrostatic Discharge
  - Cable discharge
  - High Level ESD (15KV)
- Battery Operated Electronics
  - Batter reverse insertion
- Automobile Industry
  - DC power provided by battery/charging system
  - Fault could induce voltage/current spikes in electrical system
- Careless consumer or technician
  - Uses wrong power adapter (12v instead of 5v)
  - Accidentally drops conductive material shorting two nodes together
  - Installs wrong component (driver-driver instead of driver-receiver)

EOS Environments

- Numerous ways parts can be damaged by EOS
- Cost prohibitive to protect against all forms of EOS
- Keys to EOS Robust Designs
  - Know the EOS environment
  - Identify major threats
  - Protect against these threats

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EOS Overview

ESD Overview – Know your enemy!

- Electrical Overstress Definition
  - Any electrical stimulus (voltage or current) that exceeds a part's rated operating conditions
  - Very broad category of stress
    - Nanoseconds to milliseconds (sometimes days) in duration
    - pJ to KJ in energy
  - Failure modes are dependent on the magnitude and duration of the stress; Voltage developed can initiate current paths that cause failure
- Operating Conditions
  - Defined on the datasheet
  - Absolute Maximum Ratings list upper range of voltages/currents allowed

EOS Overview – Know your enemy

- Datasheet Example

Absolute Maximum Ratings

Absolute Maximum Ratings

V_{CC} to Ground 7V
Input Voltages
DI, DE, RE . . . . . -0.5V to +7V
Input/Output Voltages
A/Y, B/Z . . . . . -8V to +12.5V
RO . . . . . -0.5V to (V_{CC} +0.5V)
Short Circuit Duration
Y, Z . . . . . Continuous

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
8 Ld SOIC Package	170
Maximum Junction Temperature (Plastic Package)	150°C
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) (Lead Tips Only)	300°C

Operating Conditions

Temperature Range
ISL43485I . . . . . -40°C to 85°C

Normal Conditions

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

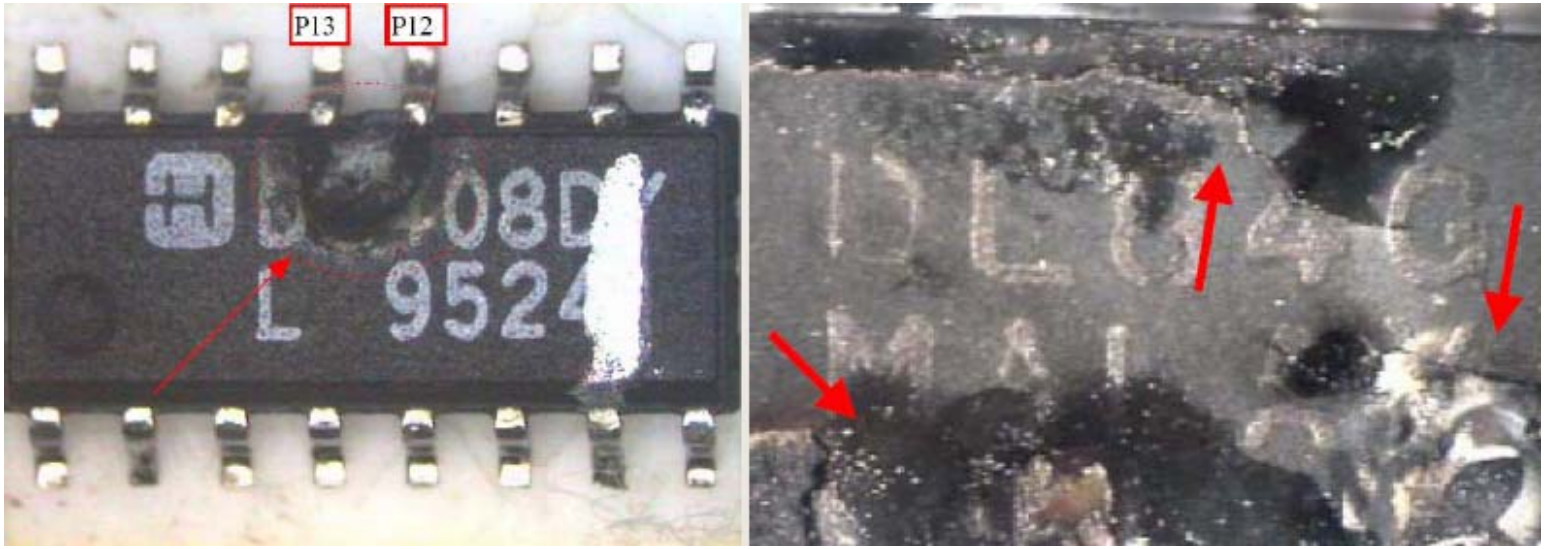
Electrical Specifications Test Conditions: V_{CC} = 3V to 3.6V; Unless Otherwise Specified. Typicals are at V_{CC} = 3.3V, T_A = 25°C, Note 2

EOS Overview – Know your enemy

- Types of EOS Damage
  - Melted Package
  - Blown or fused bond wire
  - Fused/melted interconnect
  - Shorted transistor
  - Open Resistor

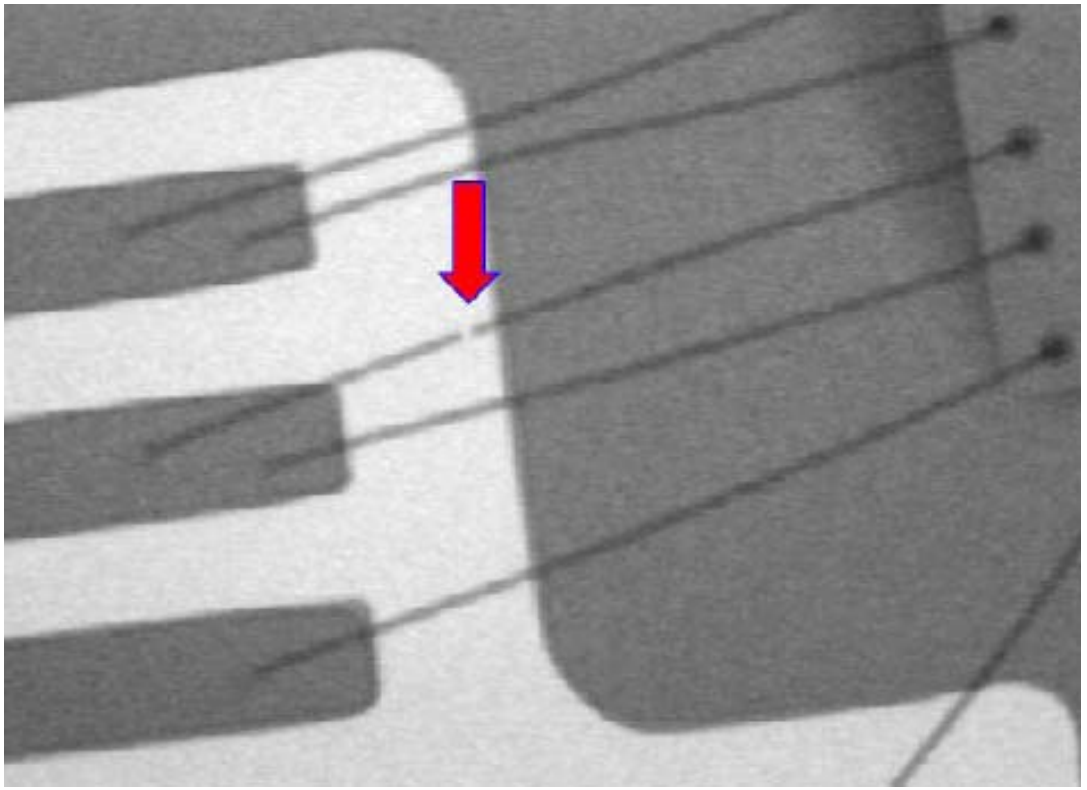
EOS Overview – Know your enemy

- Extreme EOS – Melted package
  - Temperature exceeded 200°C



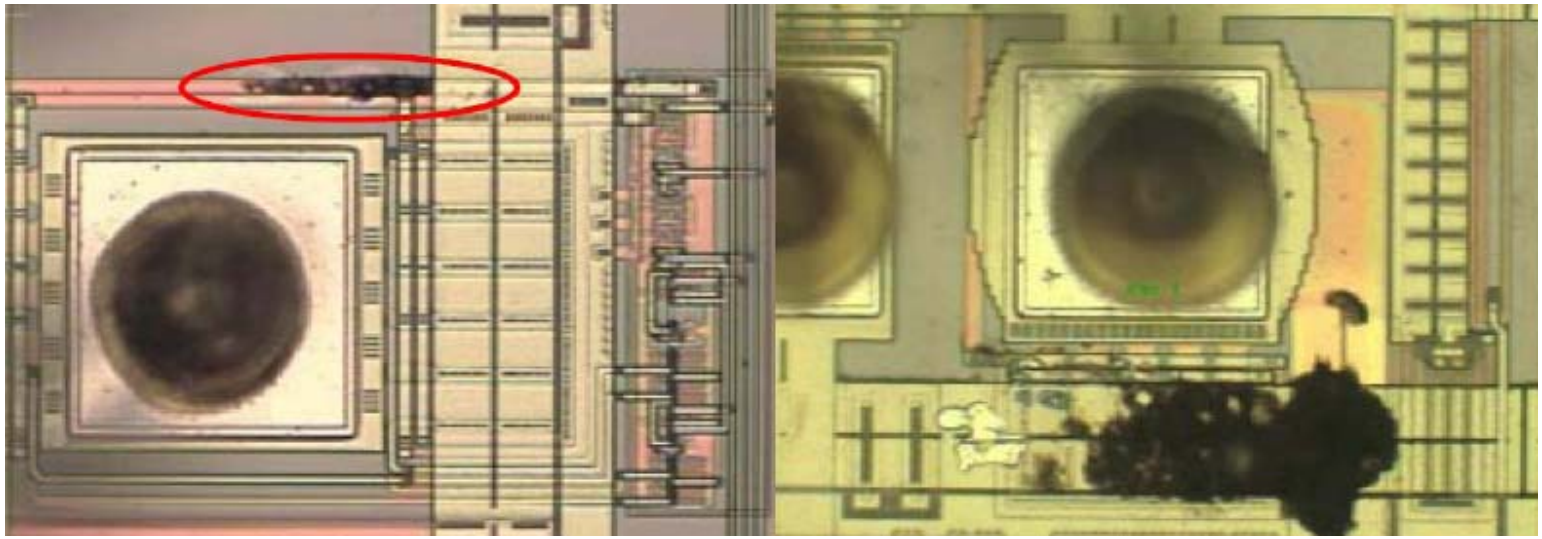
EOS Overview – Know you enemy

- Blown Bond Wire
  - Takes about 1 to 1.5 amps of current and a few ms to seconds
  - Gold wire melts at about 1060°C; Aluminum wire at about 660°C



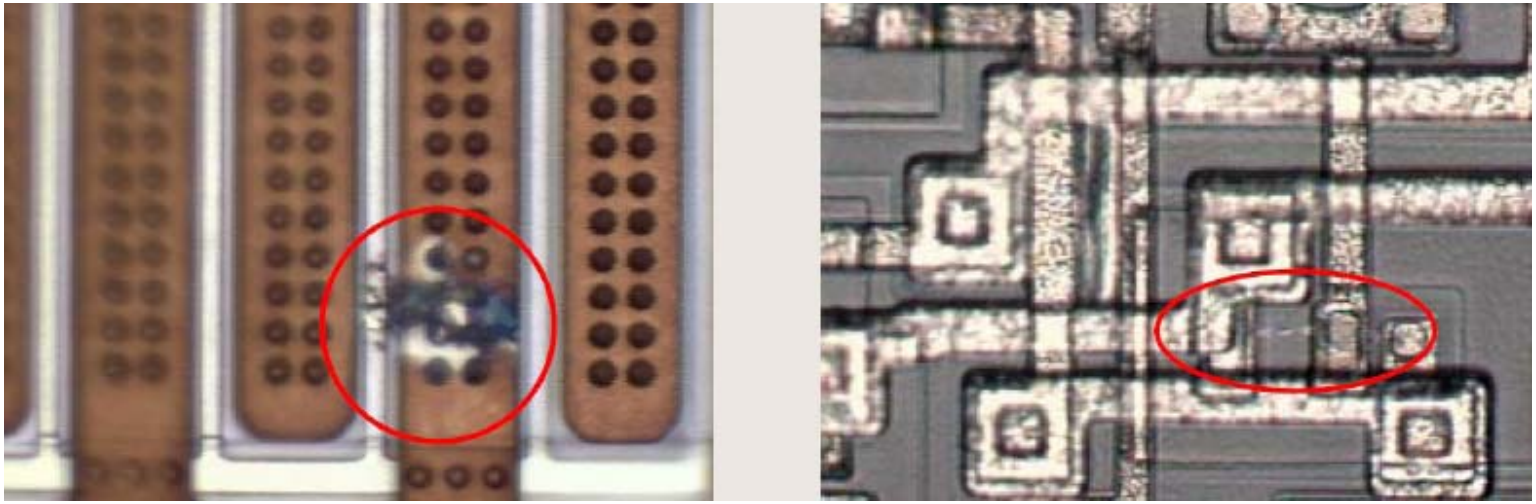
EOS Overview – know your enemy

- On chip metallization damage
  - Aluminum metal melts at ~660°C



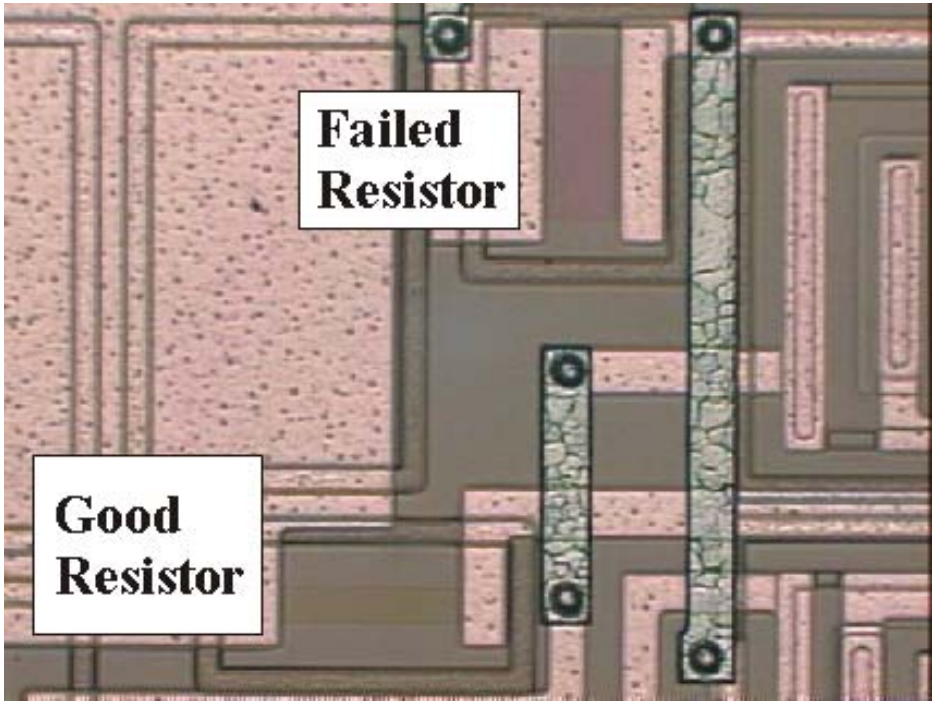
EOS Overview – Know your enemy

- Transistor Damage
  - The amount of damage is related to the pulse magnitude and its duration; larger and longer produce more damage
  - Silicon melts at ~1400°C



EOS Overview – Know your enemy

- Some damage can be very difficult to see
- Only difference between these two thin film resistors is a color difference
- The failed resistor is electrically open



EOS Overview – Know your enemy

- Why is EOS important?
  - Safety
    - EOS damage to a part can start a fire
    - Heat generated can cause burns
    - Collateral damage to surrounding equipment
  - Cost
    - EOS is the largest cause of failure (~25-50% of all failures)
    - Loss of customer confidence in your products
    - Loss of customer business

EOS Overview – Know your enemy

- How Does EOS Occur?
  - Nature/Environmental
    - Lightning
    - Power Distribution
    - Machines, Relays, and Coils (inductive elements)
  - Accident or Component Failure
    - Plug a part in wrong
    - Use wrong power adapter
    - Place a conductive object across power bus
    - Voltage regular fails (5v goes to 20v)
    - HV element fails shorting two power domains

EOS Overview – Know your enemy

- How Does EOS Occur?
  - Design Issues
    - Process doesn't match application
      - Voltage ratings too low
    - Layout of circuit board too inductive/resistive
      - Switching current produce high voltage transients
    - Layout of chip creates parasitic transistor/SCR
      - Latchup threat; noise triggers parasitic element into failure
    - Floating nodes in CMOS; Large shoot through current
    - Select wrong ESD Protection for application;
      - sensitive to false triggers while power applied
    - Violations in Safe Operating Area for power elements
      - *Current Density, J, and/or di/dt* ratings
      - Power ratings
      - Voltage ratings

EOS Overview – Know your enemy

- What causes Failure?
  - Thermally Induced Damage ← Primary End Result
    - Melted Junctions
    - Metal Lines
    - Bond Wires
    - Packages
  - Electric Field Induced ←Creates an undesired path
    - Dielectric breakdown
    - Device Breakdown

EOS Overview – Know your enemy

- EOS Failure Models
  - Wunsch and Bell, “Determination of threshold failure levels of semiconductor diodes and transistors due to pulse power voltages,” *IEEE Trans. Nuclear Science*, vol. 15, pp. 244 – 259, 1968.
  - Dwyer, Franklin, Campbell, “Thermal failure in semiconductor devices,” Solid State electronics, vol. 33, pp. 553 – 560, May 1990.
- Failure threshold related to duration of the EOS event
  - Shorter events require higher power to produce failures
- Minimum power that will cause damage
  - Below this threshold no damage is seen

EOS Sources

EOS Sources

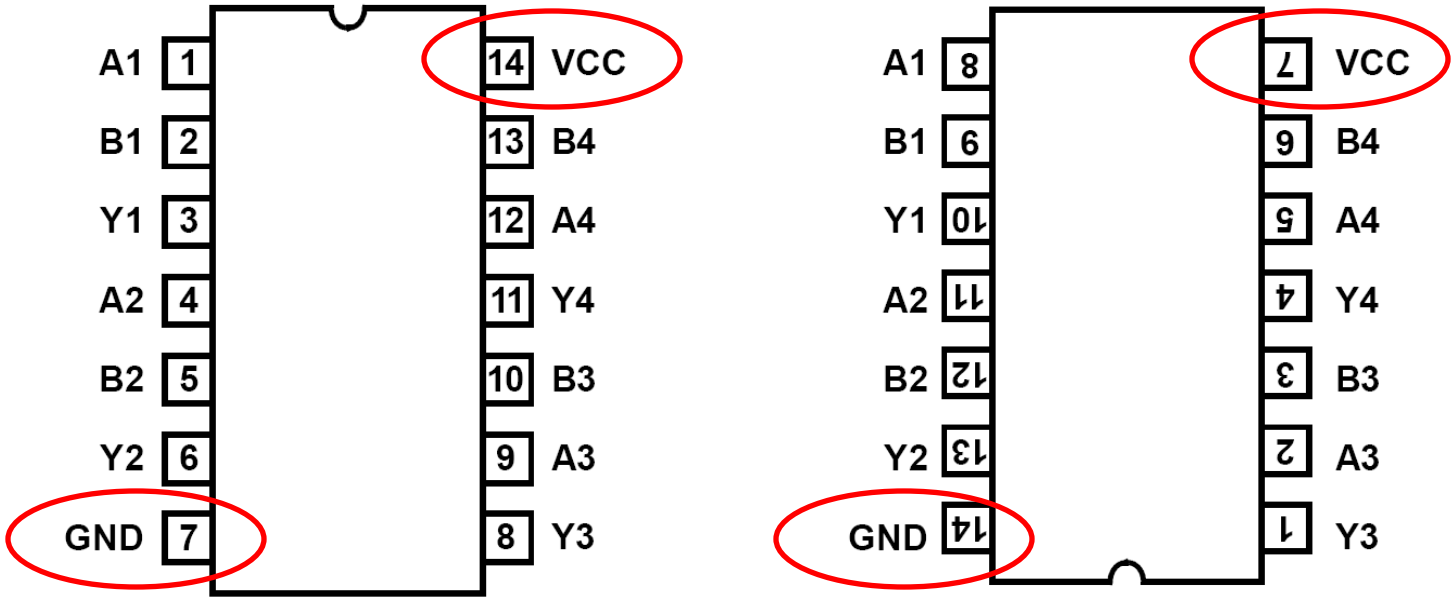
- Nature/Environment
  - Lightning
    - Florida is the known as the lightning capital of the world
    - Lightning Tracker @ http://www.flamedia.com/
    - Most electronics will not have to withstand a direct strike
      - MOV – Metal oxide varistor
      - TVS – Transient Voltage Suppressor
      - http://www.littelfuse.com/ (sold our TVS line)
    - These elements take the first part of the strike but may pass some energy to the board assembly or integrated circuit
    - Local protection at the board may be needed
    - Need to determine what gets to the IC and design for this
  - IEC 61000-4-4 – Electrical fast transient/burst immunity test
    - Repetitive electrical fast transients
  - IEC 61000-4-5 – Surge immunity test
    - Unidirectional surges caused by over voltages from switching an lightning transients

EOS Sources

- Nature/Environment
  - Power surges
    - Motors, relays, and other inductive loads create voltage transients that are felt on the power bus
    - Common example is turning on a vacuum cleaner while listen to the radio. A lot of noise is generated in the power line and radiated from the motor
    - A/C turns on and the lights dim/flicker
    - Newer electronics have filters built into the power support to suppress this noise but if the magnitude is high enough it could trigger undesirable current paths
  - Power Grid Failure/Fault
    - Transformer failure sends a surge into your house
    - Tree falls on power lines shorting out multiple phases

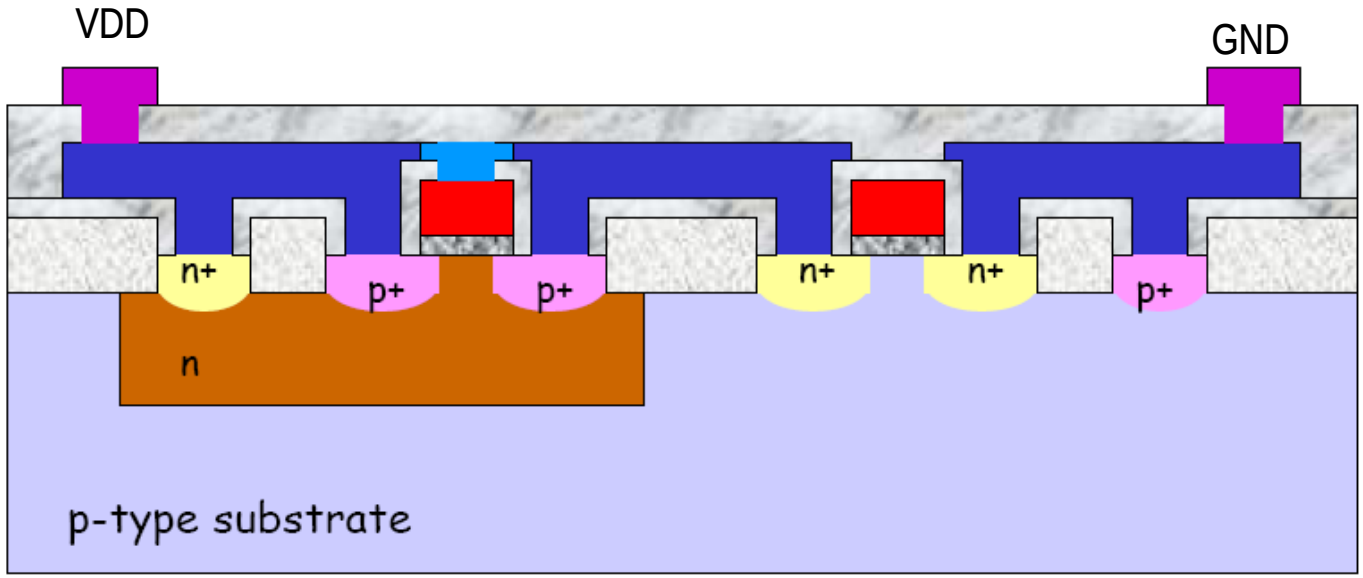
EOS Sources

- Accident or Component Failure
  - Reverse Insertion of a component
    - Small size components can make it difficult to see pin 1
    - Non-automated testing may place a part in the socket rotated
    - Swapping Power and Ground forward biases isolation diodes



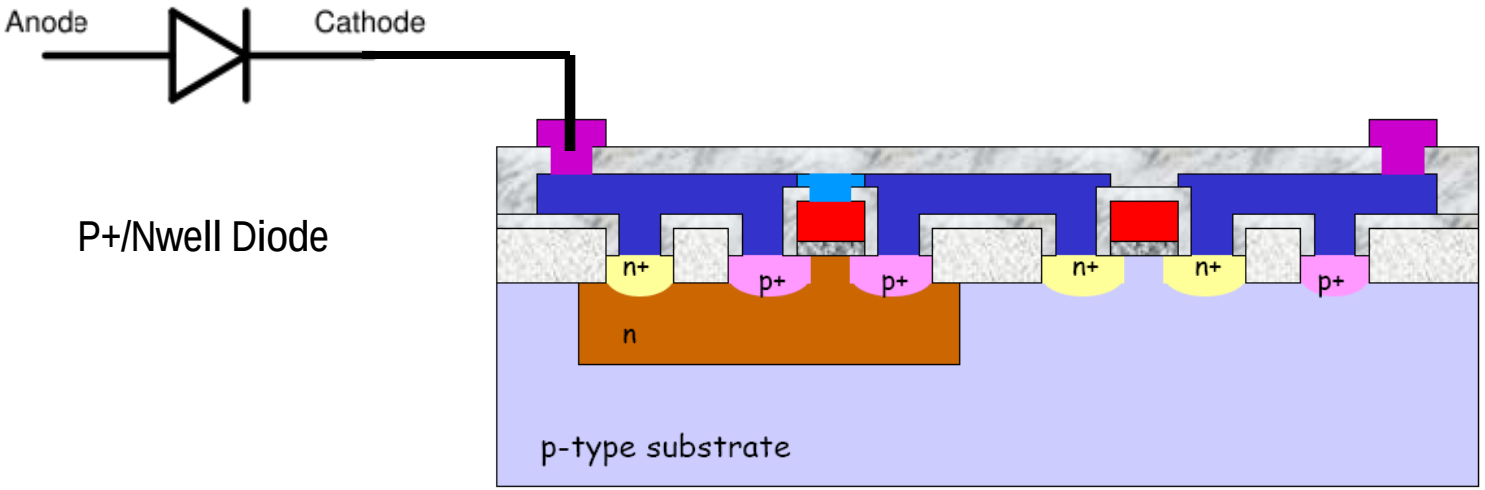
EOS Sources

- PMOS transistors are formed in an NWELL
  - Body tie of PMOS is VDD
- NMOS transistor are formed in the P Sub
  - Body tie of NMOS is GND
- IF the VDD and GND connection are reversed a forward biased diode would exist between Psub and NWELL
- Current is limited by well/sub resistance and external connection
  - Amps of current will flow
  - Typical failure is a bond wire fused open



EOS Sources

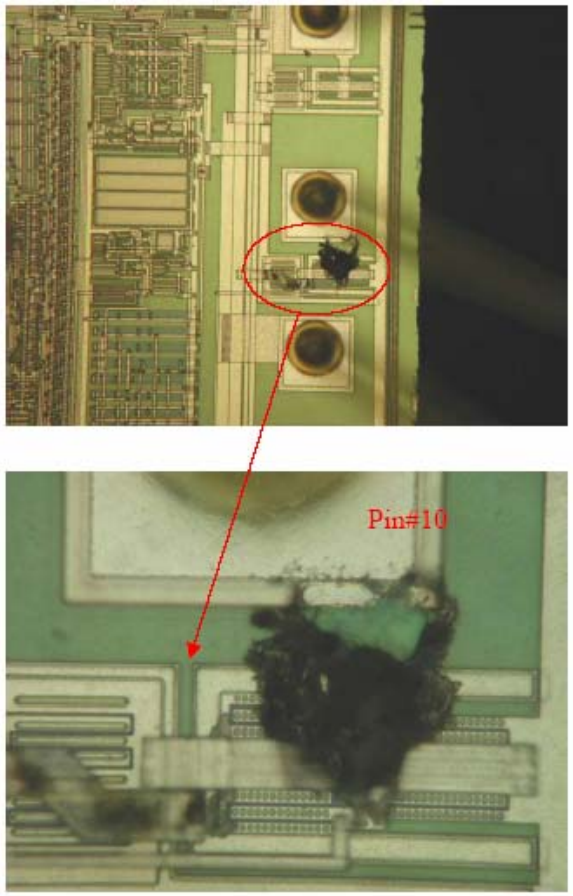
- Reverse Battery Protection
  - Could provide protection with a simple diode or PMOS (gate ground)
  - Problem is all current for chip comes through single element
    - single source of failure
  - Element size needs to accommodate the supply current
  - Creates a voltage drop (0.6v for diode; PMOS less depending on size) on the supply line
  - ESD needs to be addressed (blocking junction for reverse strike)

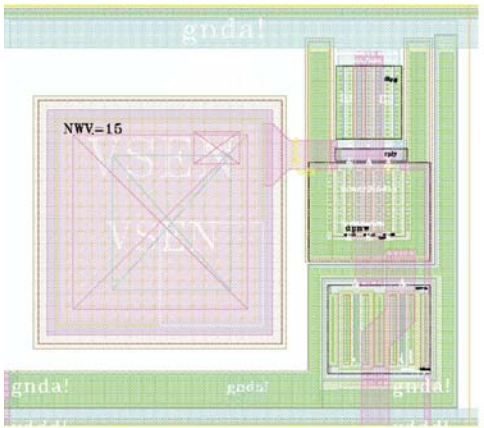


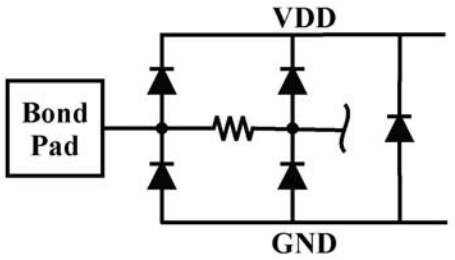
EOS Sources

- Design/Layout Issues
  - Many of the correctable issues originate here
  - Causes can be traced to each level of the product
    - IC layout issues (feedback pin on PWM)
      - Improper design of input structure
      - ESD protection minimal; Metal connection too small
      - Failure caused by EOS of metal during an over voltage event
    - Printed Circuit Board layout and component selection
      - Noise generated on PCB triggers ESD Protection (inductive spikes)
      - Noise exceeds Absolute Maximum Ratings of part (triggers ESD elements)
      - Customer does not want to change board
      - Competitor does not blow up so you are designed out if not fixed
    - Understand the Safe Operating Area (SOA)
      - Know your application
        - » In-rush current; Voltage ratings; Power ratings
      - SOA defines your voltage, current, and power ratings for the device
      - Defined based on DC or pulsed duty cycle
      - Exceed these limits and the device could fail

EOS Sources



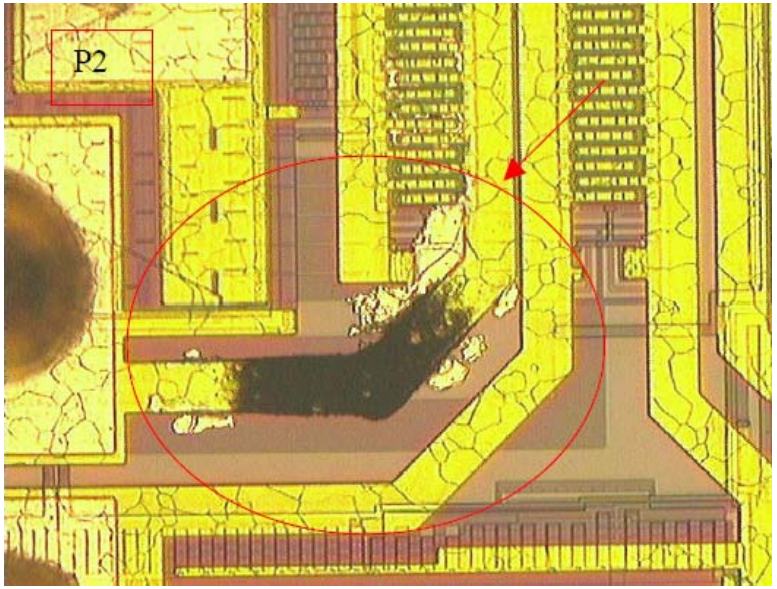




- Failure caused by narrow metal connecting pad to input protection diodes and relatively small ESD protection (~1500 volt HBM)
- Metal fused open

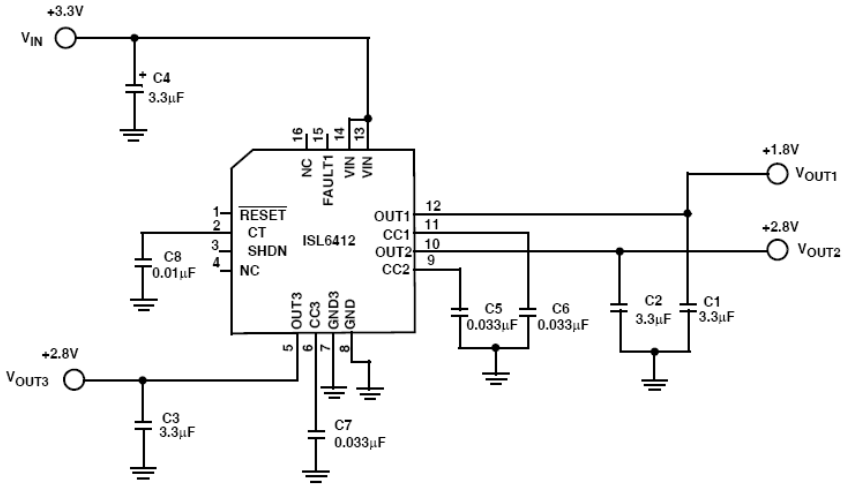
EOS Sources

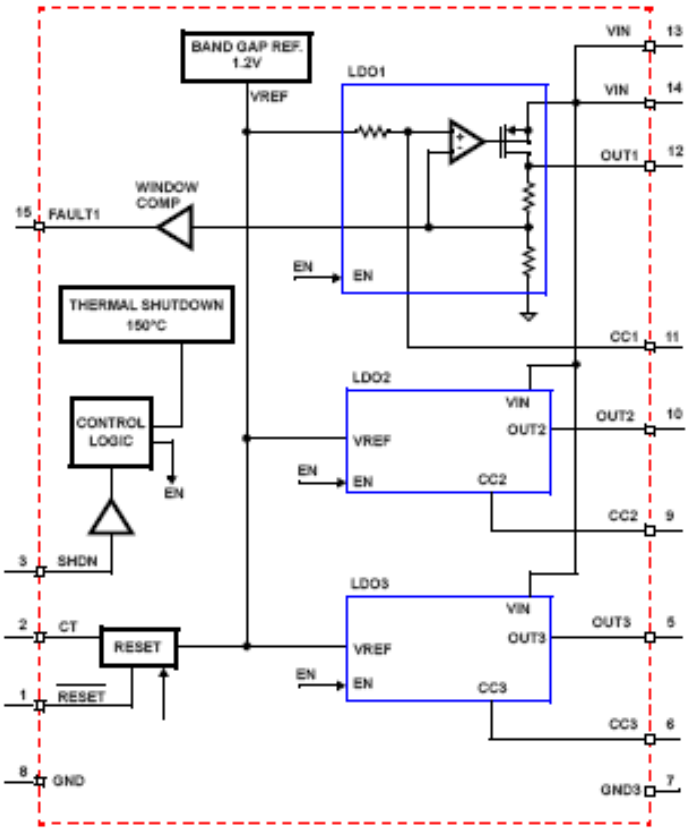
- Two ESD clamps shown in photo
- Metal connecting one clamp is fused
- Clamp triggered while power applied to the device
- Fix by controlling the board layout and noise generation
- Ultimately we need to be careful what clamps are used on noisy pins so they are robust to the noise expected



EOS Sources

- Linear Regulator
- If output capacitor too large during power up a large surge current felt on the output to charge the capacitor
- If this current exceeds the PMOS SOA it could be damaged
- Proper component selection is important; follow recommendations





Debugging EOS

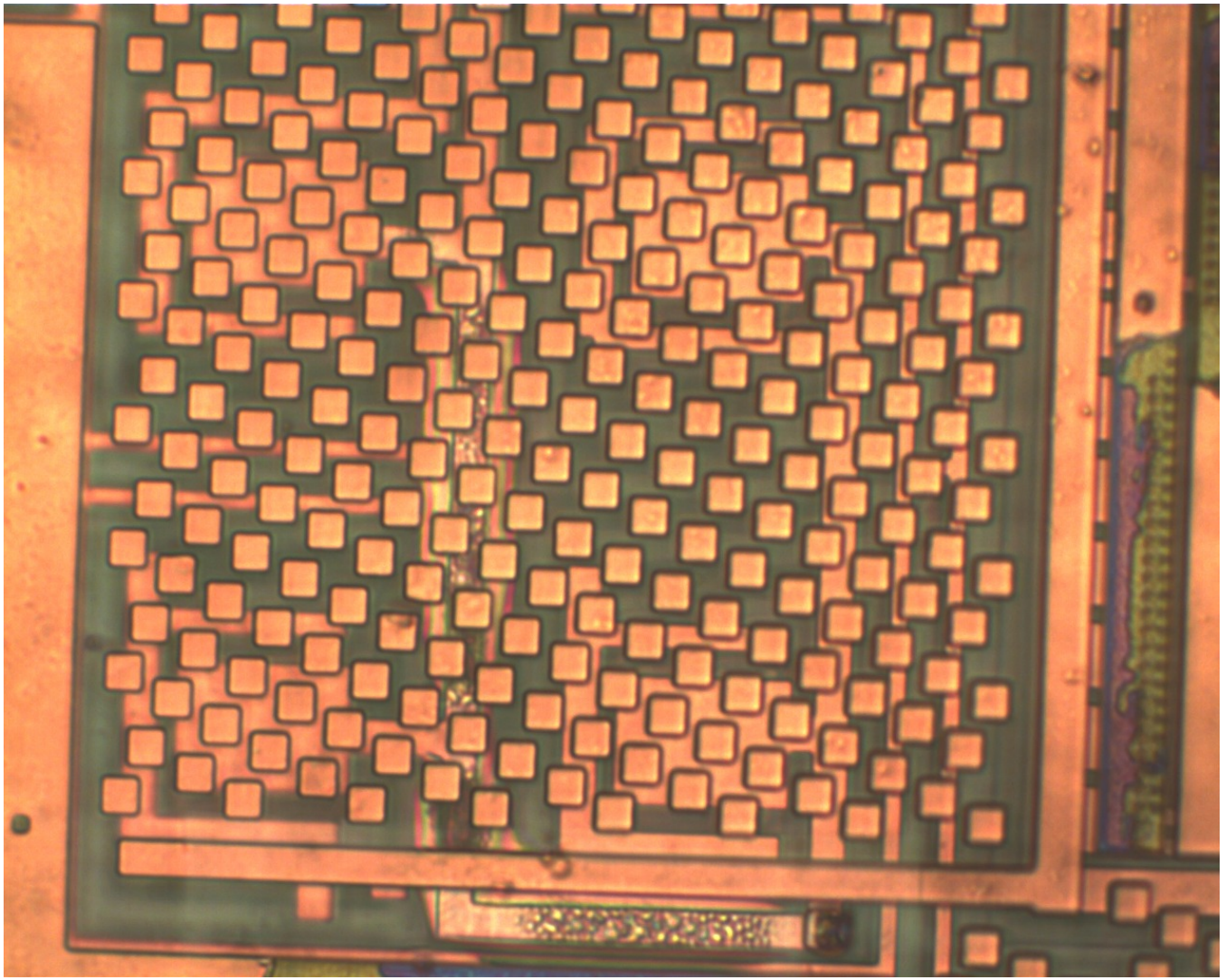
Debugging EOS Damage

- Reference:
  - Vinson, “The Search for the Elusive EOS Monster,” International Symposium for Testing and Failure Analysis, 1998.
  - http://www.tmworld.com/article/CA254574.html
- Paradigm shift in thinking required for EOS
  - EOS is an event that occurs at a point in time
  - It is probabilistic in nature
  - May require a unique set of circumstances
  - May not be reproducible without a lot of testing
  - Finding the damage on a die is easy; Finding the cause is difficult and resource (time, equipment, and units) consuming
  - Must weigh the cost/benefit before starting the “Hunt”

Debugging EOS Damage

- Steps in the Monster Hunt
  - Failure Analysis
    - Electrical Data
      - What caused the failure?: Short/Open/Leakage
      - Review ATE data and take Bench Data
    - Failure Site Identification
      - Sometimes it is easy but mild EOS may be buried
      - Use normal FA techniques to pin point the failure
    - Visual Evidence (look for patterns of damage)
      - Investigate the path
      - Determine what might have failed
        - » Breakdown Paths
        - » Look at the current path
    - Estimate Failure Cause
      - Type of event (over voltage or over current)
      - Path (pin combination
      - Size of the event (magnitude and duration)

Debugging EOS Damage



Debugging EOS Damage

- Determine the Source (Monster Hunt)
  - This area can take most of the time
  - Identification of the two failures in the paper took 6 months
  - Know your Enemy (Voltage or Current failure)
    - FA gives you clues about how the EOS occurred
    - Testing good units can help identify weaknesses in circuit
  - Gather Intelligence (failure source)
    - Investigative Reporter or CSI searching for clues
    - Try to recreate the circumstances leading up to the failure
    - The more information the better chance of finding the source of the EOS
  - Analyze Circuit/Board/System configuration
  - Form Theory
  - Experimentation
    - Amount of experimentation depends on how frequently the EOS occurs
    - If the problem is 10ppm (one in 100,000 part) it will be difficult to find
    - If it is 1000ppm (one in 1000) may be easier but still not easy
    - If we have 10% failure then we may only have to test 20 to get a failure

Debugging EOS Damage

- Key Obstacles
  - Thinking about normal operation – EOS is not normal
    - EOS are events outside of the normal use of the parts
    - Think about what could breakdown or what parasitic elements could conduct if enough current/voltage was present
  - Don't point fingers
    - Customer and Vendor has to work together
    - Blame game will stall or kill progress
  - Looking for the wrong cause
    - Not willing to accept that fault
    - Looking at your process flow shows no issues
    - EOS is a probabilistic problem; if you have routine failures you should see it in a simple audit but if you only see 1 or two failures a month a simple audit will not detect the issue
  - Lack of Information
    - Sometimes vendors and customers are unwilling to share detailed information necessary to come up with a solution
    - The information is considered proprietary and cannot be shared

Concluding Remarks

- EOS damage is more prevalent on power components and HV circuits
- EOS occurs because of an event – not a gradual degradation; Frequency of the event determines how easy it is to find the source
- Damage is proportional with event – need to correlate damage to get estimate of event type
- Think in terms of excess voltage or excess current – excess voltage can induce undesired current paths (breakdown)
- Secondary damage produced when EOS current interrupted (inductive voltage spike)
- Always look for patterns in the damage as it relates to the application
- Keep communication lines open between customer and supplier
- The more information you can get and share the better chance you have of determining the source of the EOS
- Finding the source may take a lot of time and resources; Determine up front if you are willing to invest it