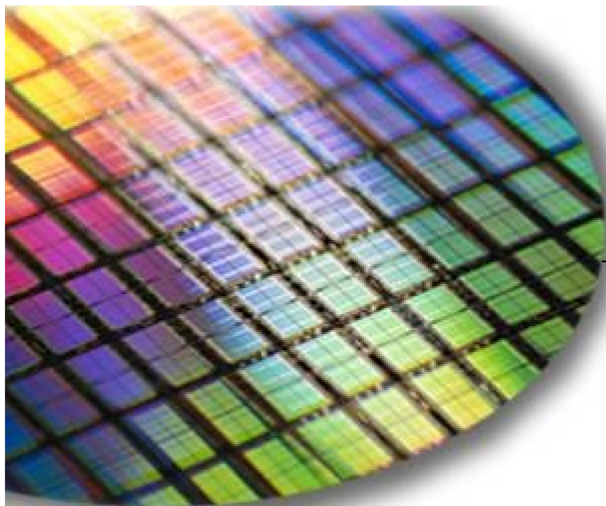

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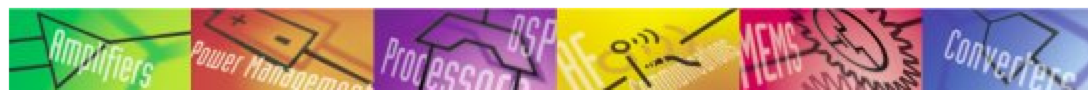


“Predicting Circuit ESD Performance Through SPICE-type Simulations”

Yuanzhong (Paul) Zhou,
Thorsten Weyl &
Jean-Jacques (J-J) Hajjar
Analog Devices Inc.

IEEE Electron Device Colloquium
University of Central Florida
February 21-22, 2008

Proprietary Information

MOTIVATION

- **ESD high on Pareto chart of reliability product returns from customers**
- **Predicting ESD performance is very compelling:**
  1) Design tool prior to manufacturing
  2) Design verification
  3) *Post-mortem* failure troubleshooting tool

—Analog Devices Proprietary Information—
ANALOG DEVICES

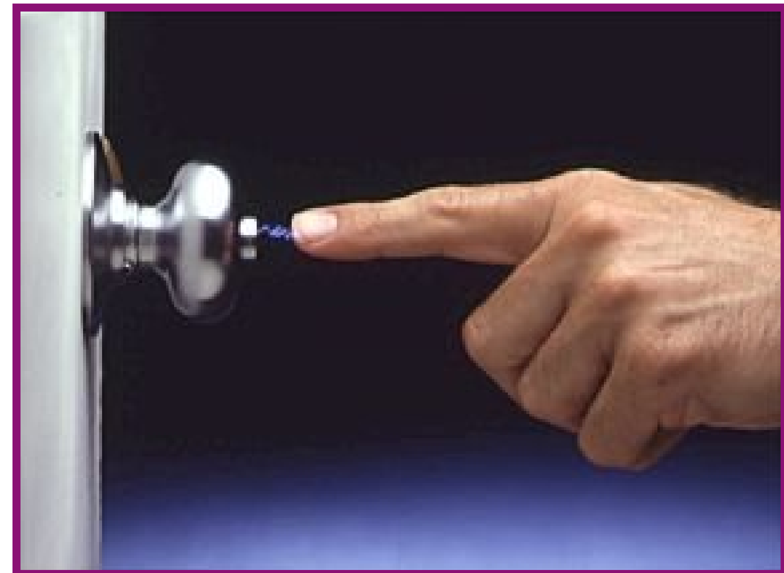
OUTLINE

- What is ESD?
- Circuit Simulation Consideration
- Compact Modeling Approaches and Modeling Verification
- ESD Circuit Simulation Examples
- Concluding Remarks

—Analog Devices Proprietary Information—

What is ESD?

- ESD: Electrostatic Discharge
- Cause: Tribo-electric charge transfer
- Characteristics
  - High energy resulting
    - Large currents
    - High voltages
  - Short in duration (typically <1 to over 100 nano-seconds)



from RTP Company, Winona, MN

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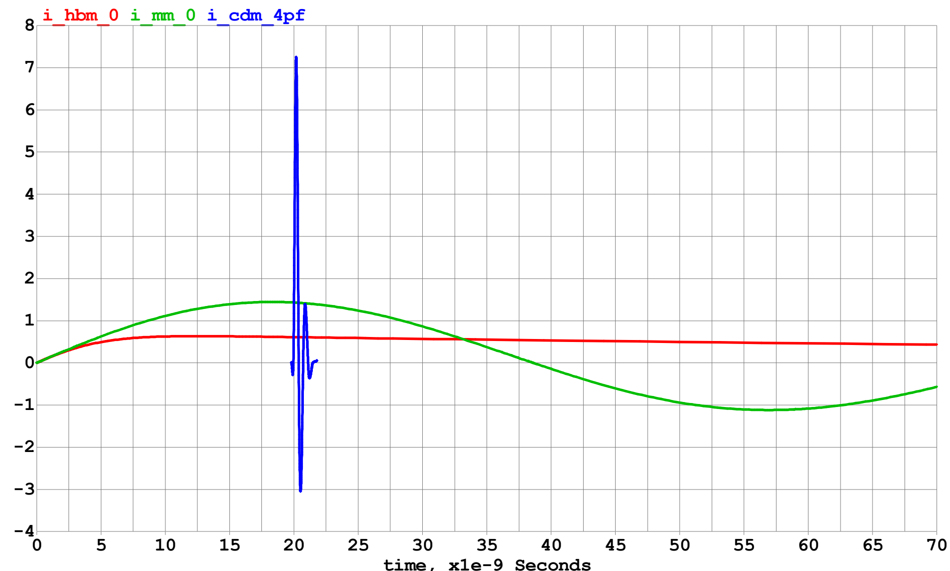
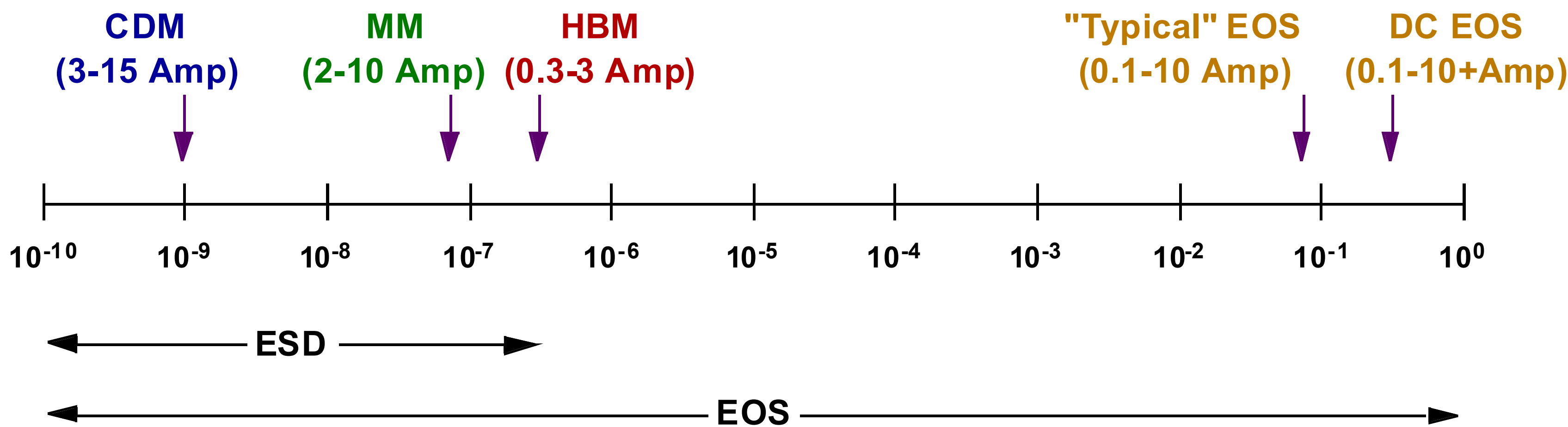
ANALOG DEVICES

SOURCE of ESD

- Human touches IC: Human Body Model (HBM)
- Charged IC touches grounded surface: Charged Device Model (CDM)
- Charged machine touches IC: Machine Model (MM)





TIME in SECONDS (LOG SCALE)

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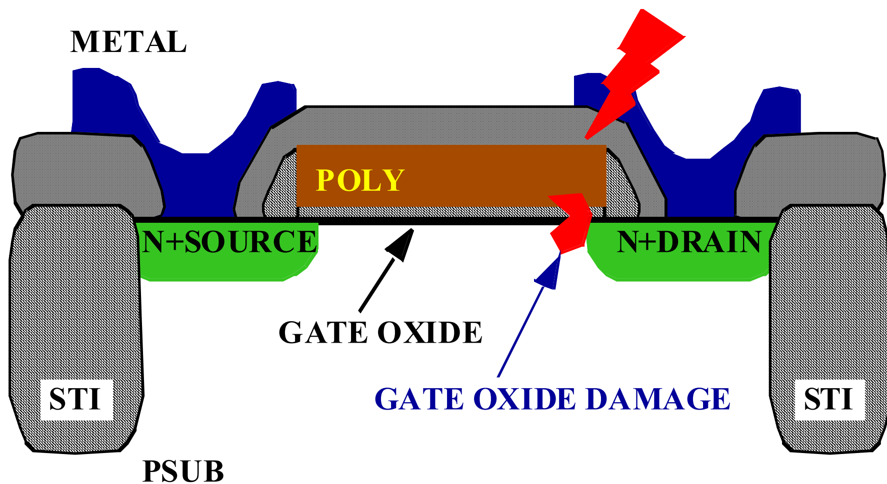
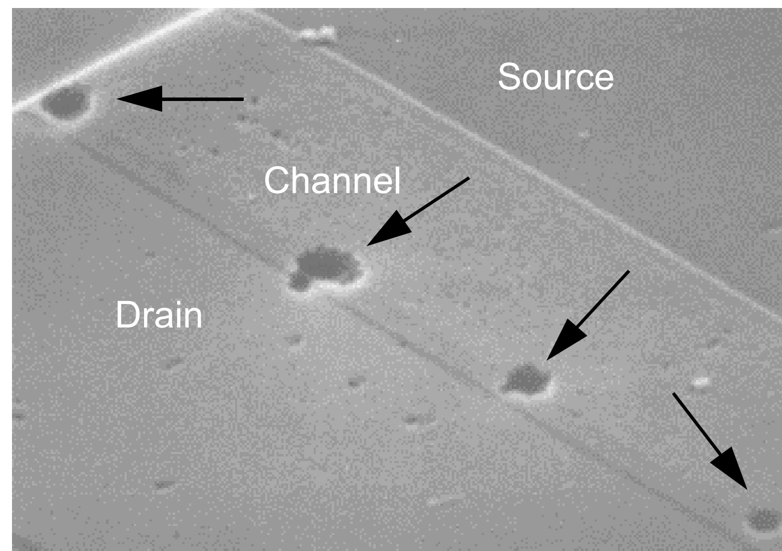
ANALOG DEVICES

ESD DAMAGE in ICs (1)
MOSFET Gate-Oxide Punch-through





- **SEM micrograph depicts NMOS after de-processing.**
- **Pits are 0.2 to 0.5µm in width & correspond to regions where Si flowed into gate oxide.**

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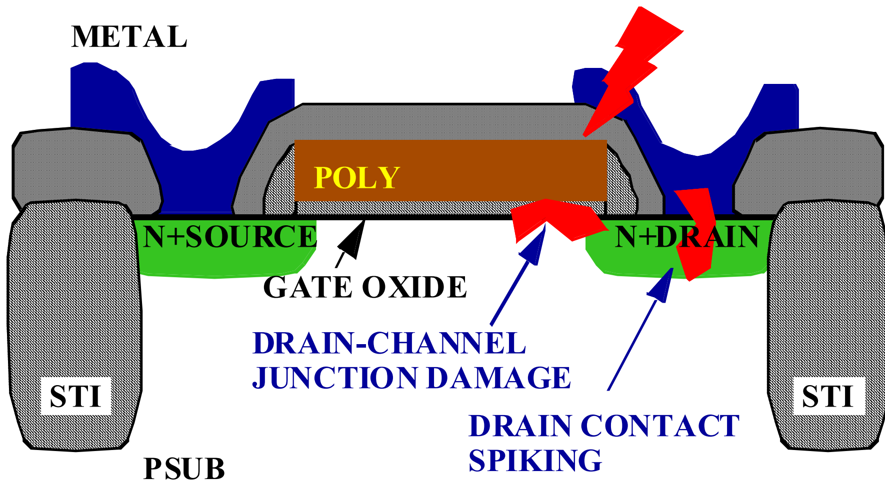
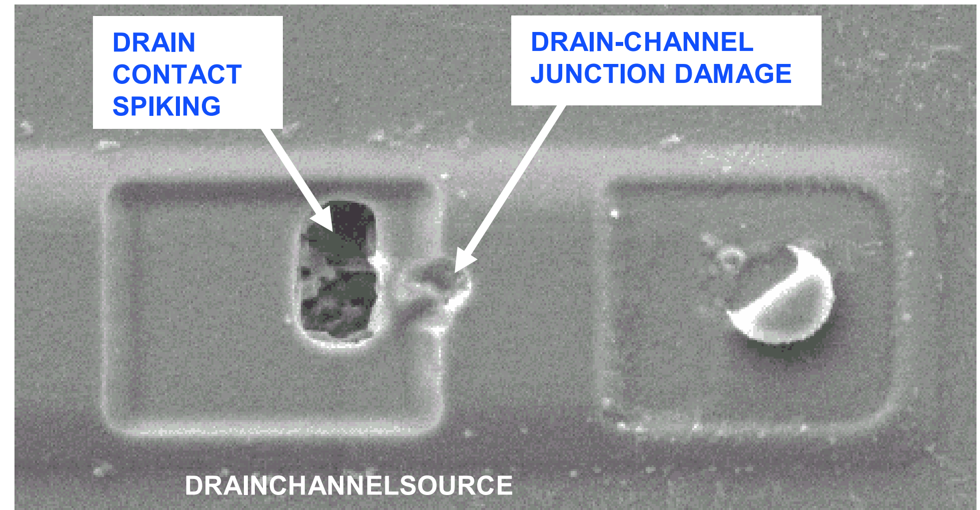
ANALOG DEVICES

ESD DAMAGE in ICs (2)
Junction Damage/Contact Spiking

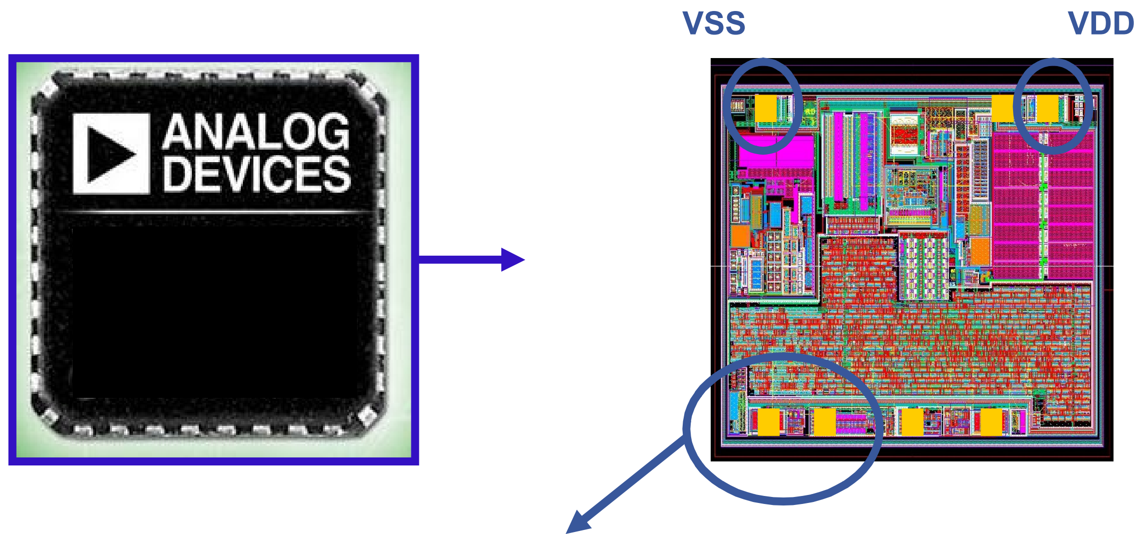


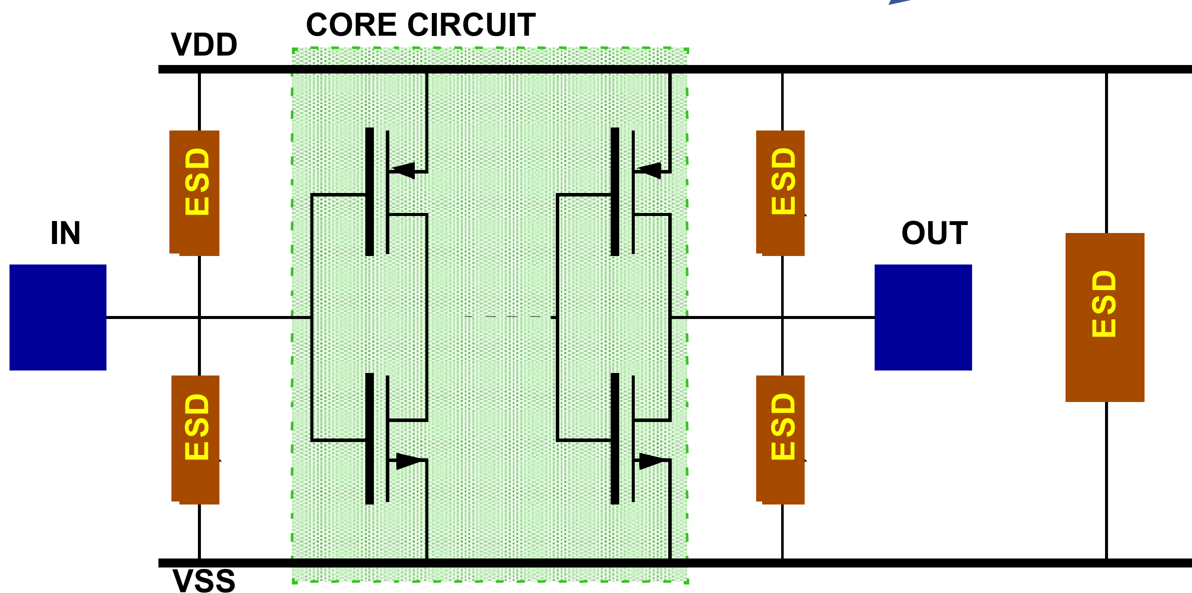


- **SEM micrograph depicts NMOS after de-processing.**

—Analog Devices Proprietary Information—

On-Chip ESD PROTECTION SCHEMES





OBJECTIVE:

1. Shunt current discharges away from the *CORE CIRCUIT*
2. Clamps I/O & Power pad voltage to a safe level

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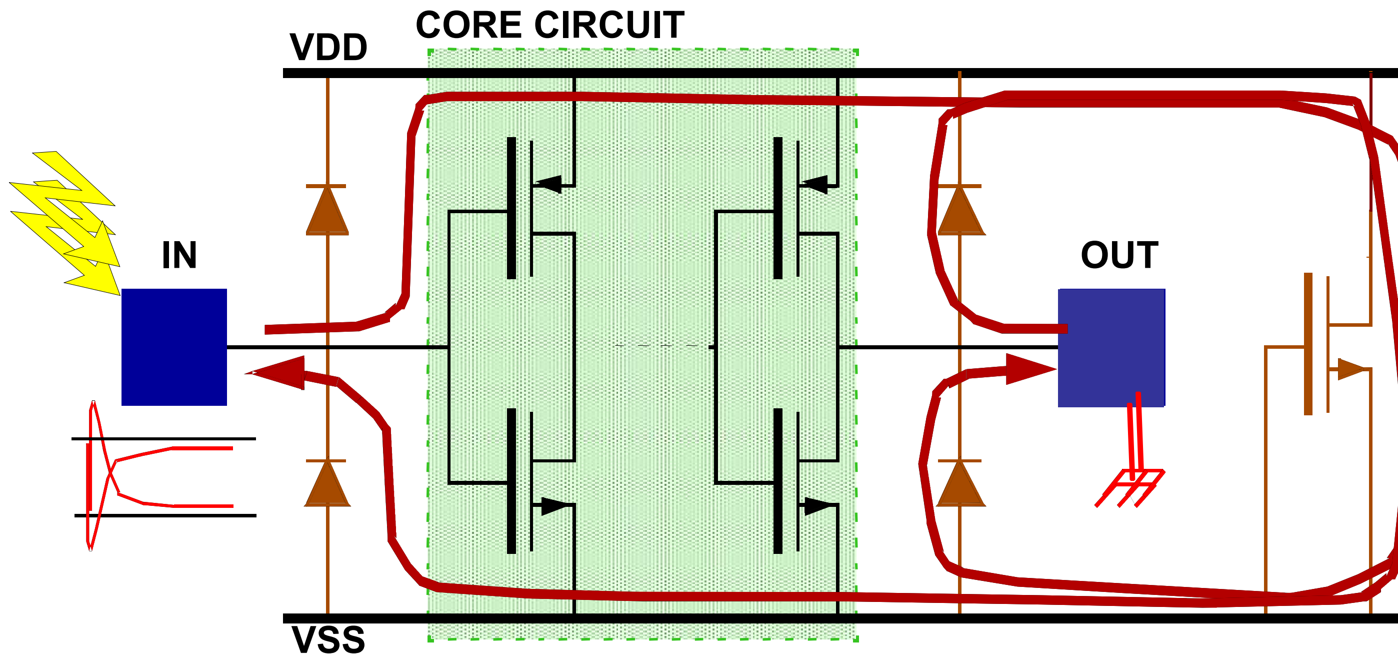
On-Chip ESD PROTECTION SCHEMES

An Example



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ANALOG DEVICES

Circuit Simulation Considerations

- Impact of ESD structure on I/O and core circuits.
- ESD current paths.
- Impact of internal circuitry on ESD protection performance.
- Optimization to reduce ESD over design.

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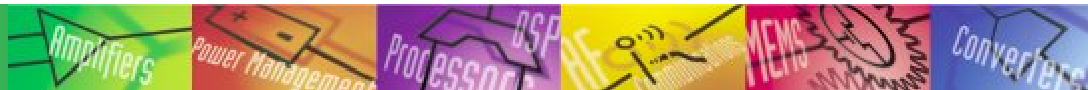
ANALOG DEVICES



Circuit Simulation Approach

- SPICE is a Primary Tool for Circuit Level Simulation
- ESD–capable Compact Device model
- Modeling physical phenomenon particular to ESD:
  - *Breakdown*
  - *Snapback*
  - *…*

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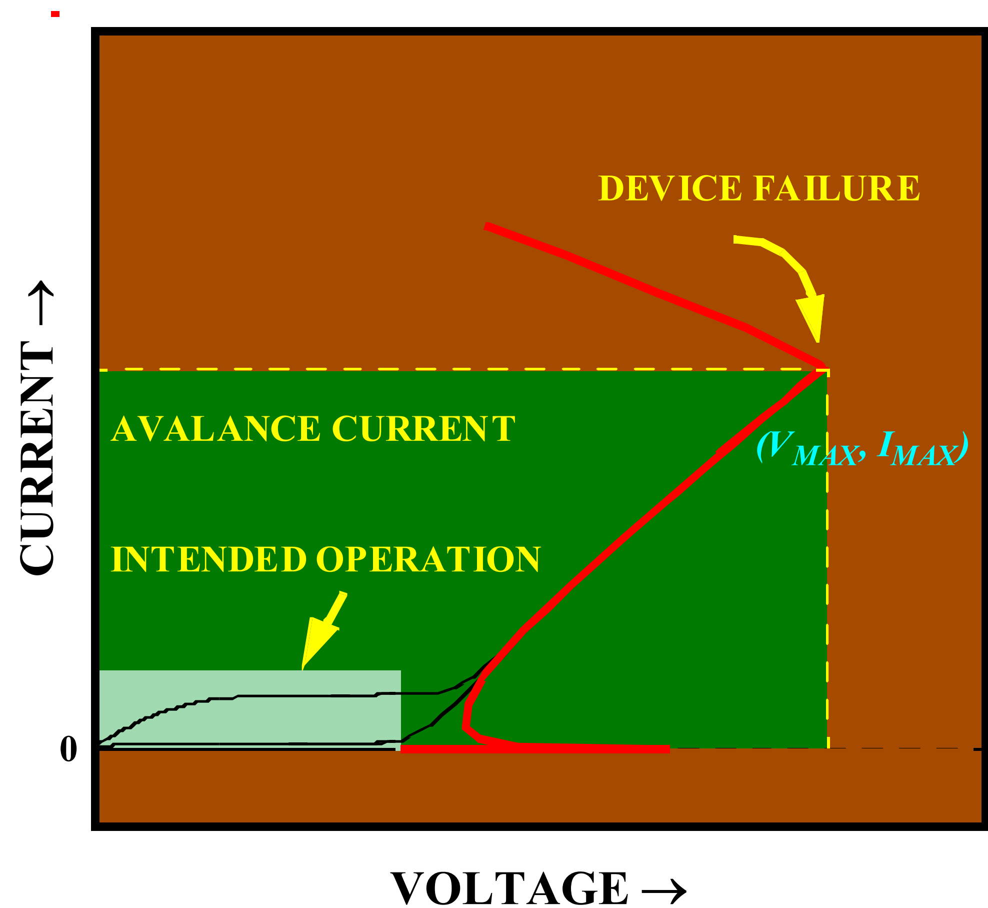
ANALOG DEVICES

Major Challenges (1)

- Devices operate in unintended bias space:
  - high voltages
  - very large currents



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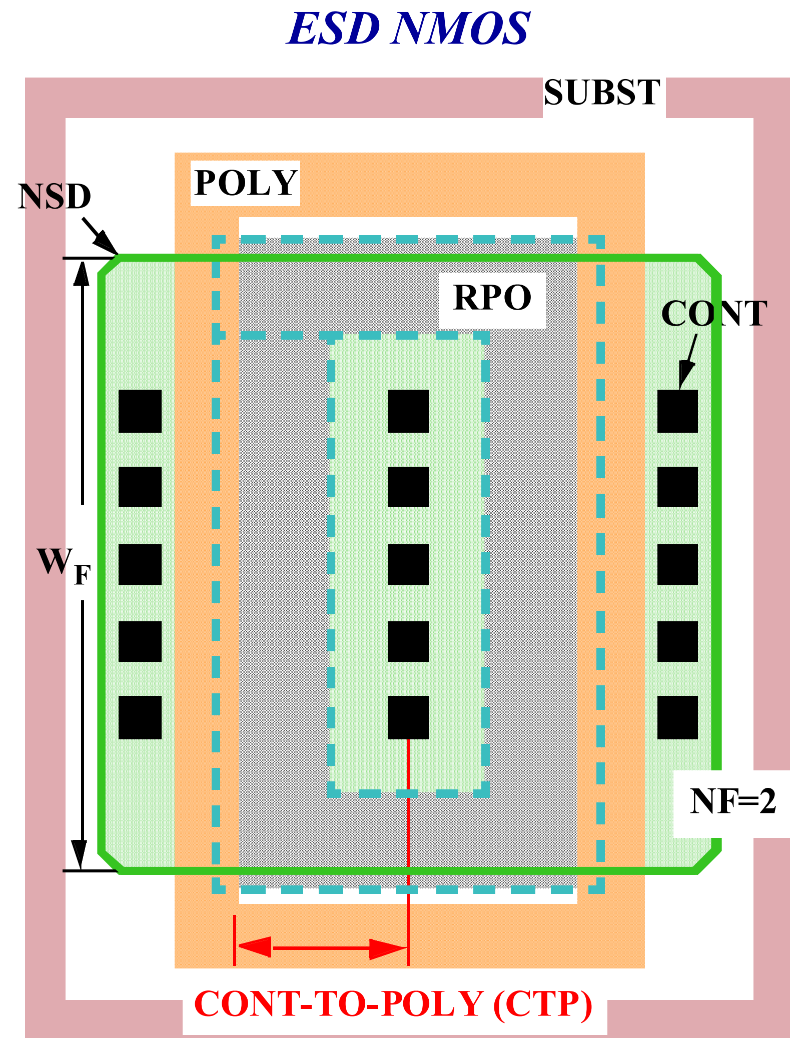
Major Challenges (2)

- Device operation highly dependent on layout.
  - ESD NMOS – DESIGN SPACE
    - Width
    - Gate length
    - w/ or w/o RPO in drain
    - Drain side CTP
    - Gate stripes
    - Substrate contact



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ANALOG DEVICES

Major Challenges (3)

- Thermal effects important
- Parasitics (*L, C & R*) critical due to fast-transient nature of ESD:
  - Interconnect
  - Package
  - Board
  - Test fixture
  - …

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ANALOG DEVICES

What Devices to Model?

Primary Protection Devices

1) MOS
2) SCR
3) Bipolar
4) Diodes
5) Resistors

Modeling Strategy

1) Modify standard Compact models
2) Customized Model

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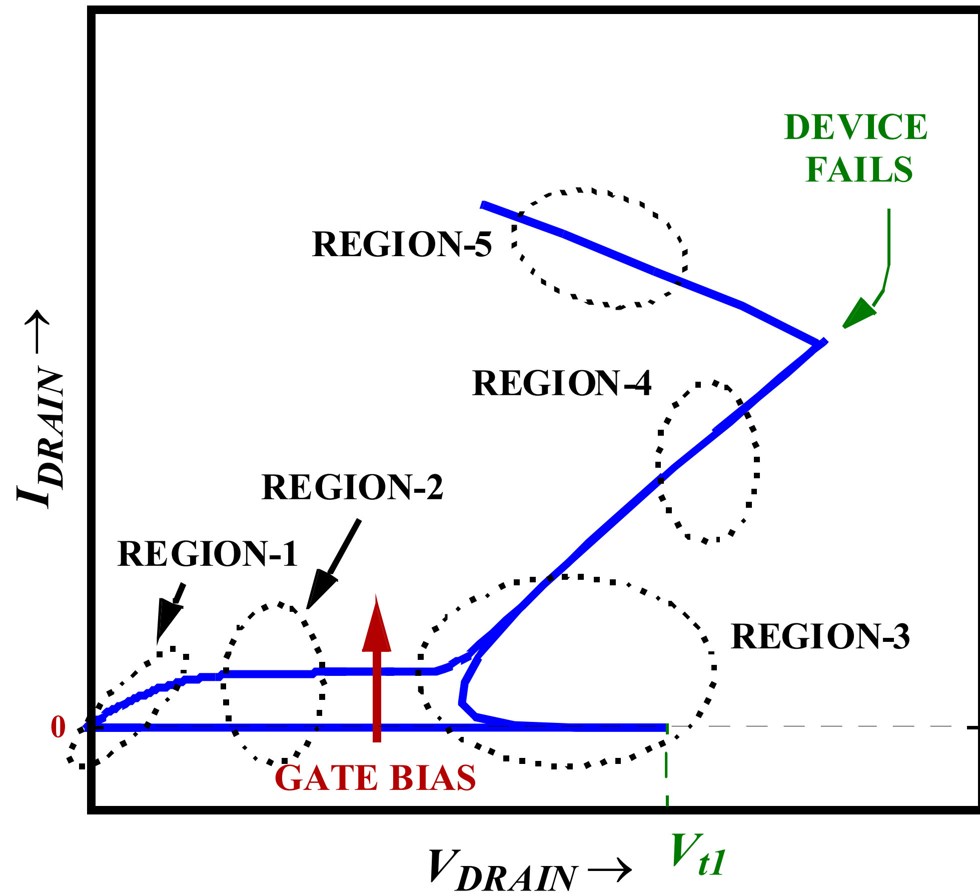
Snapback in ESD Devices

- Devices (MOS) operating in "snapback" mode carries more current per unit width
- Operating I-V Regions of MOS Devices
  1) Linear Region
  2) Saturation Region
  3) Avalanche Region
  4) Snapback Region
  5) Failure Region
- V_{t1} represents the "snapback effect" trigger voltage



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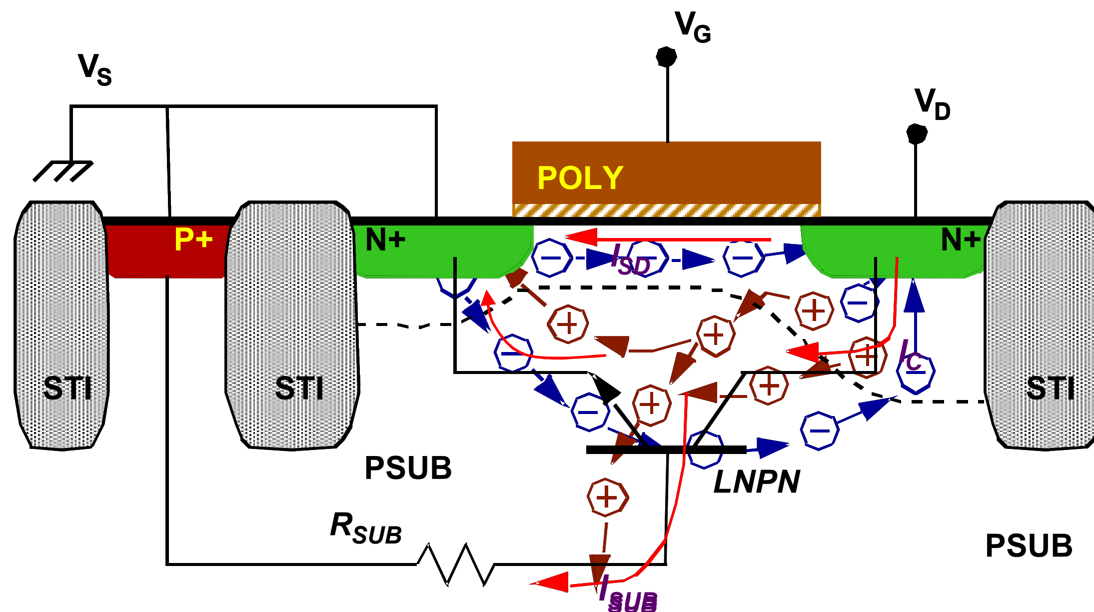
ANALOG DEVICES

Snapback in MOS Devices

Snapback Effect in MOS is due to the Parasitic BJT, triggered by the substrate current (I_{SUB}).



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ANALOG DEVICES

Critical Effects in Snapback Modeling

- Substrate current as function of V_{DS}, V_{GS} and V_{BS}
  - Due to impact ionization in Drain/Backgate depletion layer.
  - Avalanche current multiplication factor is different before and after snapback
  - Displacement current (*dV/dt*) through Drain/Backgate junction
  - Gate induced drain leakage (GIDL)

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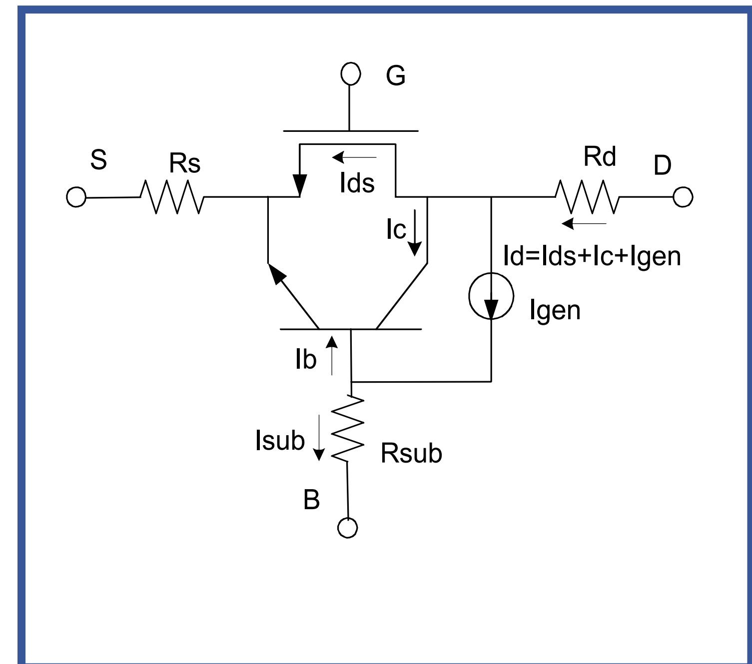
ANALOG DEVICES

Previous Snapback Models

- Standard MOS and BJT models.
- An explicit current source which is a function of V_{GS} and V_{DS}
- (*dV/dt*) effect, GIDL and separate M for MOS and BJT are included in some models by adding equations.
- The implementation of the models includes C code and behavioral languages (*Verilog-A*)



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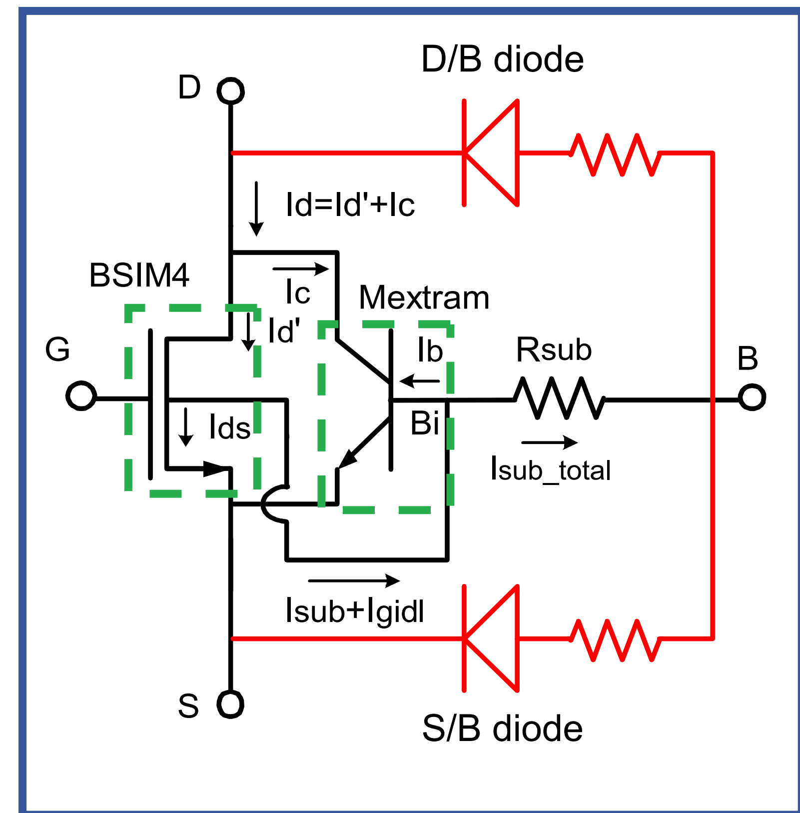
ANALOG DEVICES

Model for MOS under ESD Stress

- New approach eliminates the current source of previous models.
- Model constructed of standard BJT (Mextram) and MOS (BSIM4) devices.
- Models intrinsically includes all major physical phenomenon presented.
- Source/Backgate and Drain/Backgate Junction Diodes for completeness.



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Model Verification

- Transmission Line Pulse measurement:
  - *Quasi-static*
  - *Transient*

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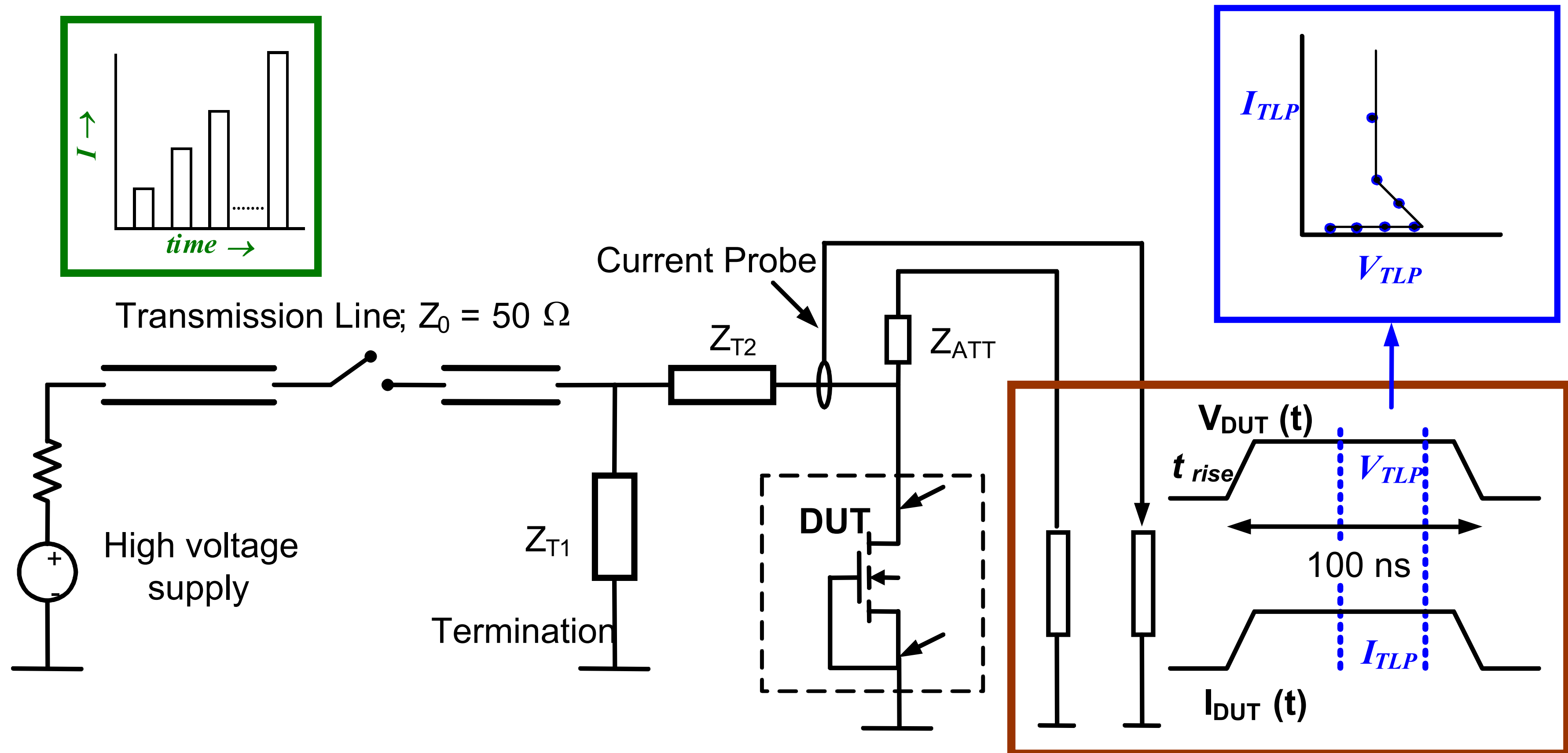
Transmission Line Pulse (TLP)

Measurement Setup



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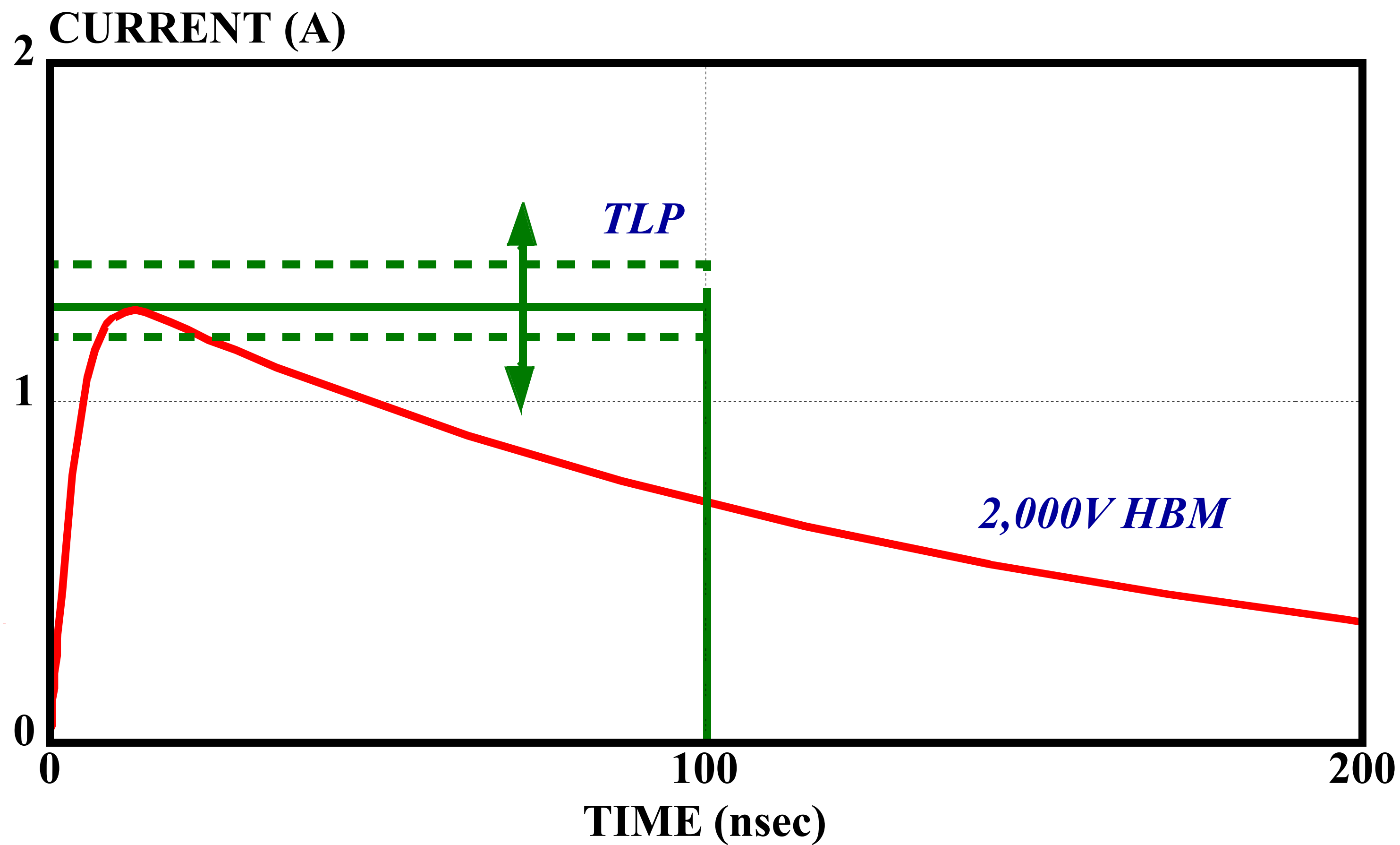
ANALOG DEVICES

Why Transmission Line Pulse?



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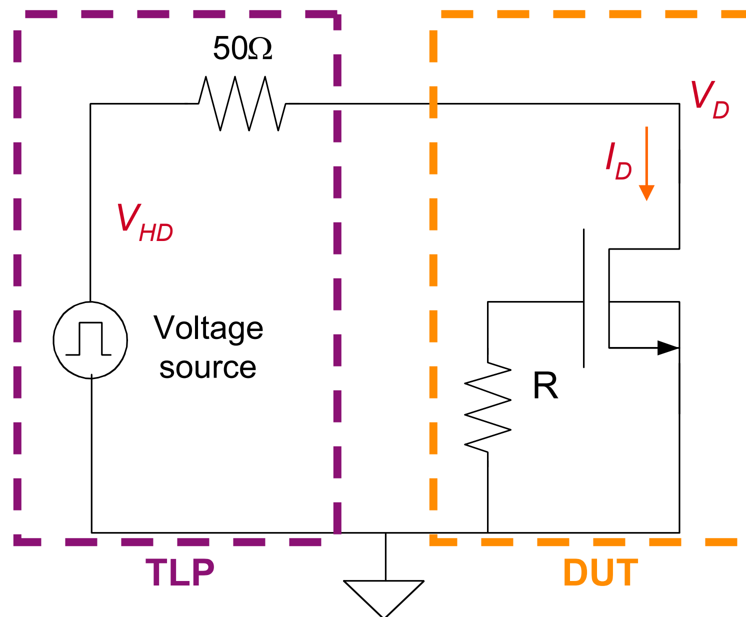
ANALOG DEVICES

Model Verification

- Snapback effect was simulated with transient simulation.
- Voltage Pulse Sequence (100ns) were used as the Input.
- The stabilized V_D and I_D were measured as the simulation results (~80ns).



Schematic of Snapback Simulation (R=0Ω for ggNMOS)

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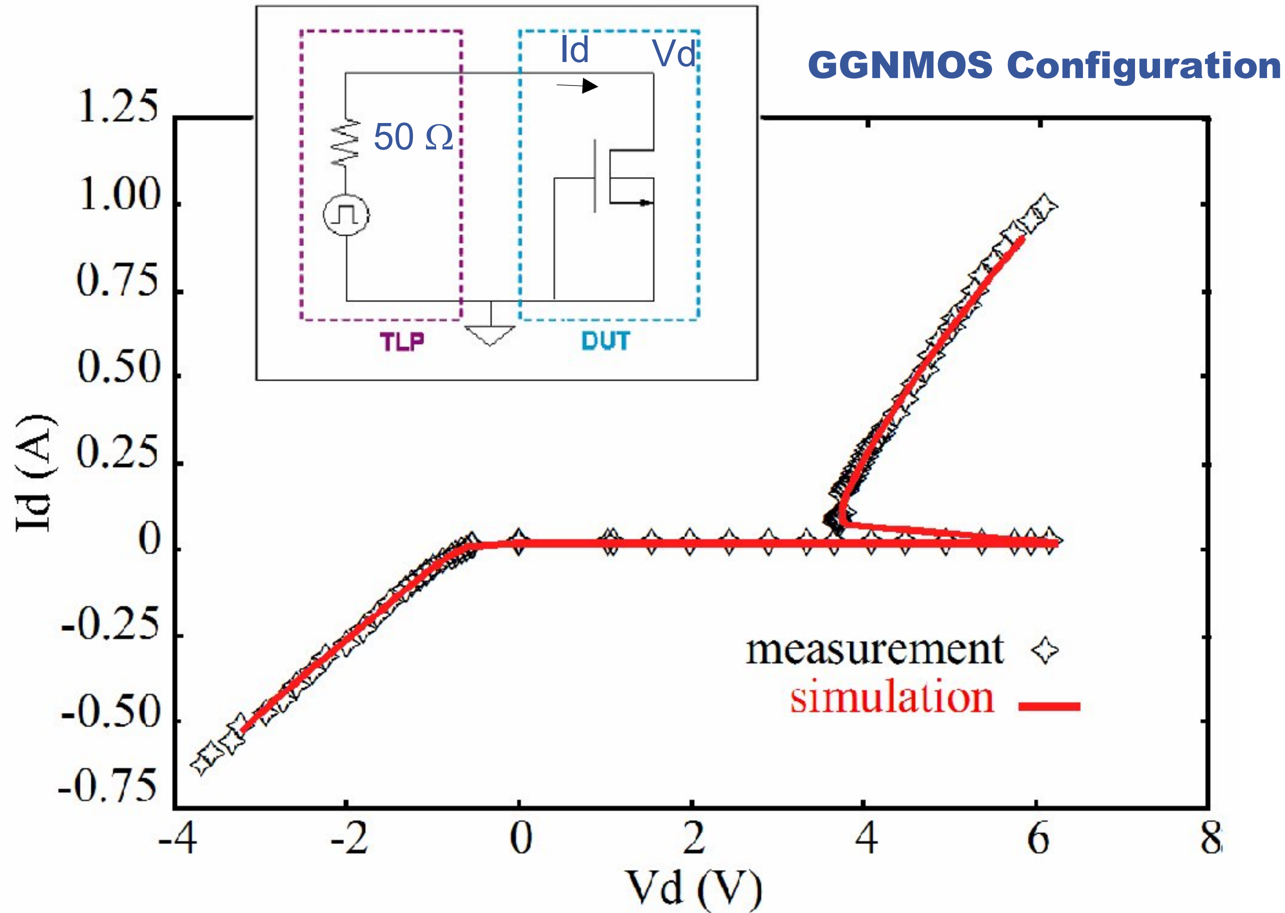
ANALOG DEVICES

Simulation Results vs. TLP Measurement

A ggNMOS device

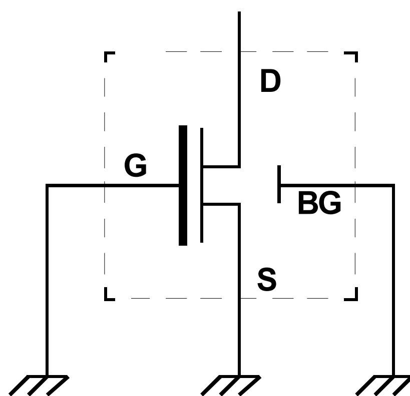


—Analog Devices Proprietary Information—

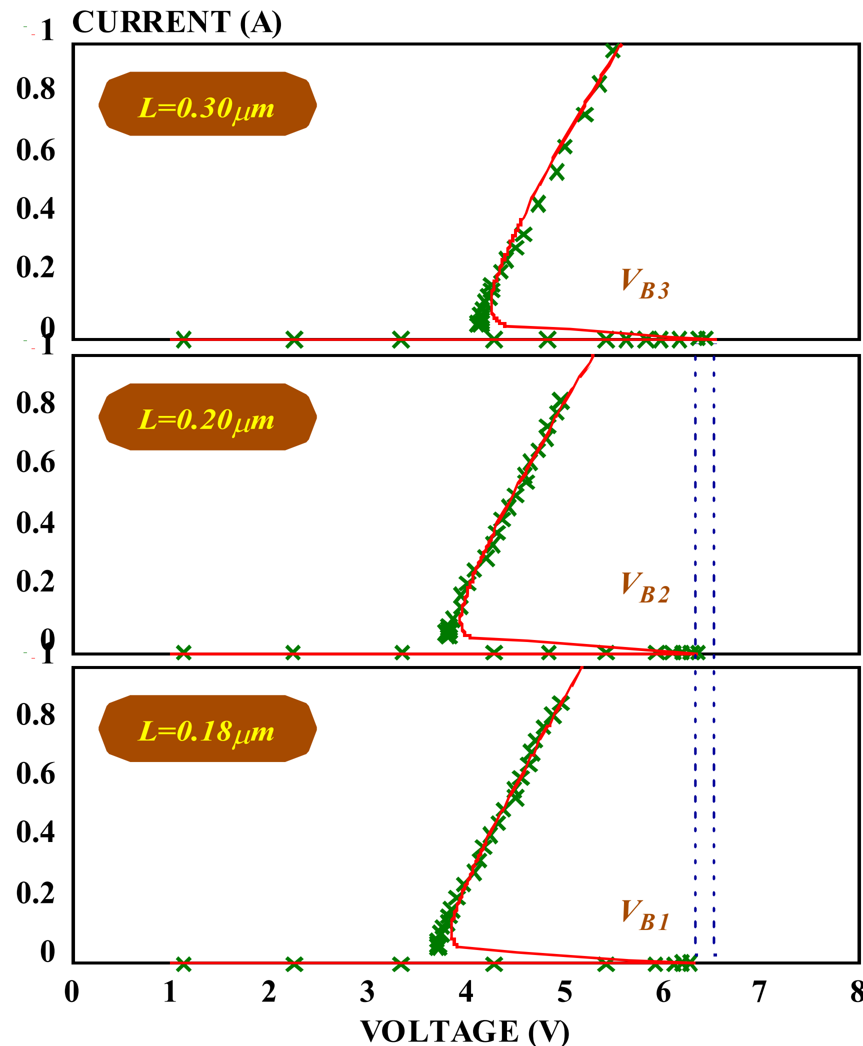
ANALOG DEVICES

MOS CHARACTERISTICS & MODEL

- **Deep submicron CMOS**
- **Model Scalability**
  - W = 300μm
  - 0.18 < L < 0.30 μm
  - Stripes = 12
  - Wrap-around backgate contact



GGNMOS



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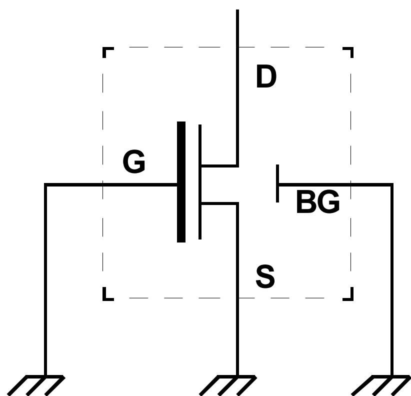
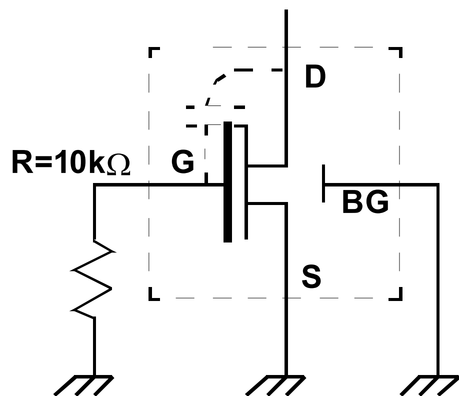
ANALOG DEVICES

MOS CHARACTERISTICS & MODEL

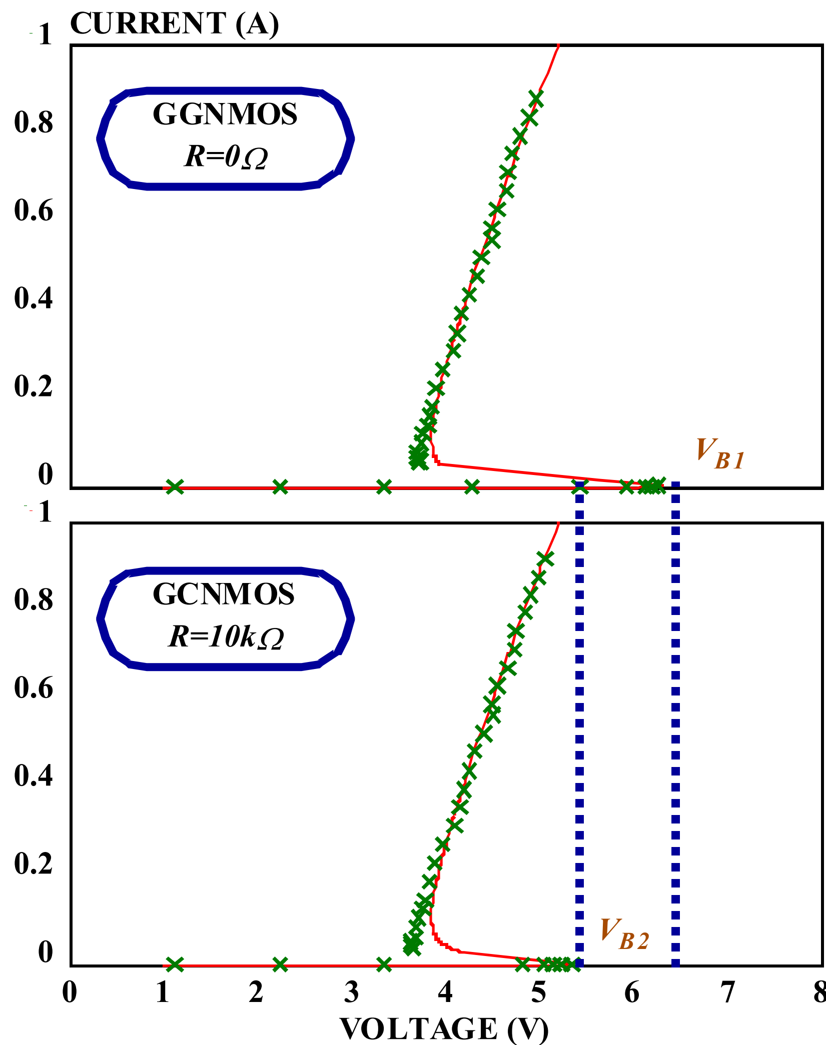
- **Deep submicron CMOS**
  - W/L = 300/0.18μm; Stripes = 12



GGNMOS



GCNMOS



100ns TLP: Sim vs. msmt

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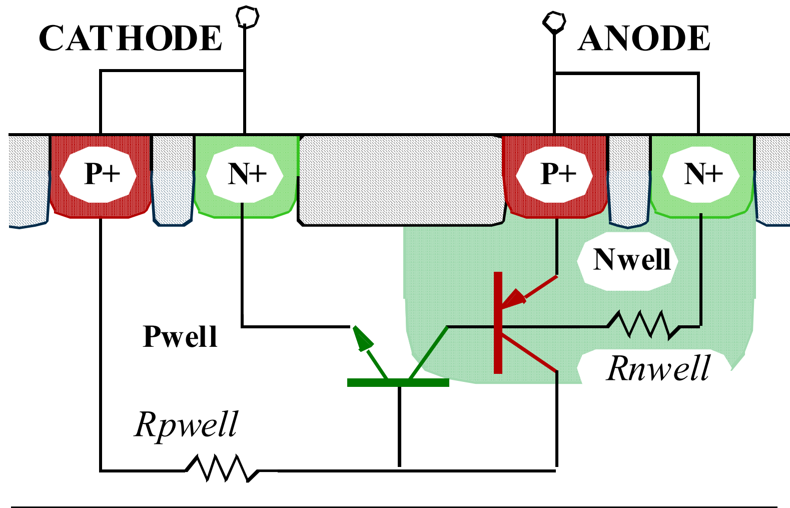
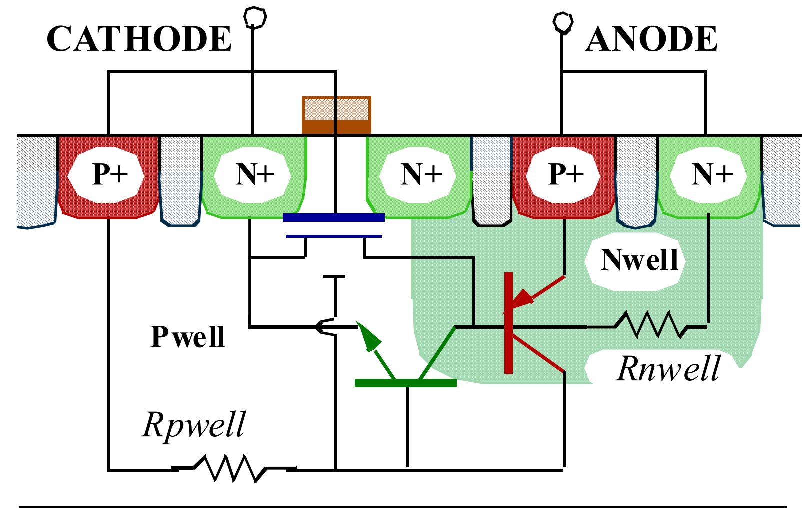
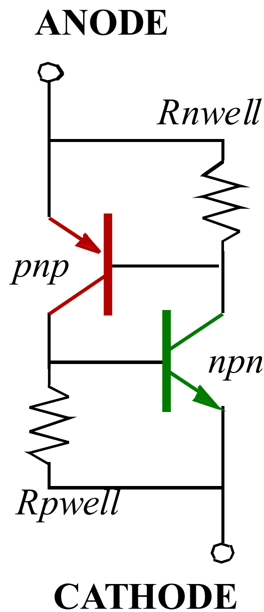
ANALOG DEVICES

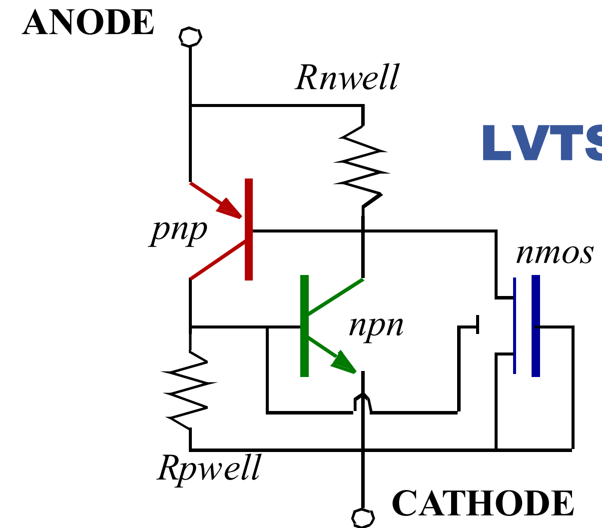
SCR Devices





SCR





LVTSCR

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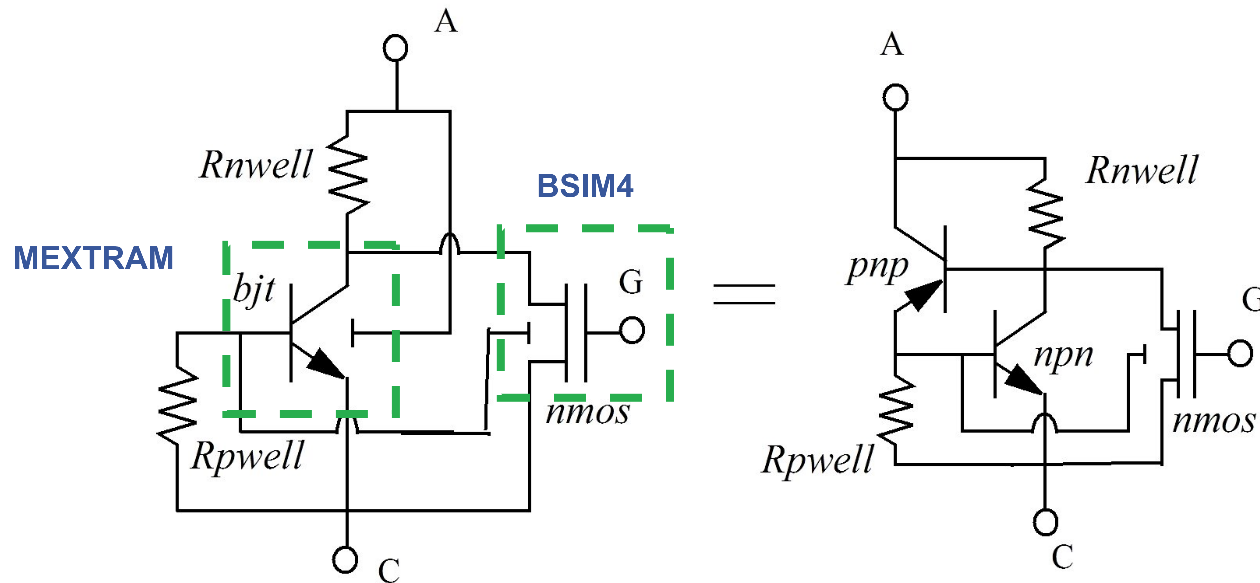
ANALOG DEVICES

Macro Model for LVTSCR

- Similar approach to MOS
- New model consists of four components:
  - An NMOS modeled by BSIM4
  - A four terminal NPN modeled by Mextram
  - Two resistors



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ANALOG DEVICES

Key effects in New LVTSCR Macro Model

- The PNP is modeled by the parasitic BJT in the 4 terminal NPN modeled by a Mextram-like model
- Current sources for avalanche and GIDL are intrinsically built in MOS and BJT models

$$I_{GEN} = I_{AVL} + I_{SUB} + I_{GIDL}$$

- Decoupled multiplication factors for BJT and MOS are included in I_{AVL} and I_{SUB} respectively
- The *dV/dt* effect is modeled by Collector/Base junction capacitance of the BJT

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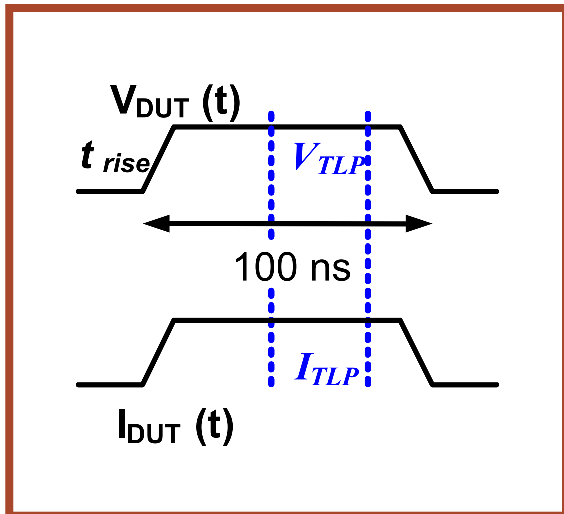
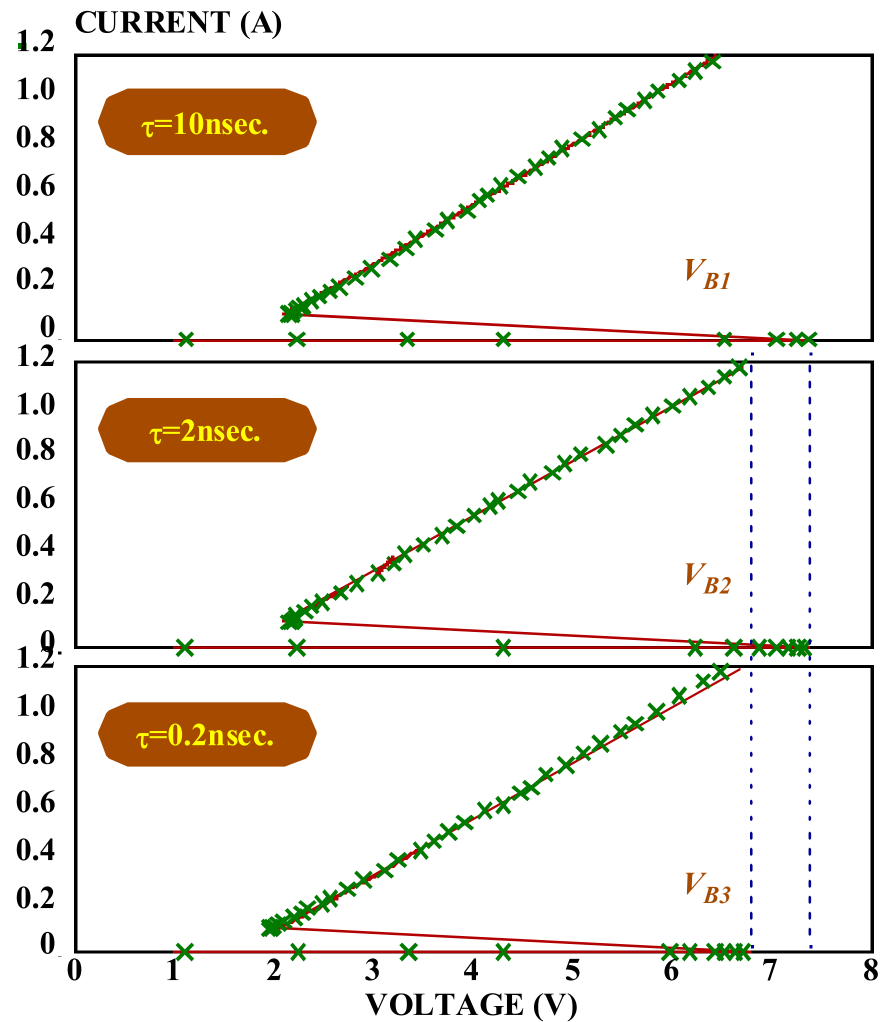
ANALOG DEVICES

SCR CHARACTERISTICS & MODEL

- CMOS: SCR-1
- 100nsec TLP Pulse
  - Different pulse rise-time





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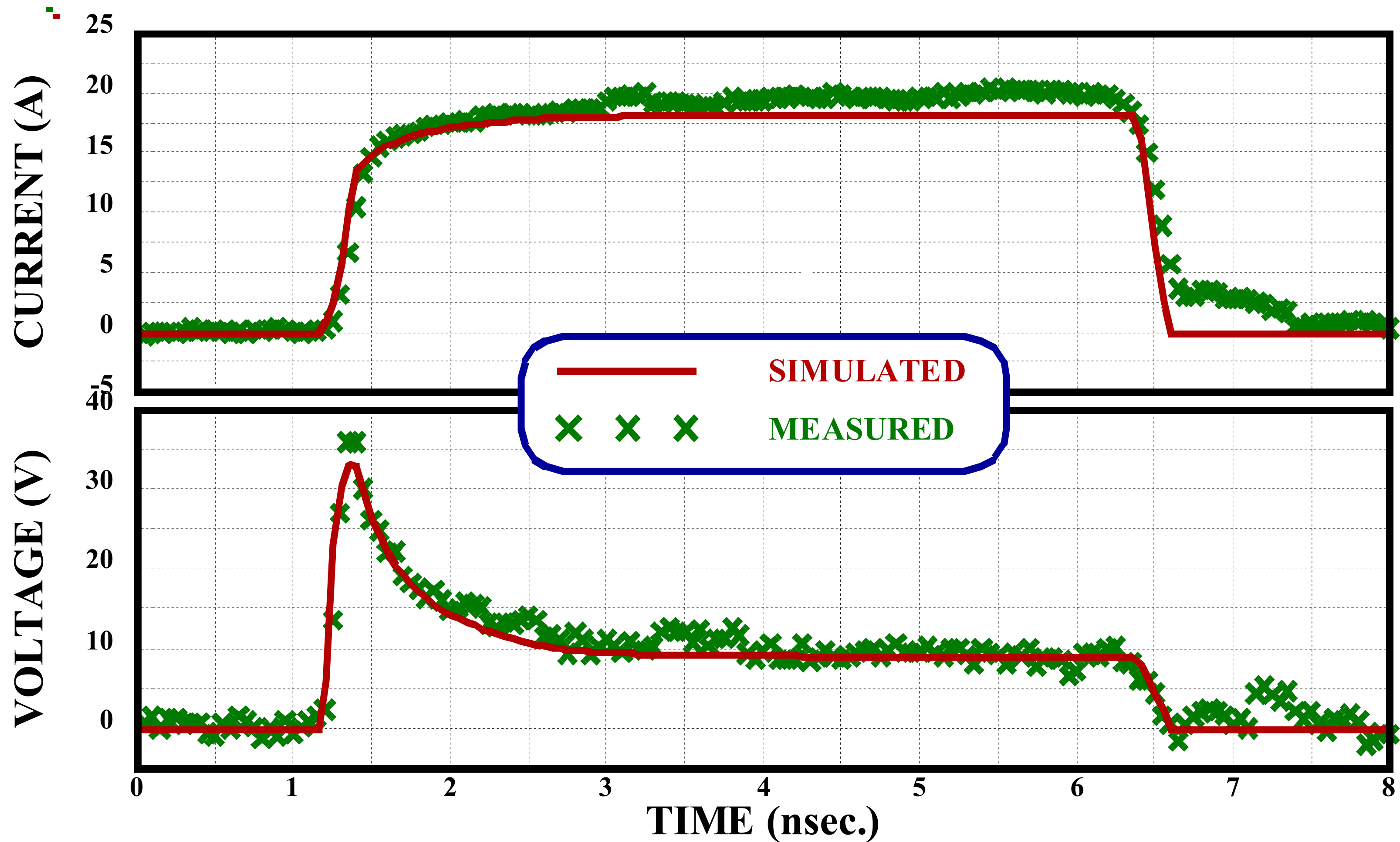
SCR CHARACTERISTICS & MODEL

- **CMOS: SCR-1**



VFTLP: SCR ADICE Simulation vs. measurement

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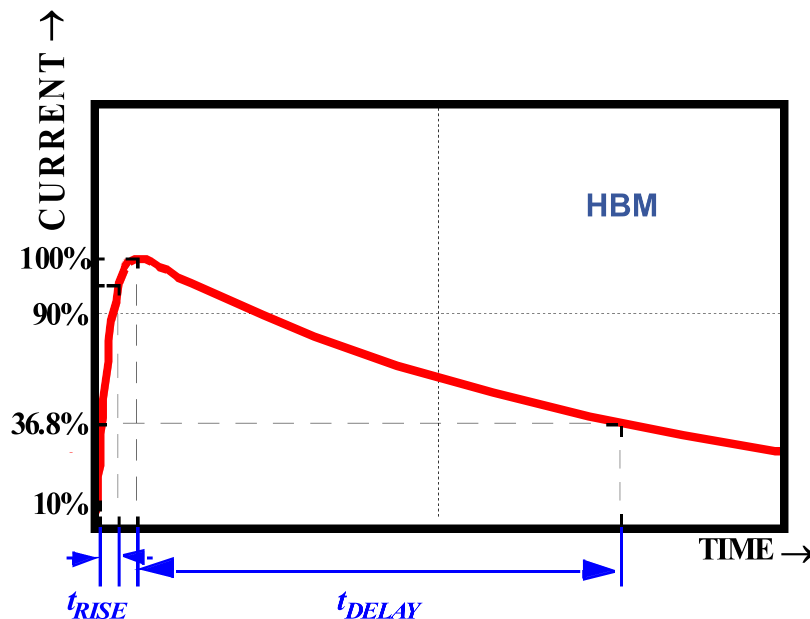
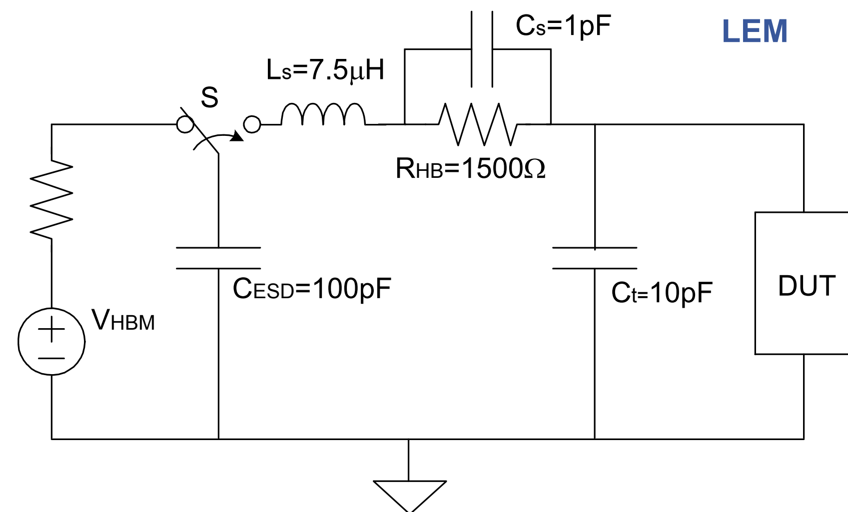
ANALOG DEVICES

CIRCUIT SIMULATION

Human Body Model (HBM)

- Simulates the discharge from the finger of a standing person
- I_{PEAK} = ~0.67 A/kV, t_{RISE} ~ 5-9ns, t_{DELAY} = ~150 nsec.
- Modeled by a Lumped Element Model (LEM)





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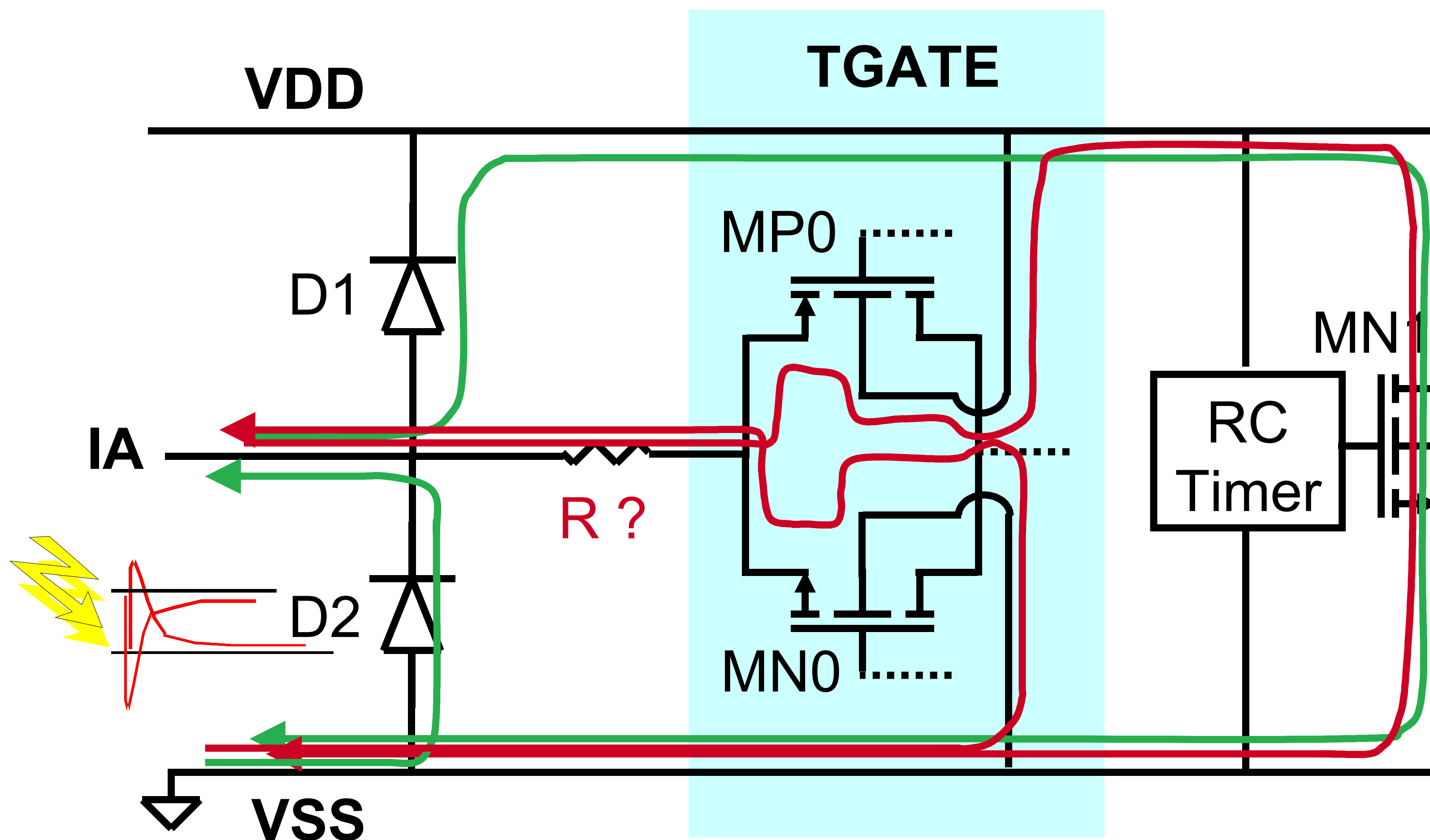
SPICE Simulation Examples

I/O Cell – Circuit



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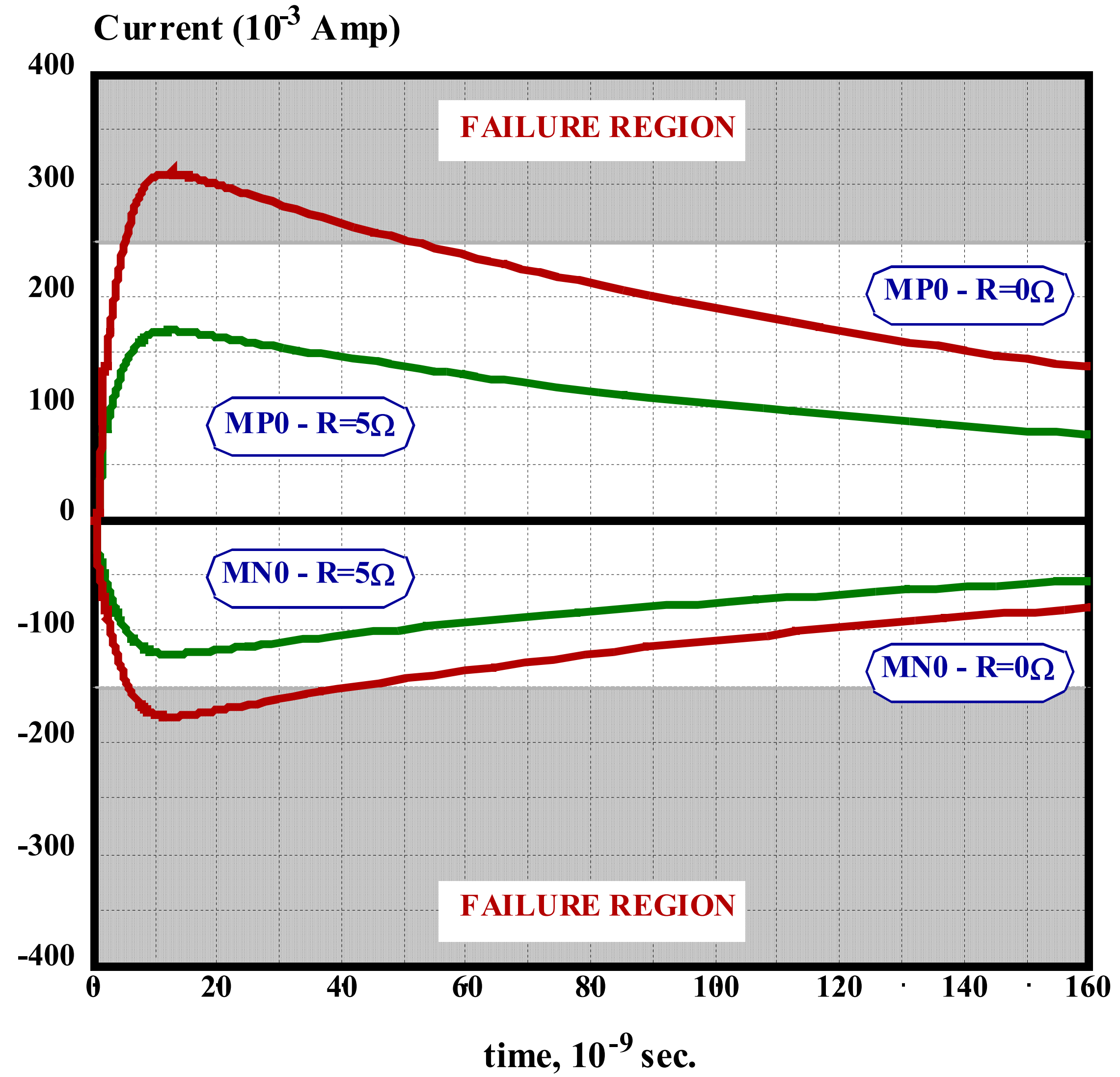
ANALOG DEVICES

SPICE Simulation Examples

I/O Cell – Simulation



W_{PMOS}~$2W_{NMOS}$

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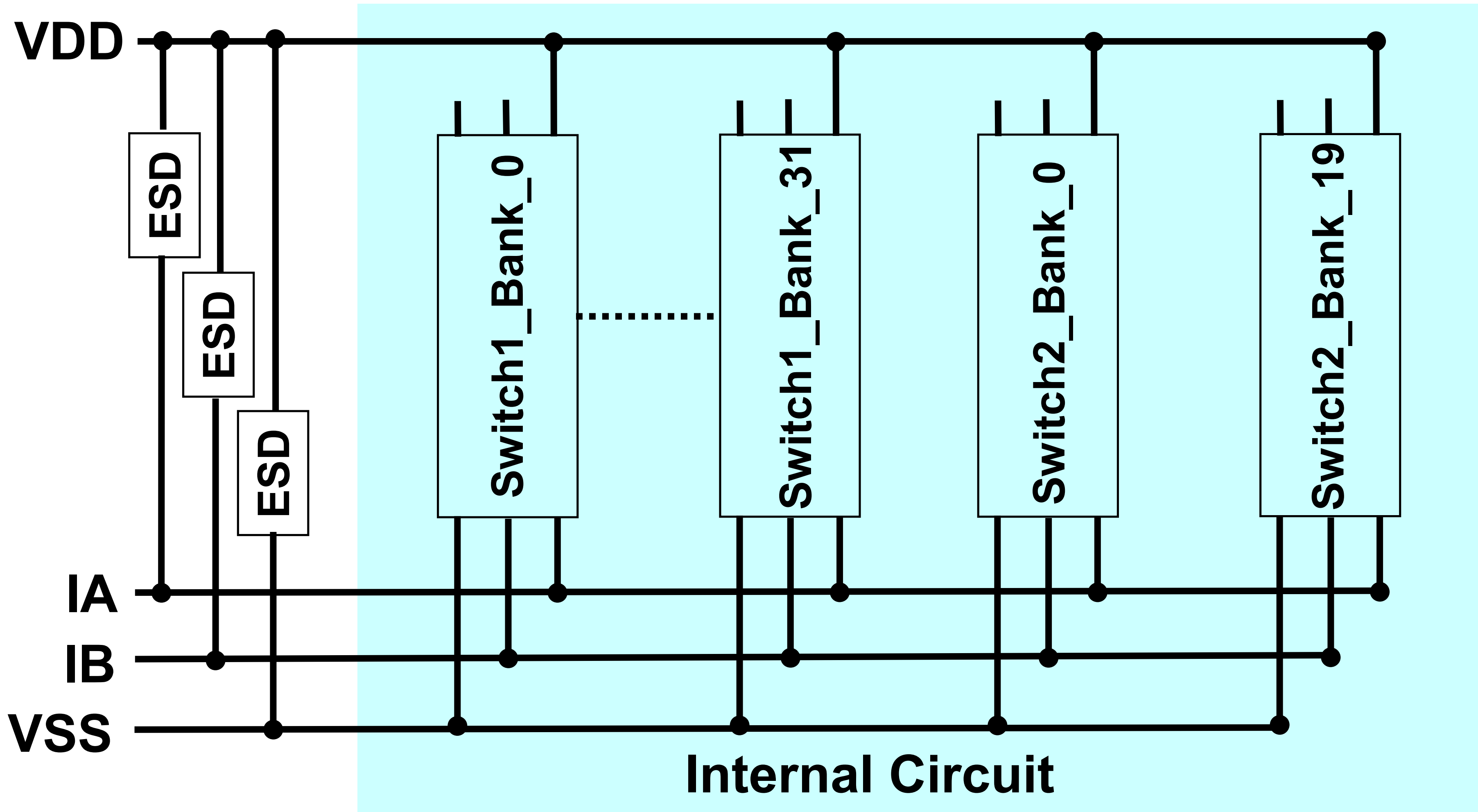
SPICE Simulation Examples

Block Level



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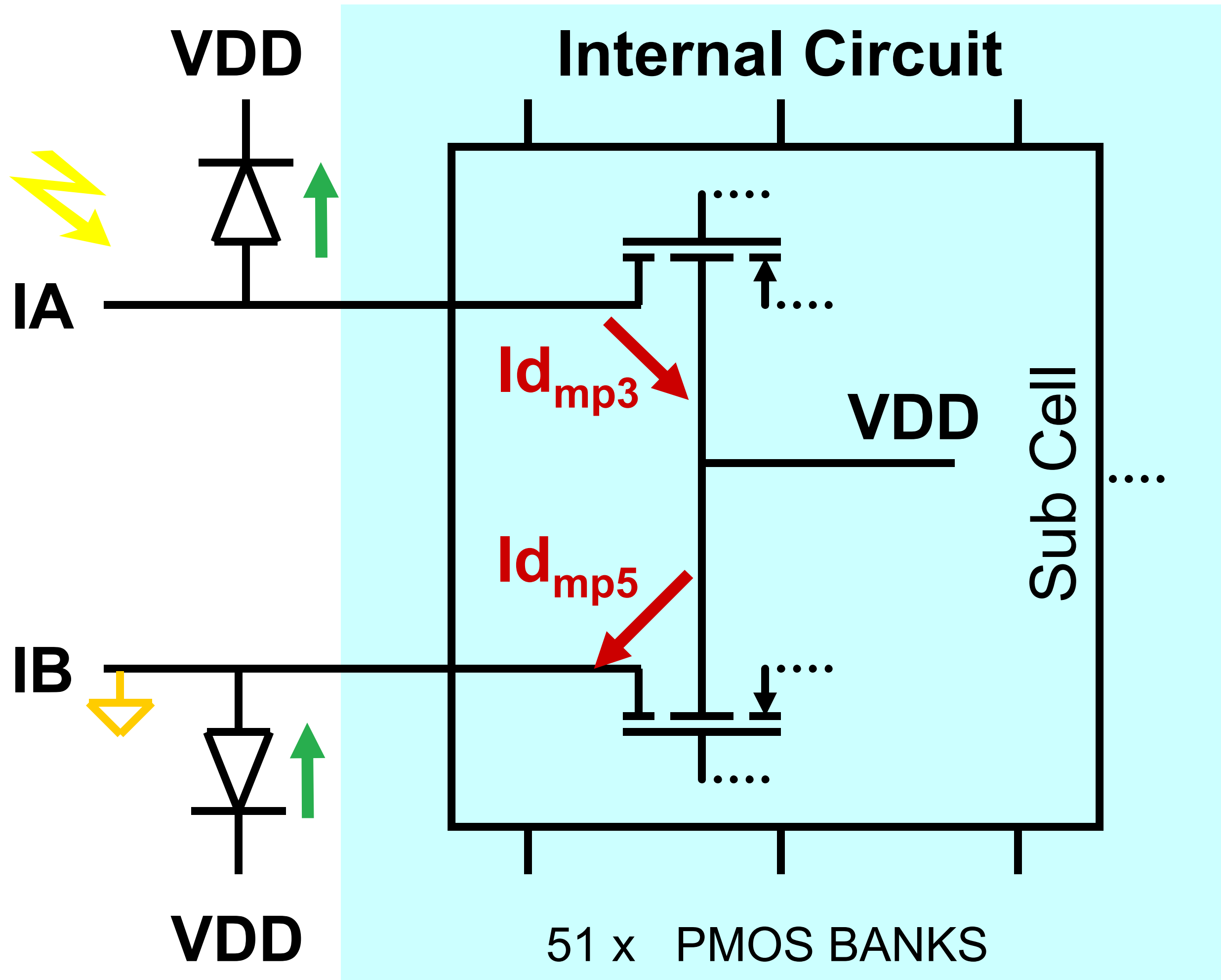
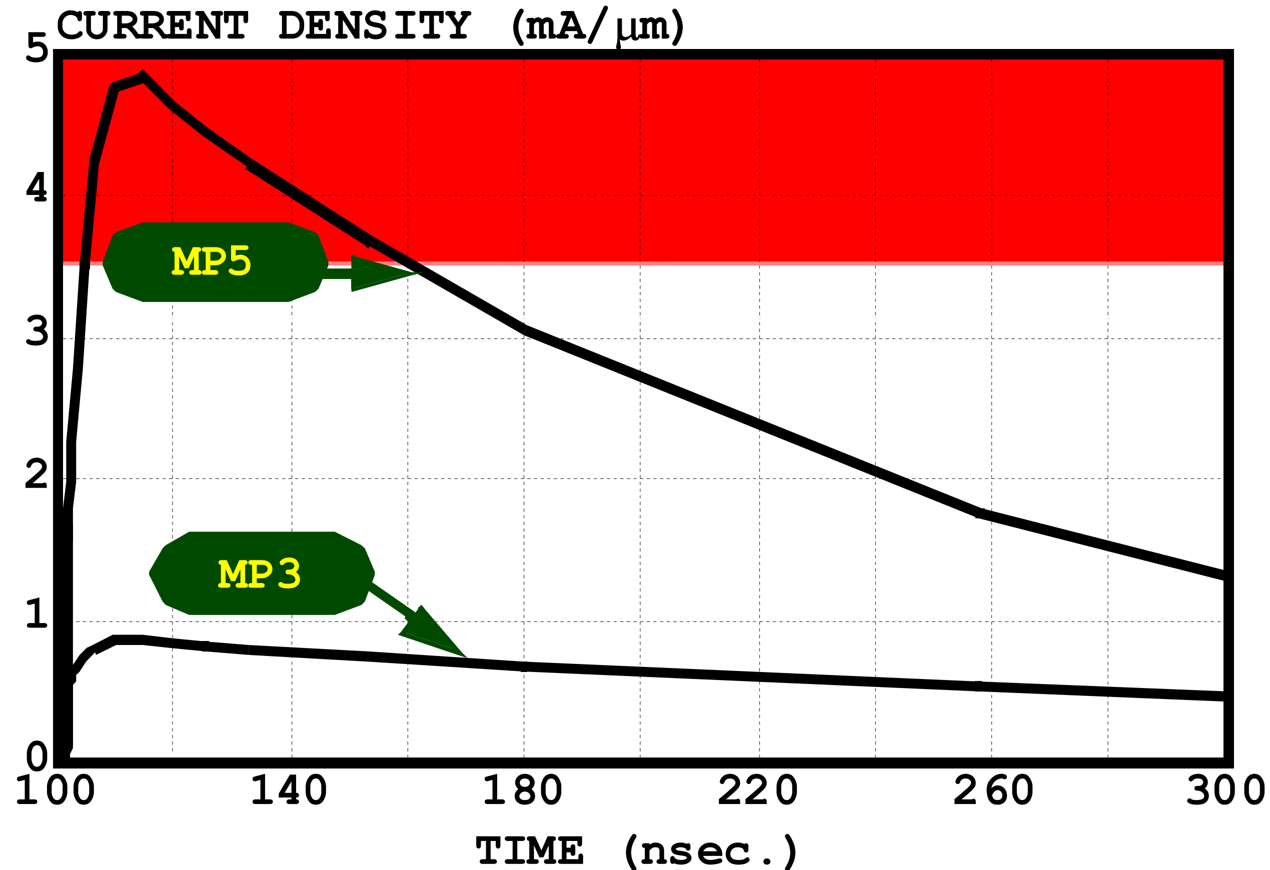
SPICE Simulation Examples

Block Level – Original Design Fails 1,000V HBM



SPICE Simulation Examples

Block Level – Simulation Results – Fails 1,000V



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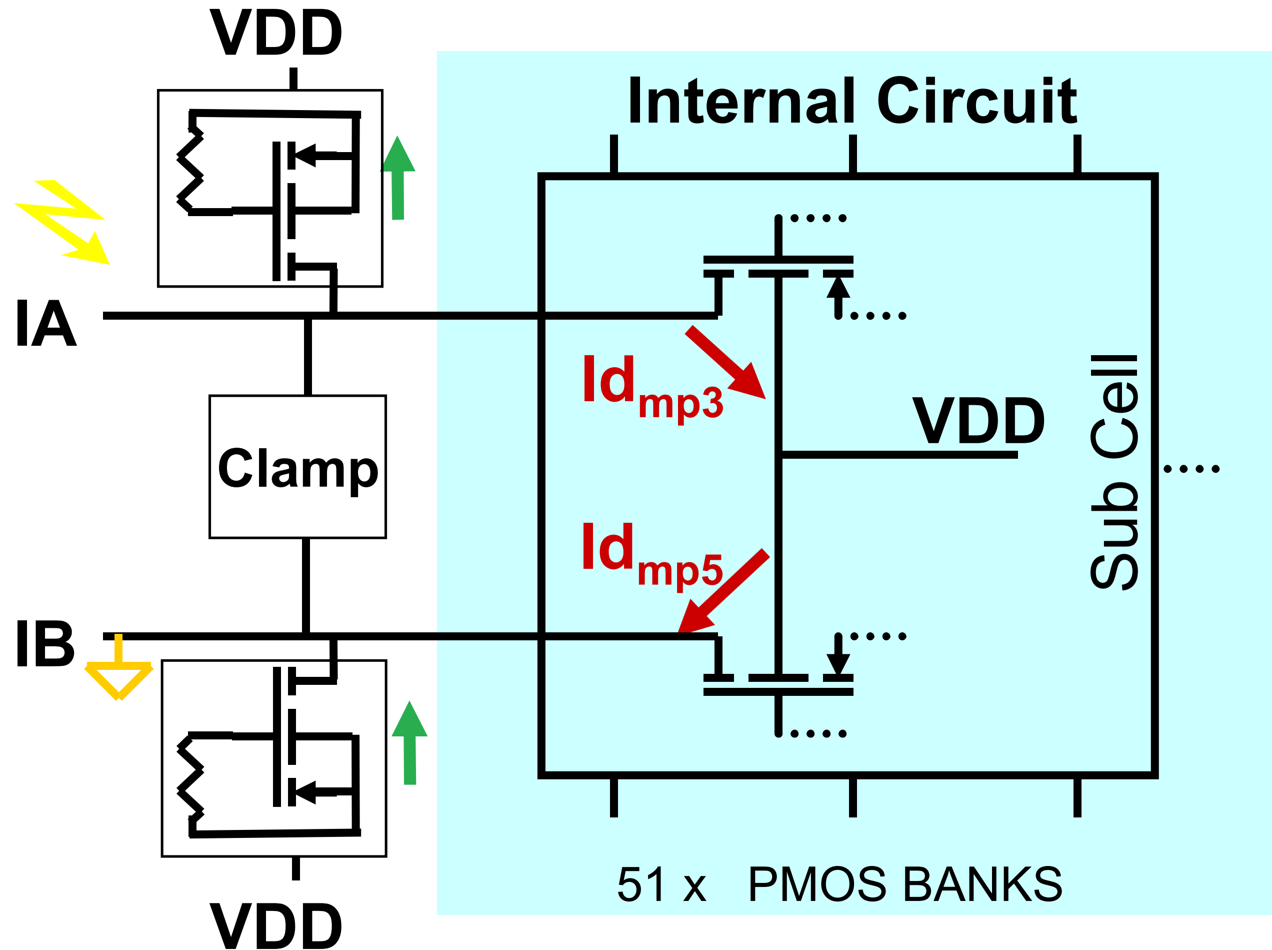
ANALOG DEVICES

SPICE Simulation Examples

Block Level – Revised Design Passes 1,500V HBM



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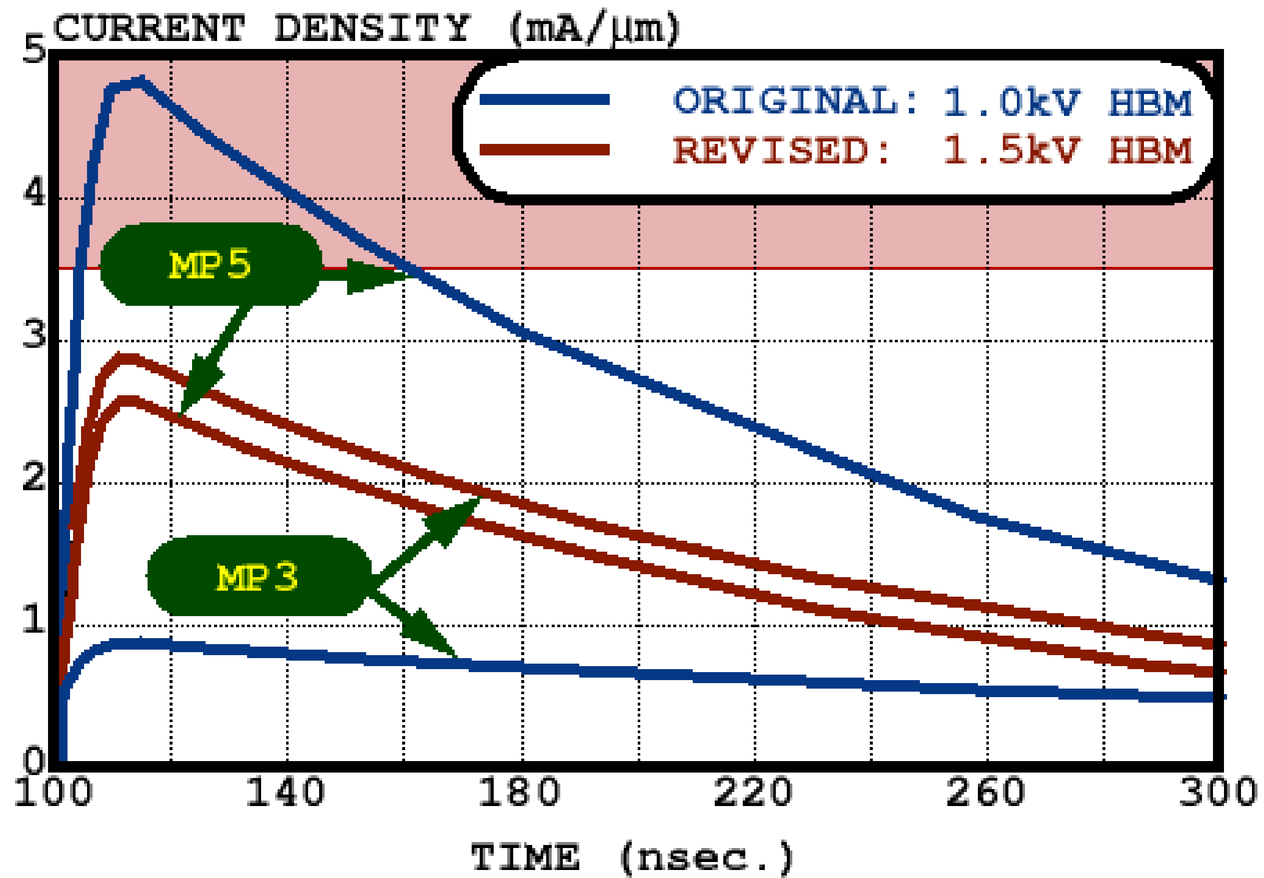
ANALOG DEVICES

SPICE Simulation Examples

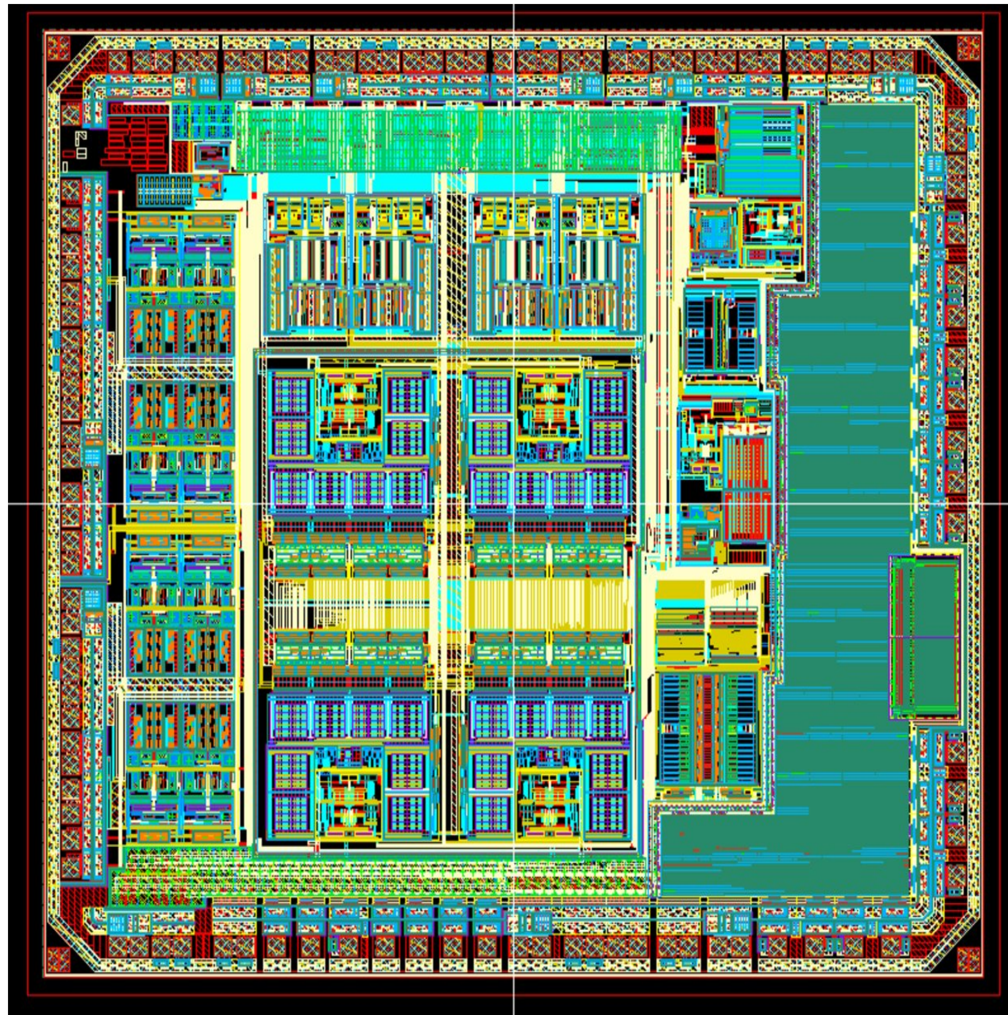
Block Level – Simulation Results



—Analog Devices Proprietary Information—

SPICE Simulation Examples

System Level - A 24-bit Σ-Δ converter



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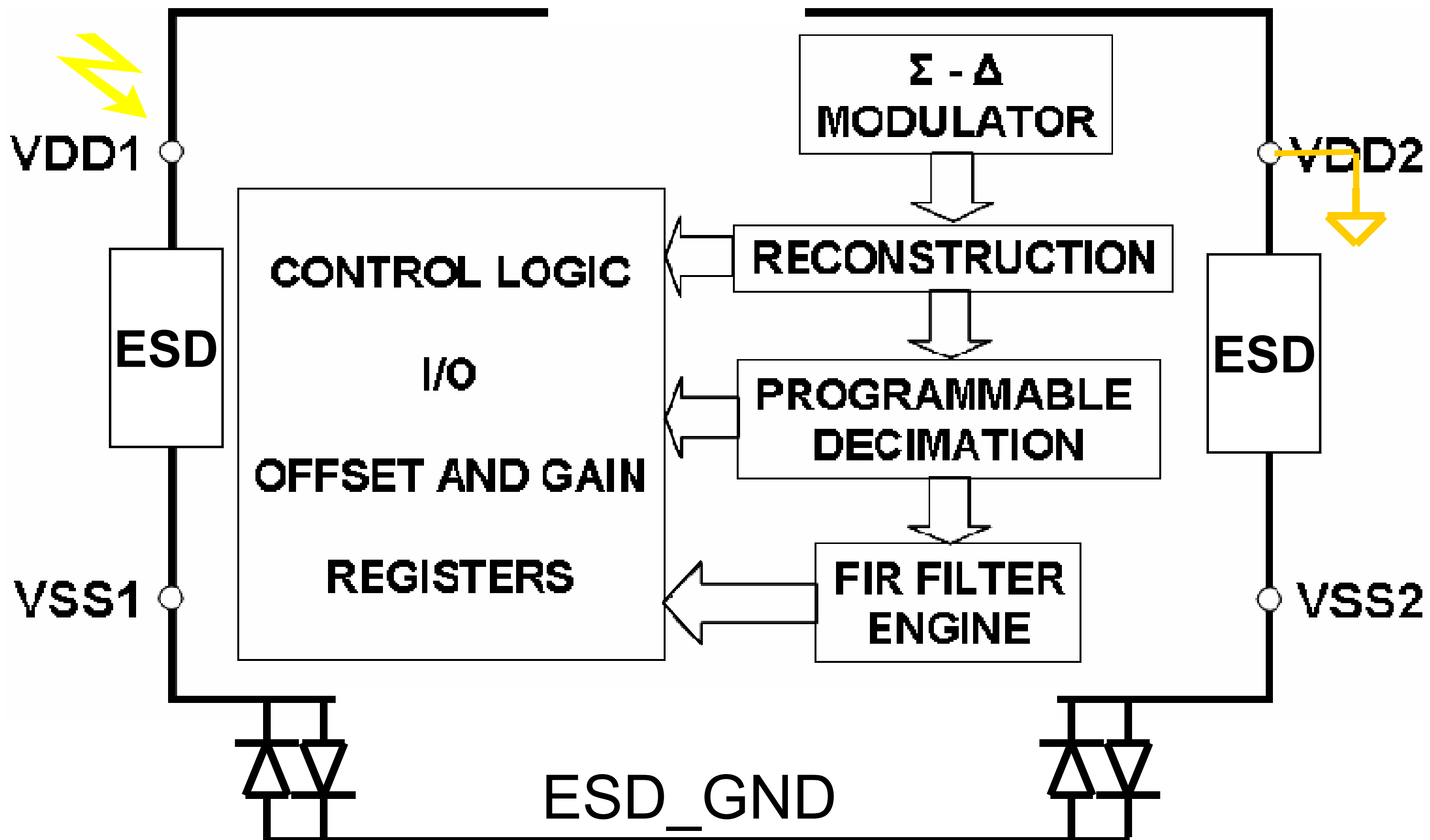
ANALOG DEVICES

SPICE Simulation Examples

System Level - HBM Stress between VDD1 and VDD2



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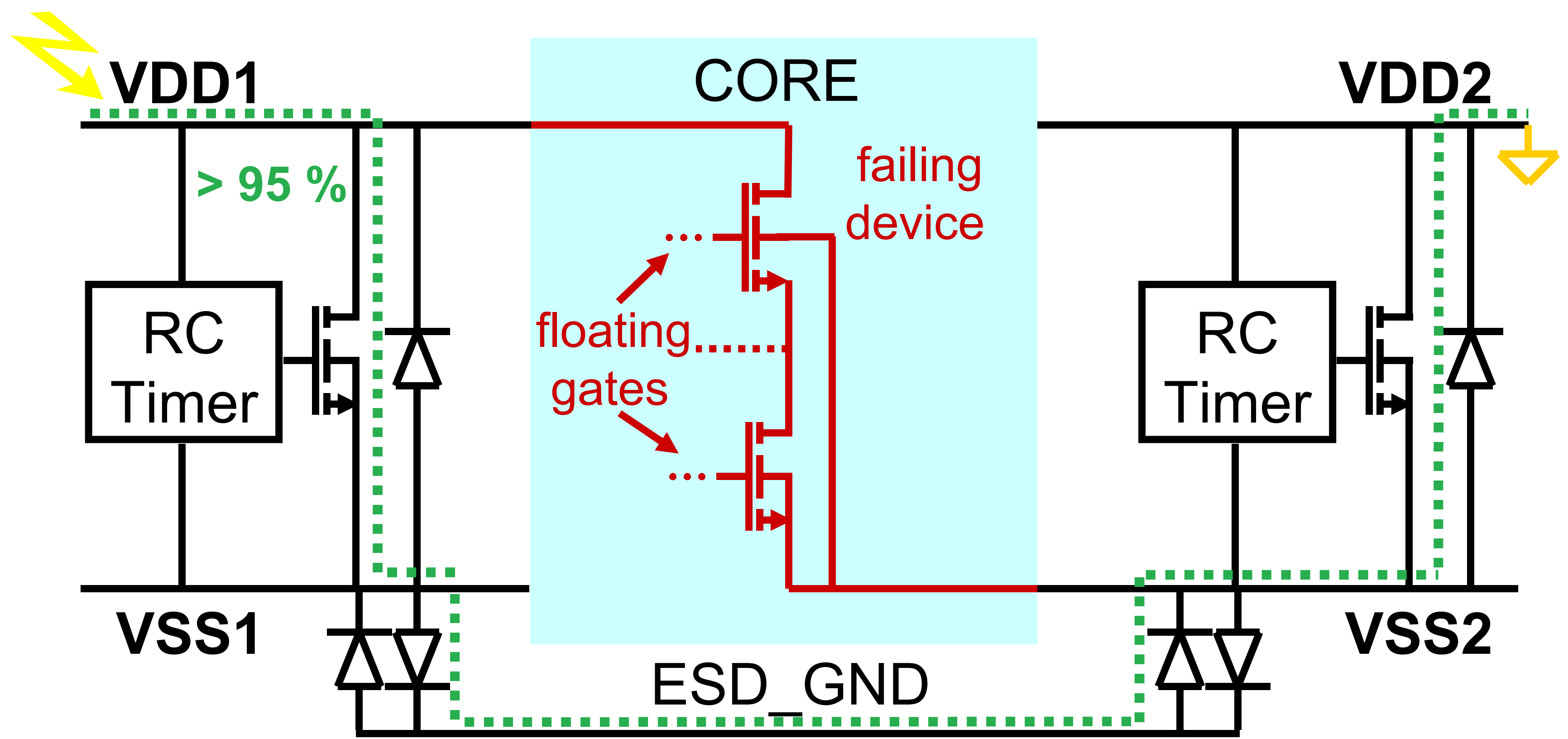
ANALOG DEVICES

SPICE Simulation Examples

System Level – Original Design Fails 700V HBM



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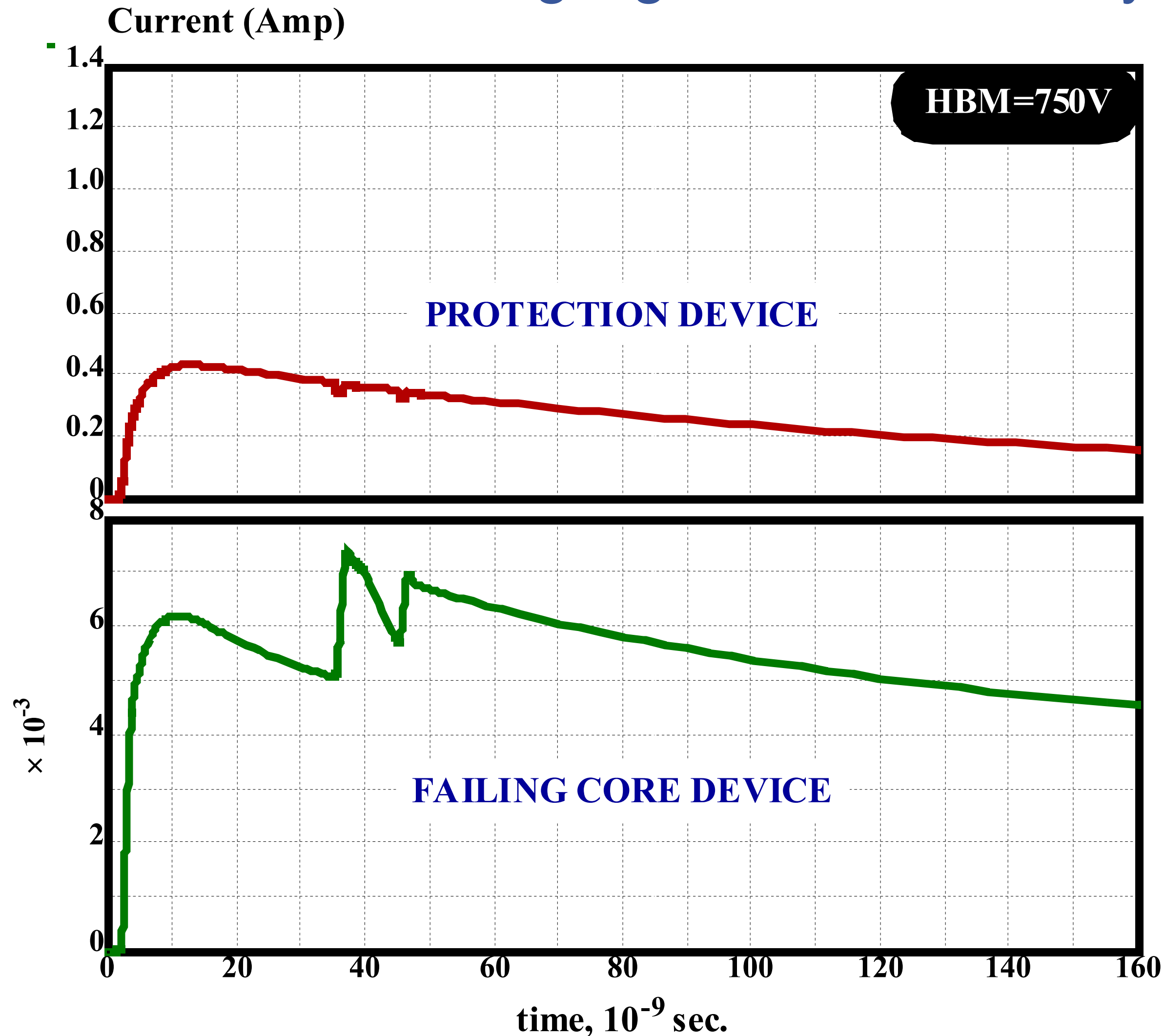
SPICE Simulation Examples

System Level – Simulation Highlights Core Circuitry Failure.



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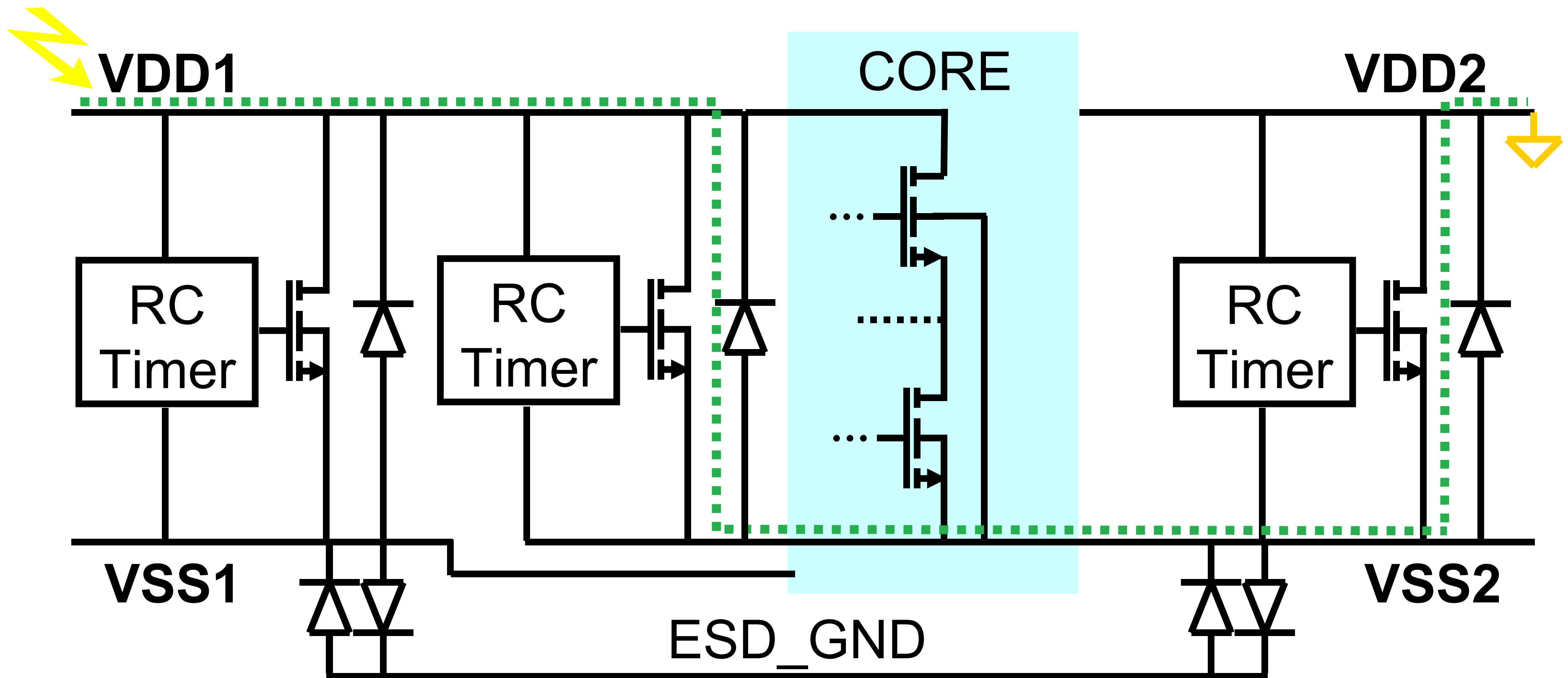
ANALOG DEVICES

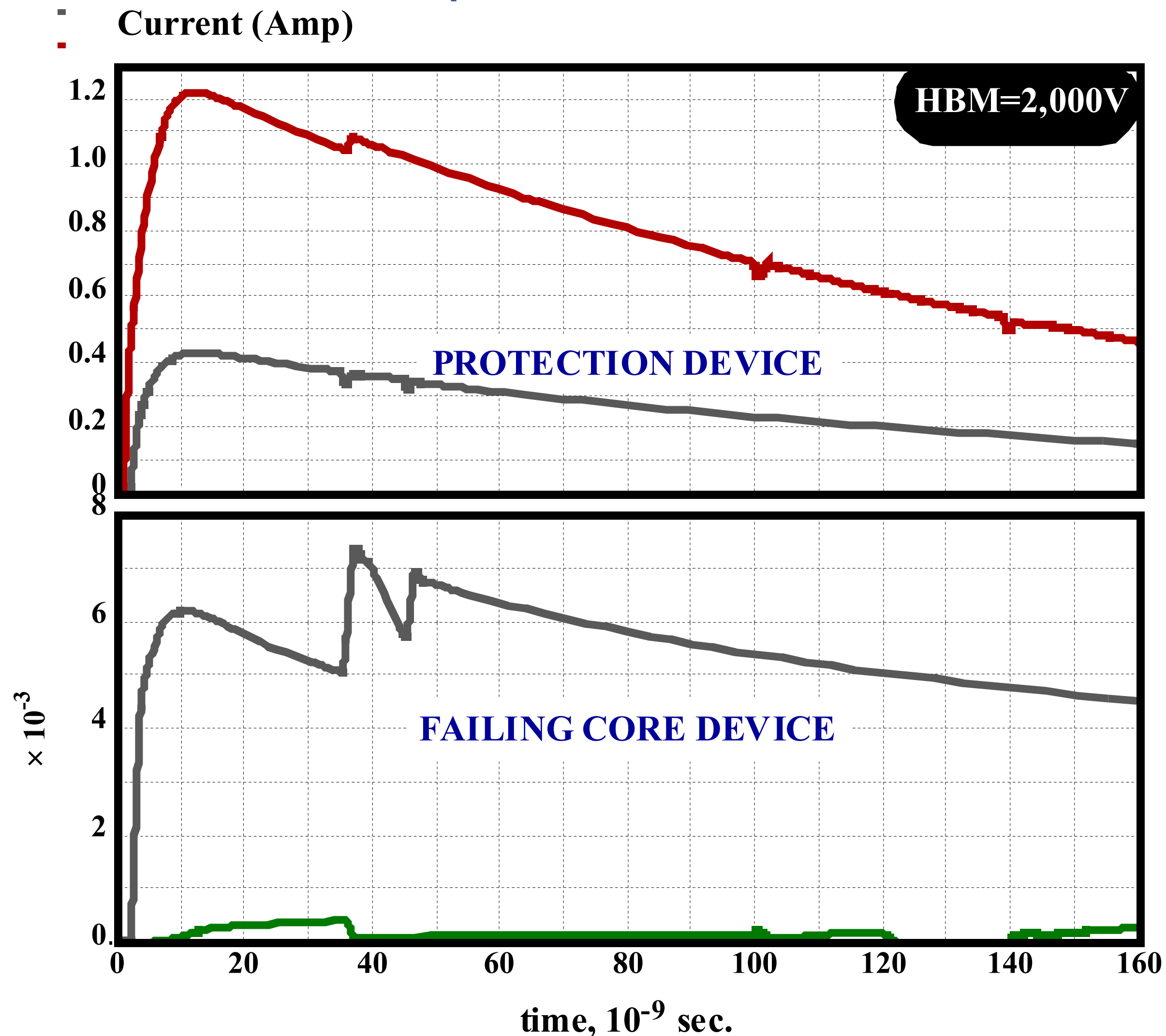
SPICE Simulation Examples

System Level – Revised Design, 2,000V HBM Level Predicted



SPICE Simulation Examples

System Level – Simulation predicts failure above 2,000V HBM



—Analog Devices Proprietary Information—

ANALOG DEVICES

SUMMARY

- ESD is an important product reliability concern.
- Compact Modeling approach for accurate modeling of MOS & SCR devices
  - Uses Industry standard Models
  - Simple Implementation
- Successful SPICE-type circuit simulation of ESD event:
  - Design ESD Protection Cells
  - Predict ESD Performance
  - Confirm and fix known ESD failures

—Analog Devices Proprietary Information—

ANALOG DEVICES

END

—Analog Devices Proprietary Information—