A Succinct Overview of Electron Device Evolution

(Past, present, and future)

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CONTENTS:

- Historical milestones.
- Present tendencies.
- The future.

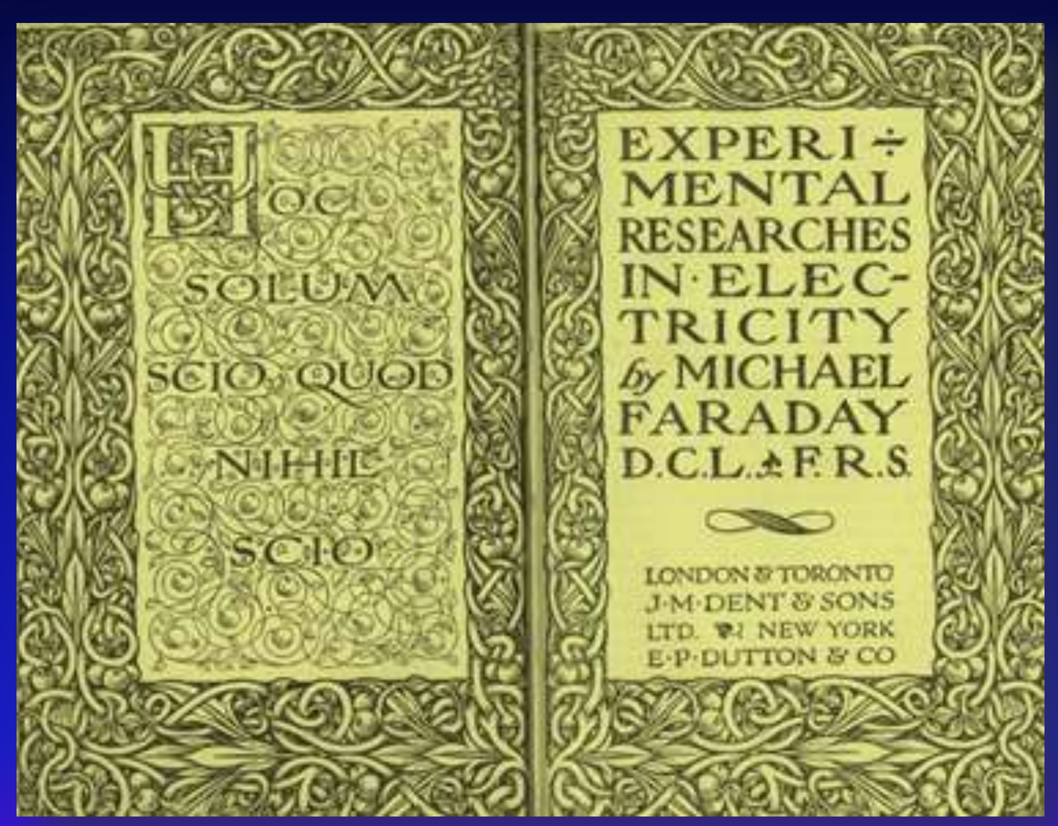
The technological foundation of today's information society, **the Integrated Circuit, is the most complex artifact ever built.**

It is humankind's greatest engineering achievement.

In 2007 the worldwide microelectronics industry produced 900 million transistors for every man, woman, and child on earth – a total of 6×10^{18} transistors.

Source: Semiconductor Industry Association (SIA)

1833: Discovery of semiconductors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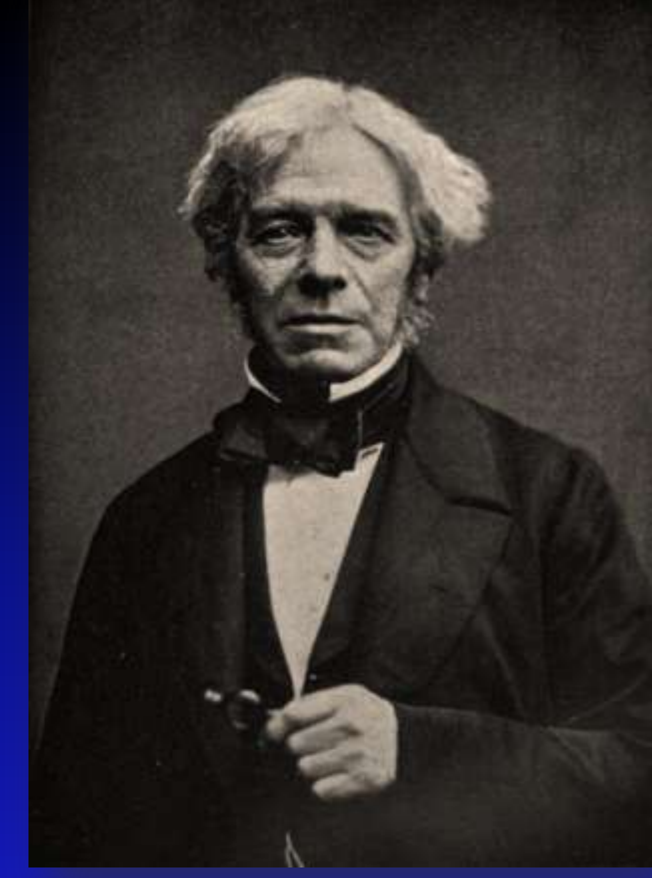
EXPERIMENTAL RESEARCHES IN ELECTRICITY by MICHAEL FARADAY D.C.L. F.R.S.

LONDON & TORONTO J·M·DENT & SONS LTD. NEW YORK E·P·DUTTON & CO



Michael Faraday

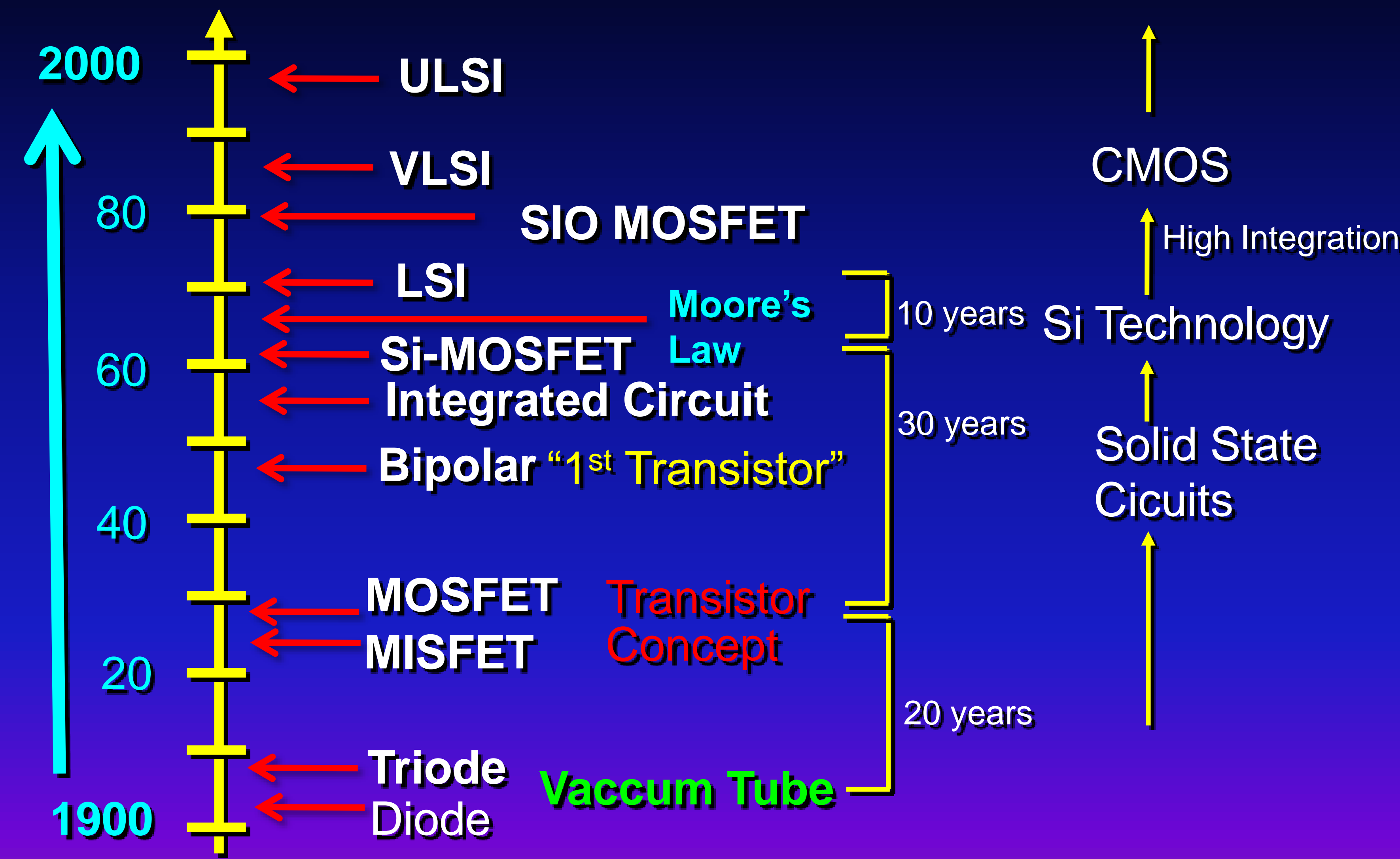
First time a semiconductor's electric property is observed and reported: The increase of Silver Sulfide's conductivity with temperature.

1876: Discovery of the rectifier effect

Karl Ferdinand Braun

The "point contact" rectifier effect is demostrated: When Lead Sulfide ("Galena") is contacted with a fine metallic probe electric current flows easily in one direction but not in the opposite.

A century of evolution

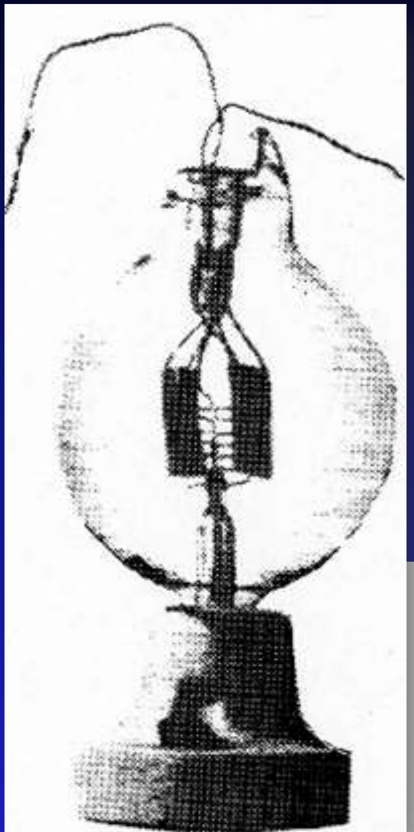


1901: Point-contact semiconductor rectifier is patented as a means for detecting radio signals

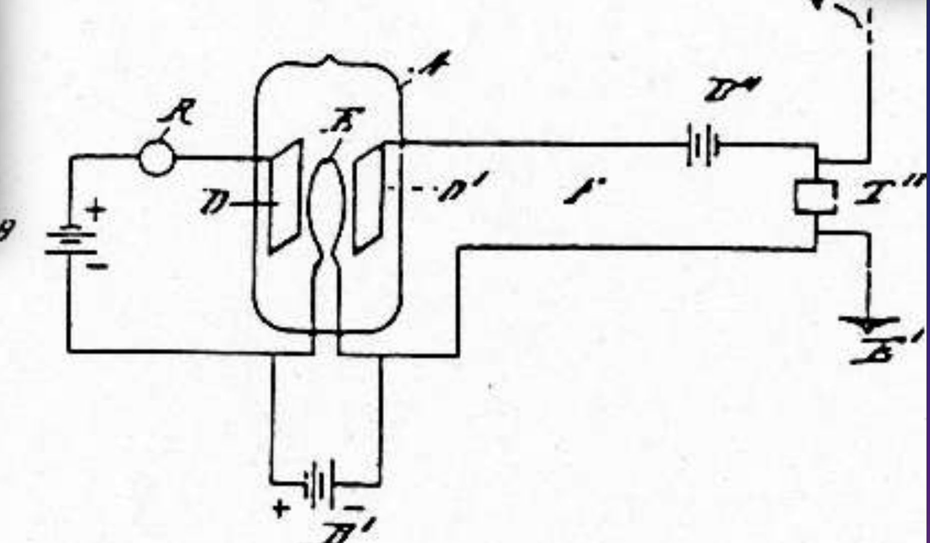
Jagadis Chandra Bose

A point contact "cat's-whisker" Lead Sulfide (Galena) crystal rectifier is used to detect millimeter electromagnetic waves. (US Patent 755,840)

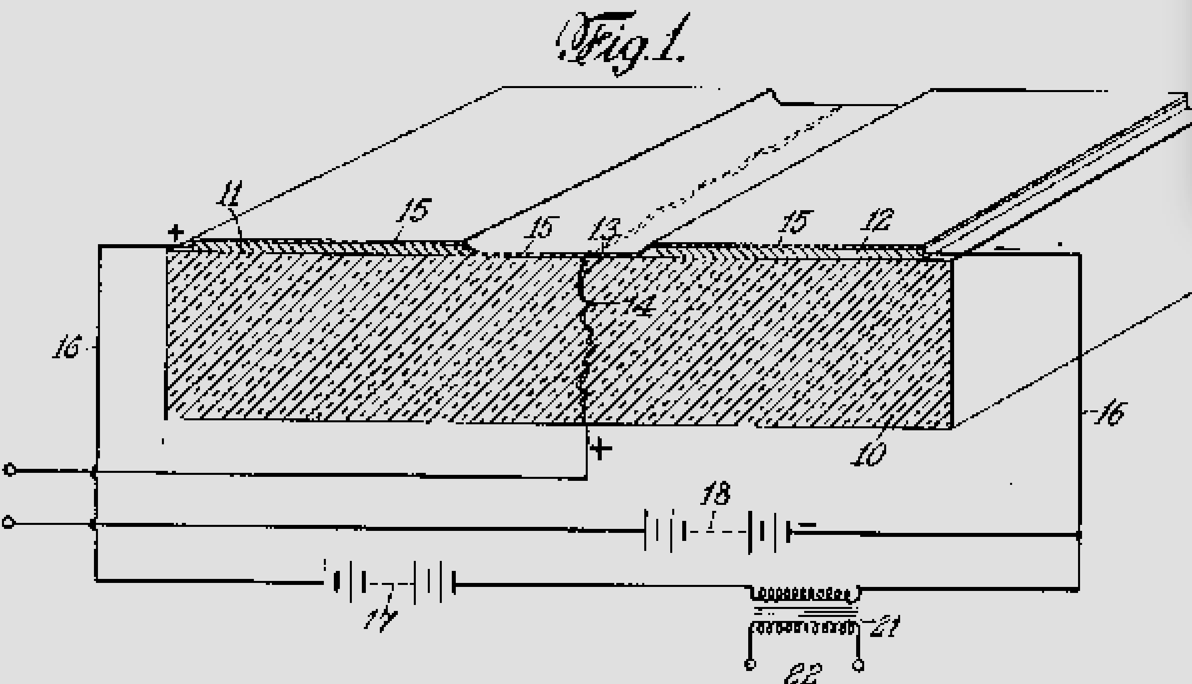
1906: Vaccum Tube - Triode



Lee De Forest



1926: Concept of Field Effect Transistor



Julius E. Lilienfeld

1926: Field Effect Transistor (MOSFET)

Patented Mar. 7, 1933 1,900,018

UNITED STATES PATENT OFFICE

JULIUS EDGAR LILIENFELD, OF BROOKLYN, NEW YORK

DEVICE FOR CONTROLLING ELECTRIC CURRENT

Application filed March [illegible], [illegible]. Serial No. [illegible].

J. E. LILIENFELD

DEVICE FOR CONTROLLING ELECTRIC CURRENT

Filed March 28, 1928 3 Sheets-Sheet 1

Fig. 1.

Cu_2S

S

D

Al_2O_3

Al

G

CTS

12 Copper Sulfide

11 Aluminum Oxide

10 Aluminum

Fig. 2.

12 Copper Sulfide

11 Aluminum Oxide

10 Aluminum

S

D

G

J.E. Lilienfeld

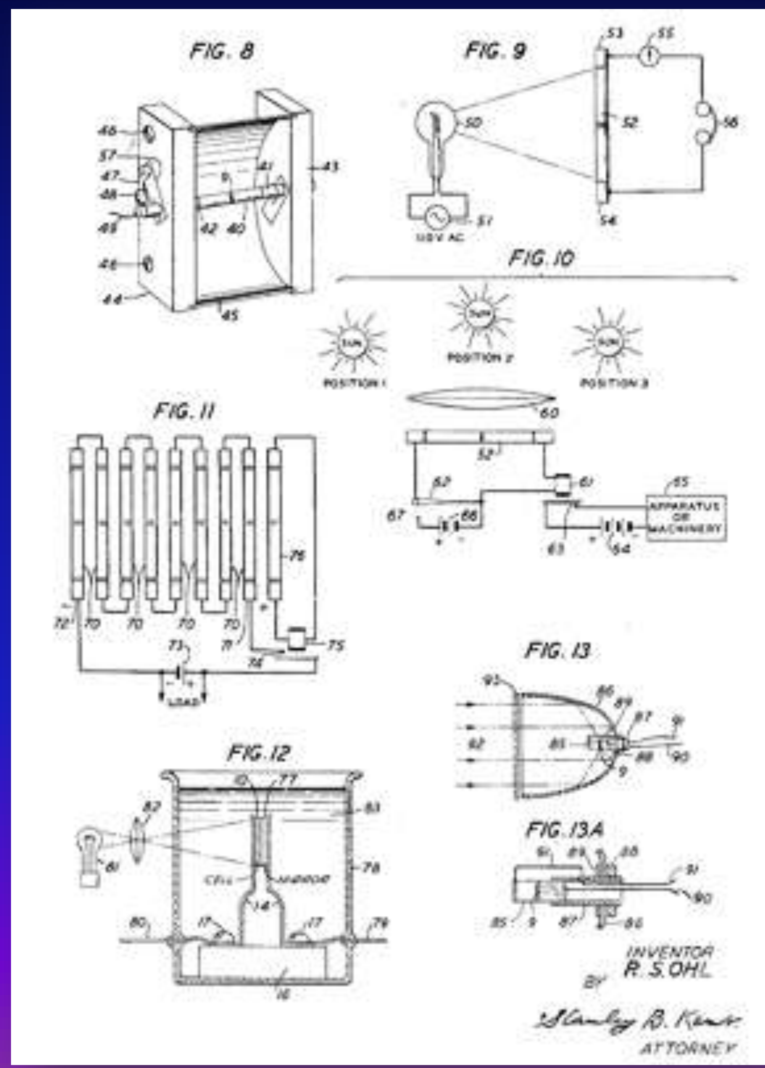
1931: First quantum mechanical model of semiconductor behavior

Alan Wilson

Wilson, A. H.

1. "The Theory of Electronic Semi-Conductors," *Proceedings of the Royal Society of London. Series A,* Vol. 133, No. 822, Oct. 1, 1931, pp. 458-491
2. "The Theory of Electronic Semi-Conductors II," in Vol. 134, No. 823, Nov. 3, 1931, pp. 277-287

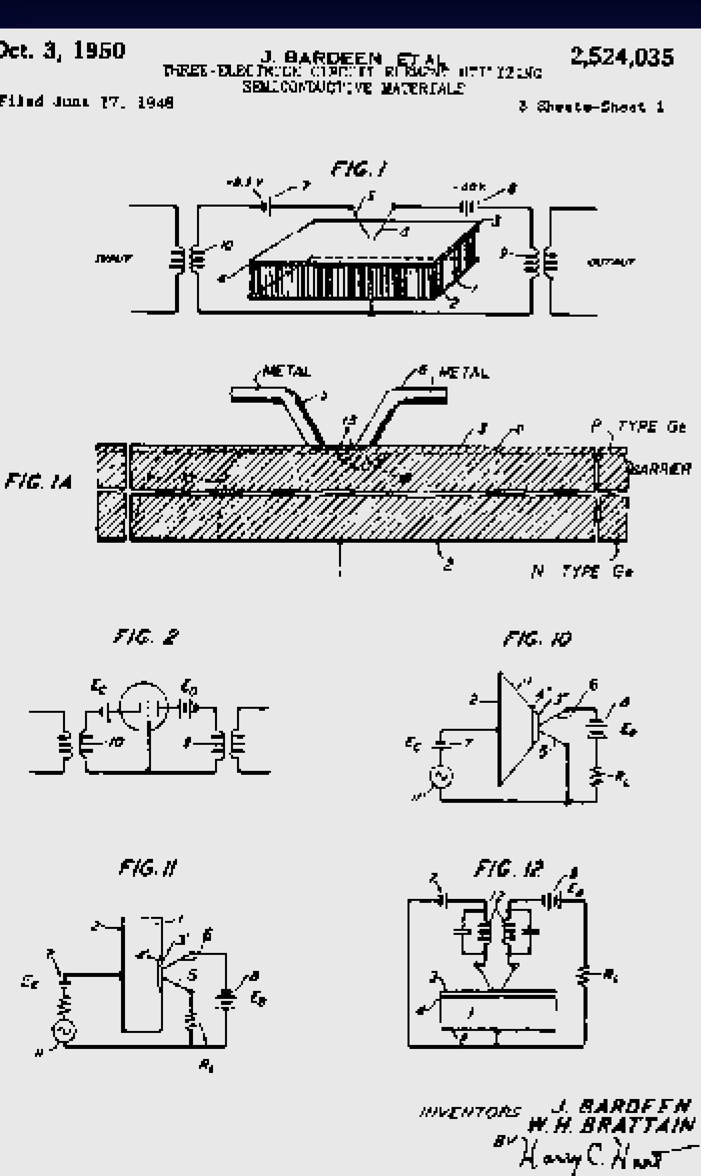
1940: Silicon “p-n” junction diode & modern solar cell



Russell Ohl

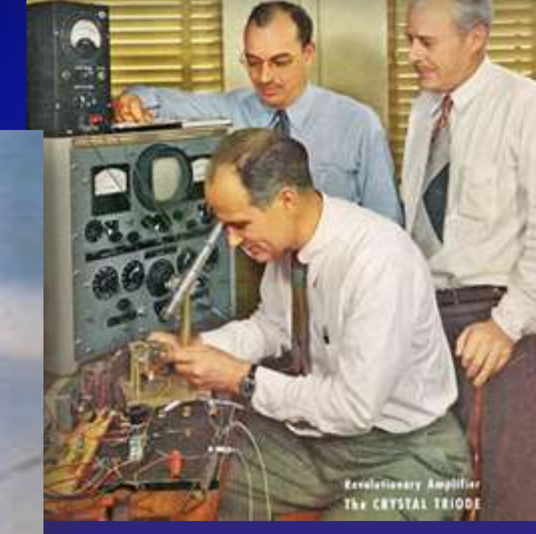
1940: ENIAC Computer

1947, 1948: Bipolar Transistor



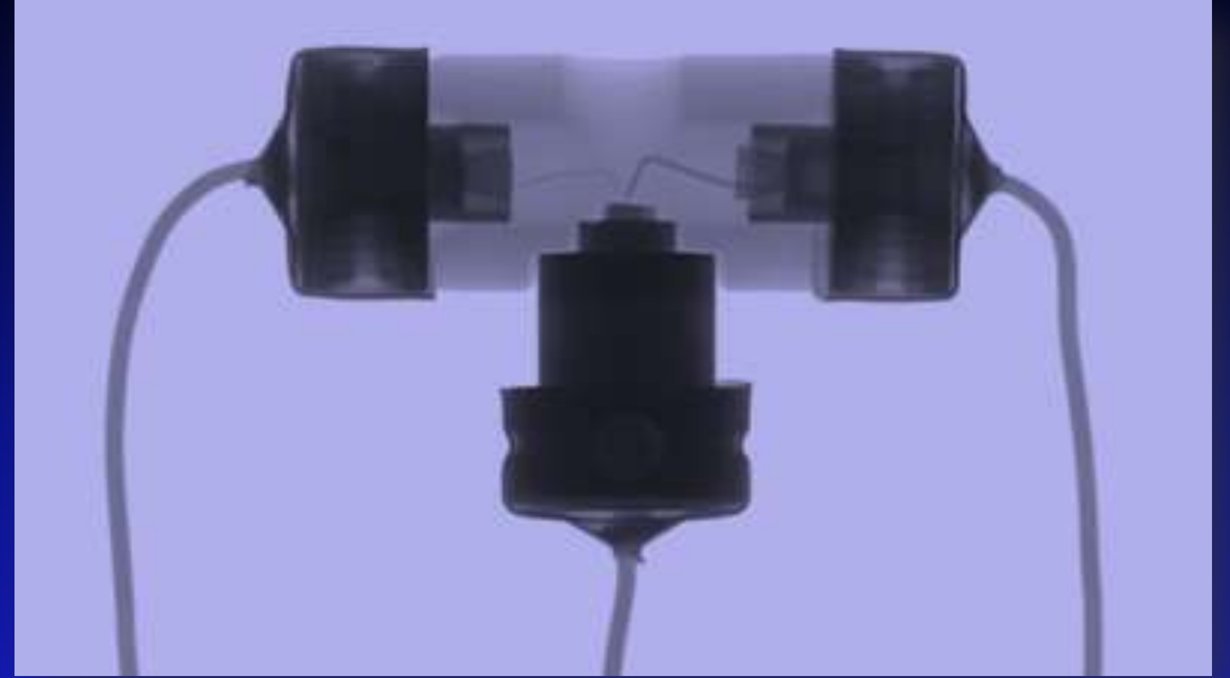
(point-contact)

J. Bardeen,
W. Bratten,
W. Shockley
(Bell Labs)



1st Transistor ?

1948: The "transistron"



"brilliante réalisation de la recherche française."

60 years ago !

Compagnie des Freins et Signaux

Herbert Mataré

Heinrich Welker

1st point-contact germanium transistor ?

1948: Germanium Bipolar Transistor

Bell Labs
"Type A"
germanium
point-contact
transistor

1953: World's first transistor radio

Built around 4 point-contact transistors made by Germany's Intermetall, founded in 1952 by Mataré.

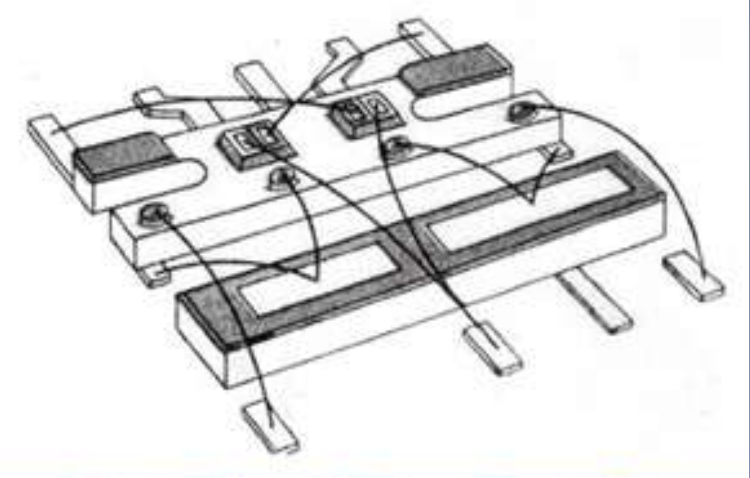
1954: First Commercial Si Bipolar Transistor

Texas Instruments

1952-1956: Introduction of diffused junction

Ref: Tanenbaum, M. and Thomas, D. E. "Diffused Emitter and Base Silicon Transistors." *Bell System Technical Journal,* Vol. 35 (January 1956) pp. 1–22.

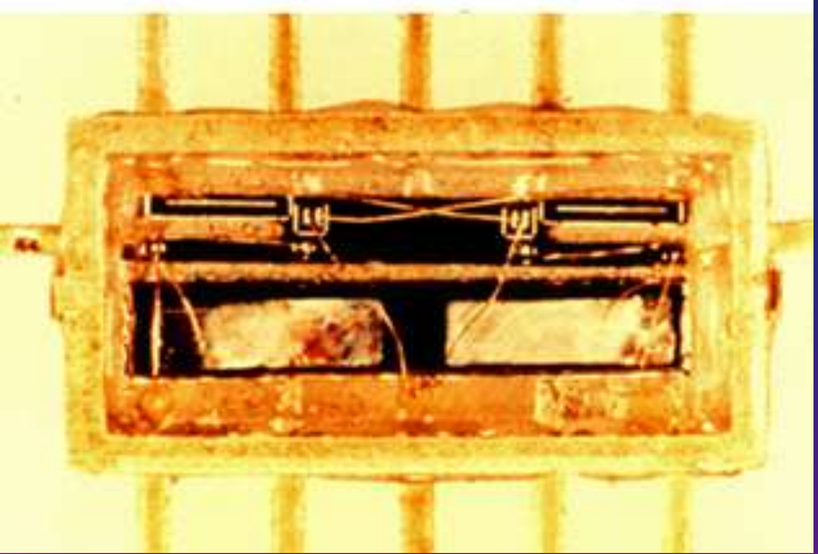
1958: First Integrated Circuit

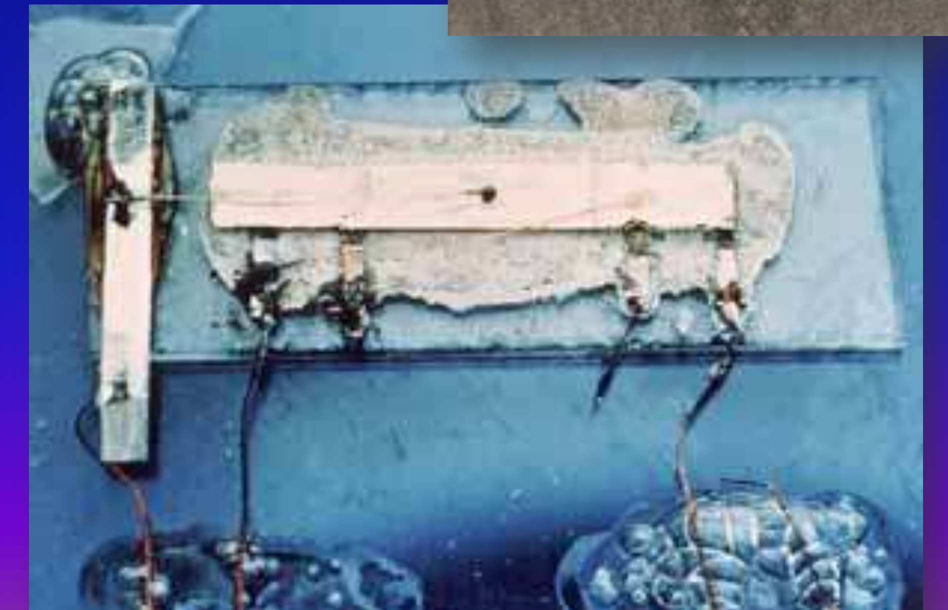


half a century ago !

Jack S. Kilby

(Texas Instruments)





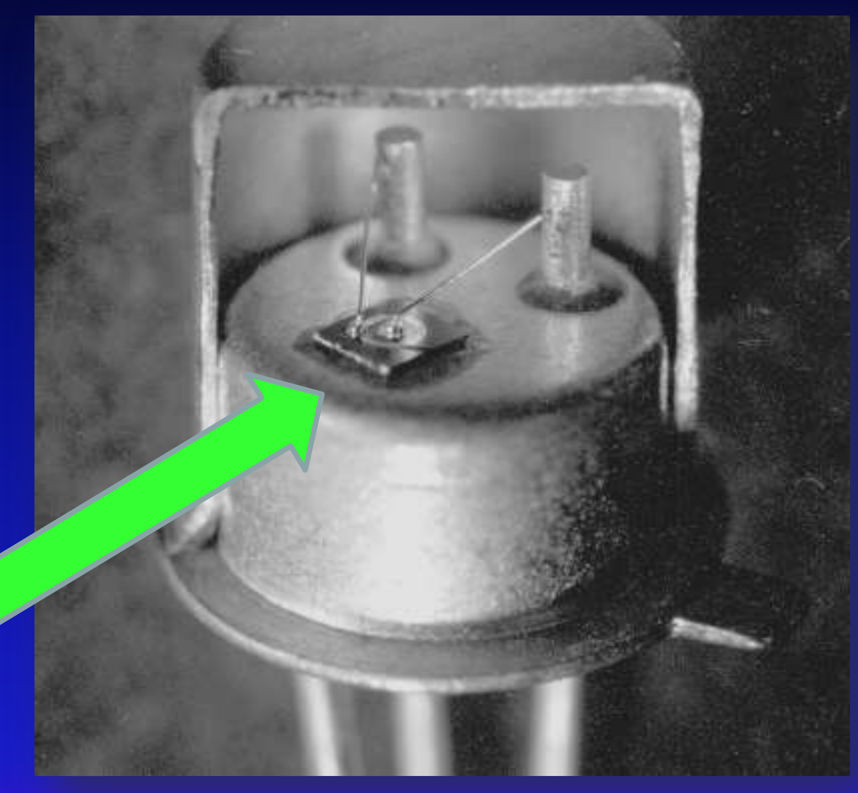
1959: SiO_2 passivation

The Traitorous Eight, according to Shockley

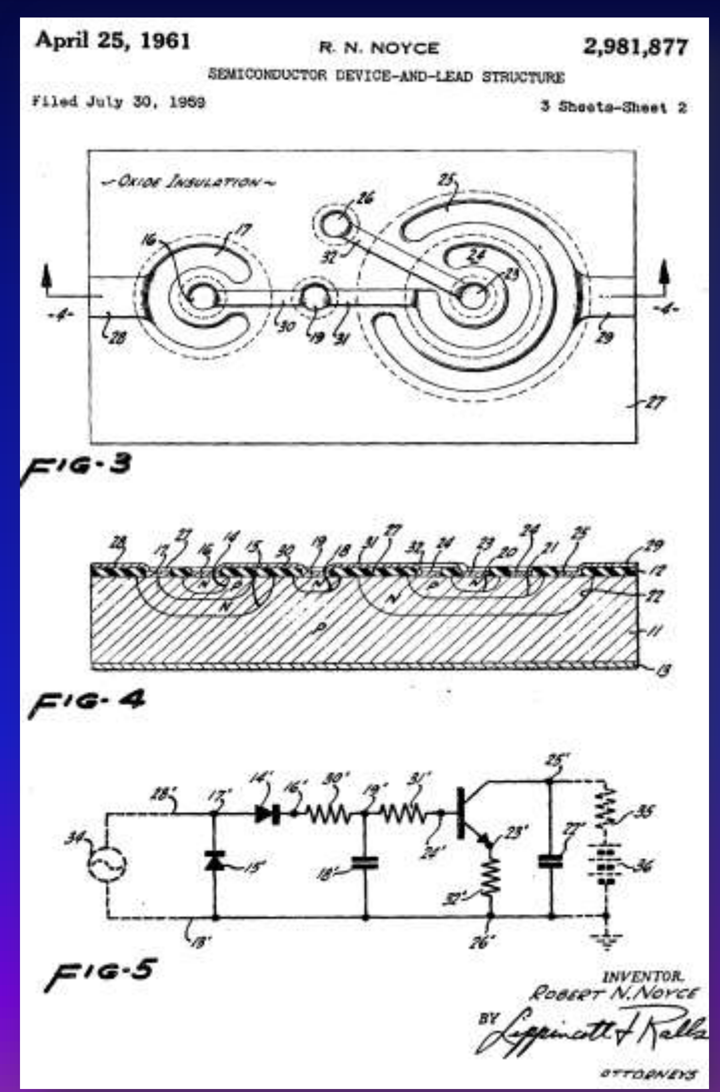
Ref: The Silicon Dioxide Solution, *IEEE Spectrum*, vol. 44 (INT), n. 12, December 2007, p.44-50.

1959: First Commercial “Planar” Si Bipolar Transistor (2N1613)

Fairchild Semiconductor



1959: Idea of "Planar" Integrated Circuit


April 25, 1961 R. N. NOYCE 2,981,877

SEMICONDUCTOR DEVICE-AND-LEAD STRUCTURE

Filed July 30, 1959 3 Sheets-Sheet 2

Robert N. Noyce

Fairchild Semiconductor.

1959: Metal Oxide Semiconductor Field Effect Transistor

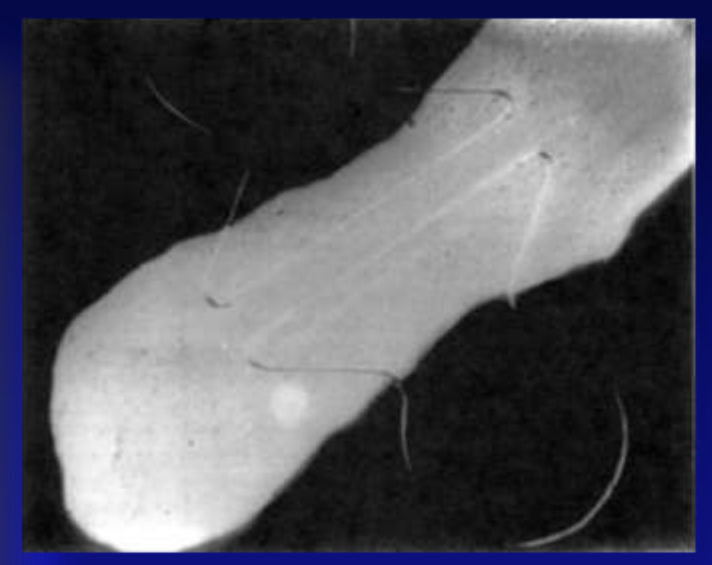
Aug. 27, 1963 DAWON KAHNG 3,102,230

ELECTRIC FIELD CONTROLLED SEMICONDUCTOR DEVICE

Filed May 31, 1960

FIG. 1A

FIG. 1B



D. Kahng
M. Atalla

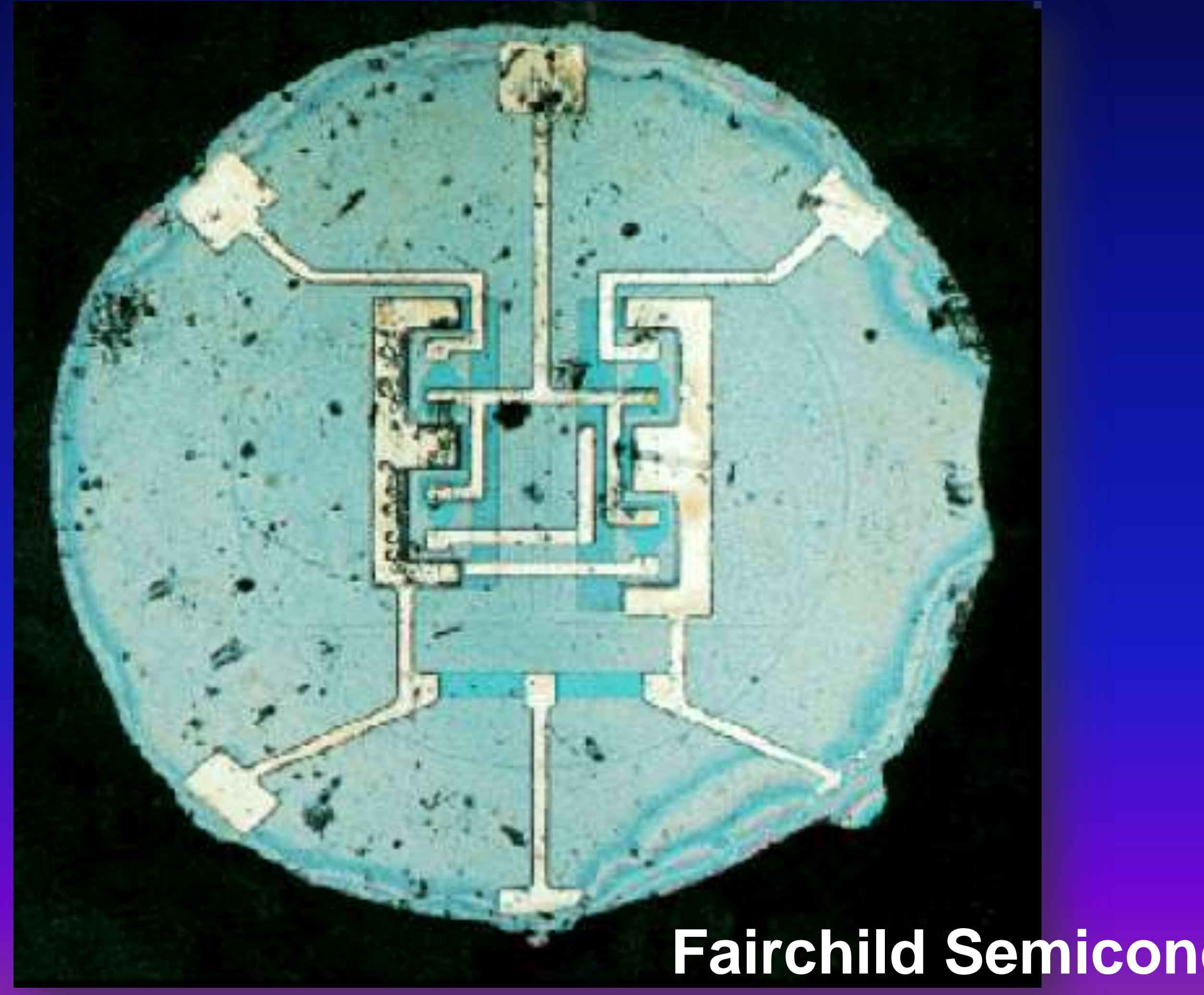
Bell Labs.

1960: Fabrication of first MOSFET

D. Kahng
M. Atalla

Bell Labs.

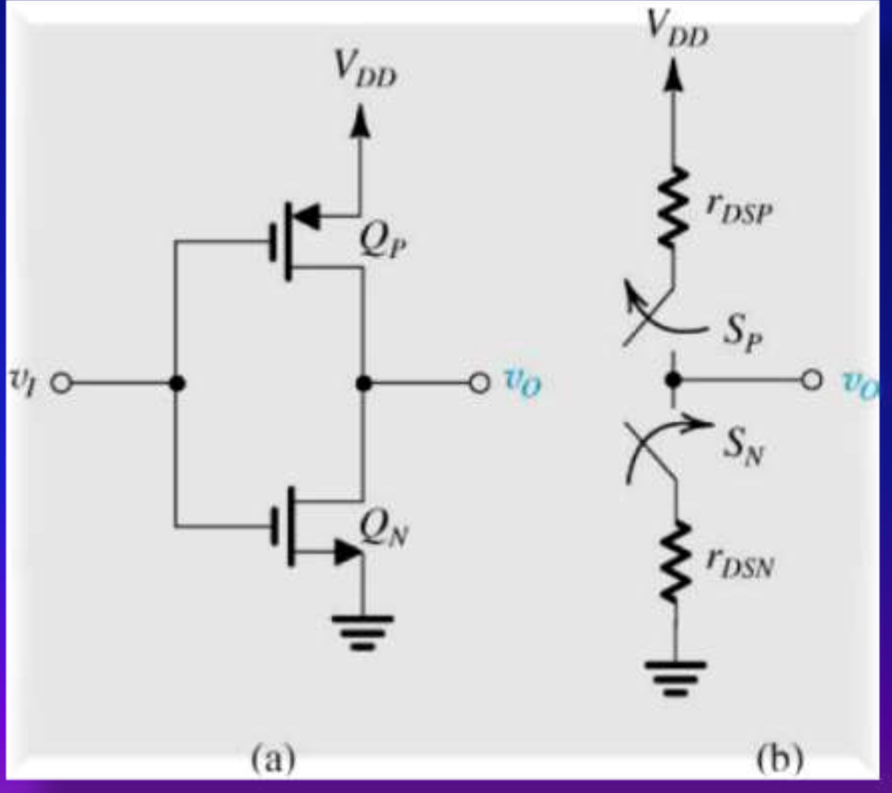
1961: First "Planar" Integrated Circuit in production.



Fairchild Semiconductor.

1963: CMOS Circuit

Frank Wanlass



Dec. 5, 1967 F. M. WANLASS 3,356,858

LOW STAND-BY POWER COMPLEMENTARY FIELD EFFECT CIRCUITRY

Filed June 18, 1963 3 Sheets-Sheet 1

Fig. 1

DRAIN GATE SOURCE

Fig. 1A

INVENTOR.
FRANK M. WANLASS
BY
ATTORNEYS

1965: First projection of Integrated Circuits density

MOORE's Law

LOG2 OF THE NUMBER OF COMPONENTS PER INTEGRATED FUNCTION

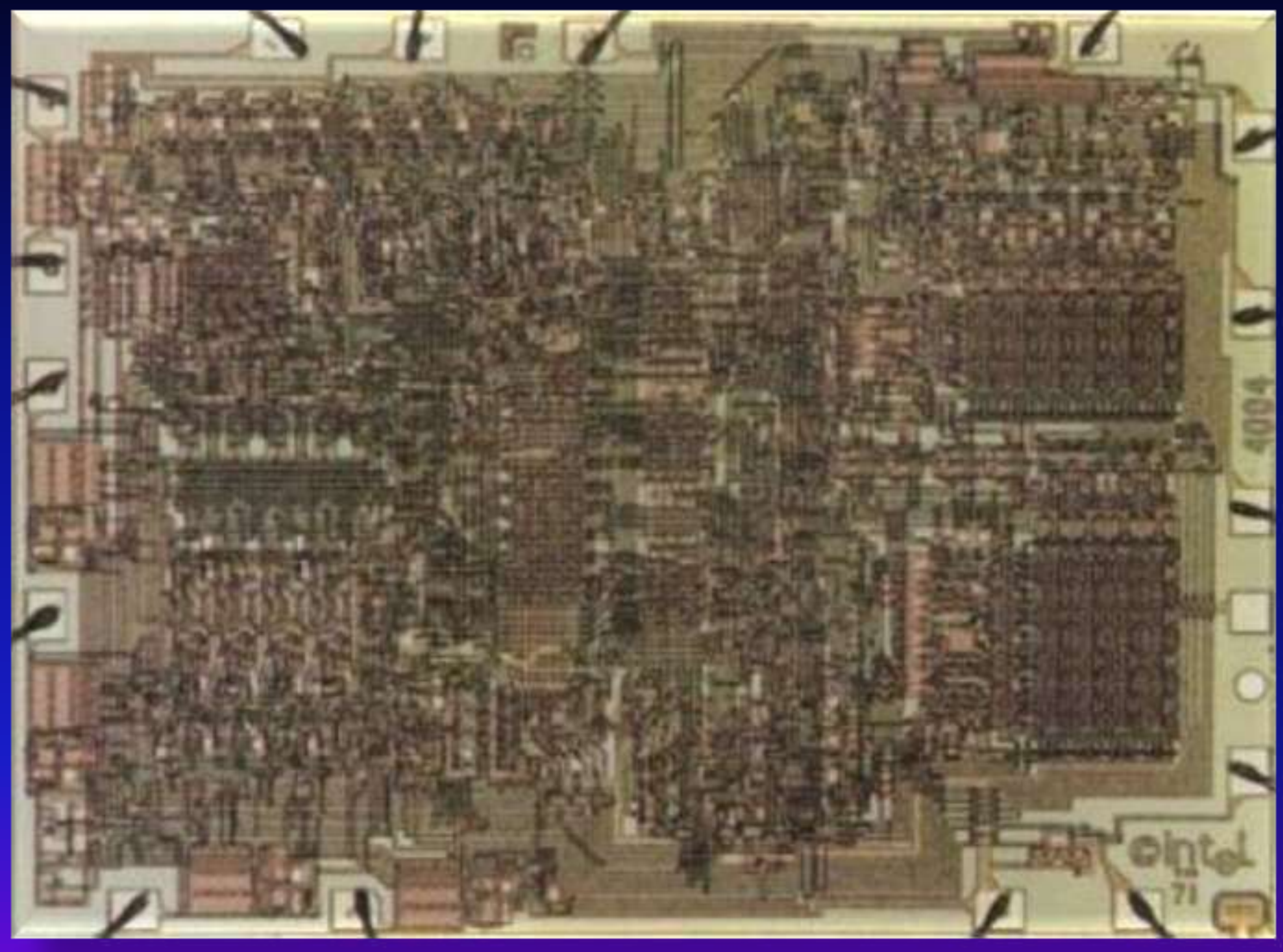
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

1959 1960 1961 1962 1963 1964 1965 1966 1967 1968 1969 1970 1971 1972 1973 1974 1975

YEAR

Ref: Gordon E. Moore, *Electronics*, vol. 38, n. 8, April 19th, 1965

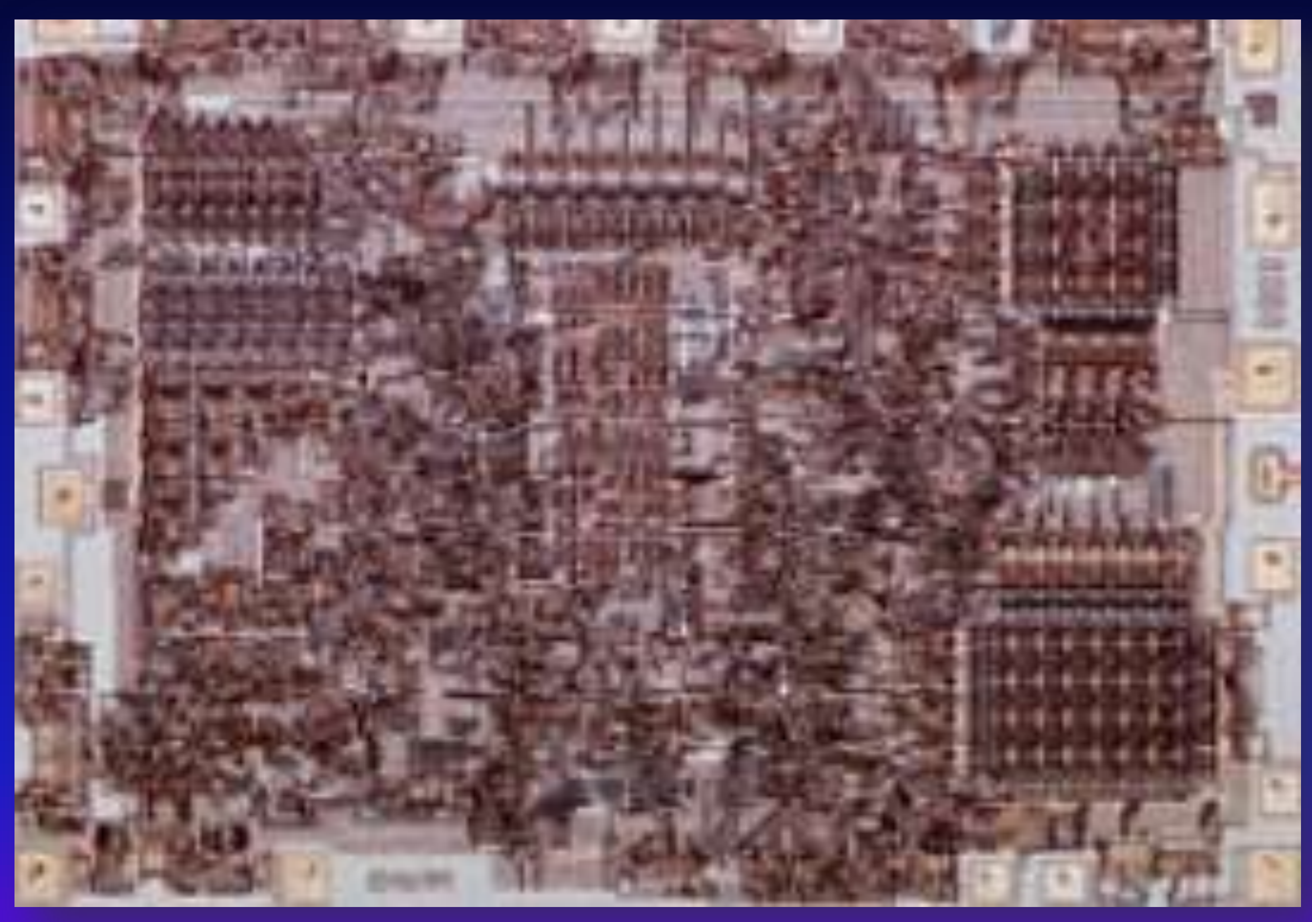
1971: First generation of LSI



Intel 4004

2,300 transistors
Line width: 10µm   Clock speed: 108 kHz

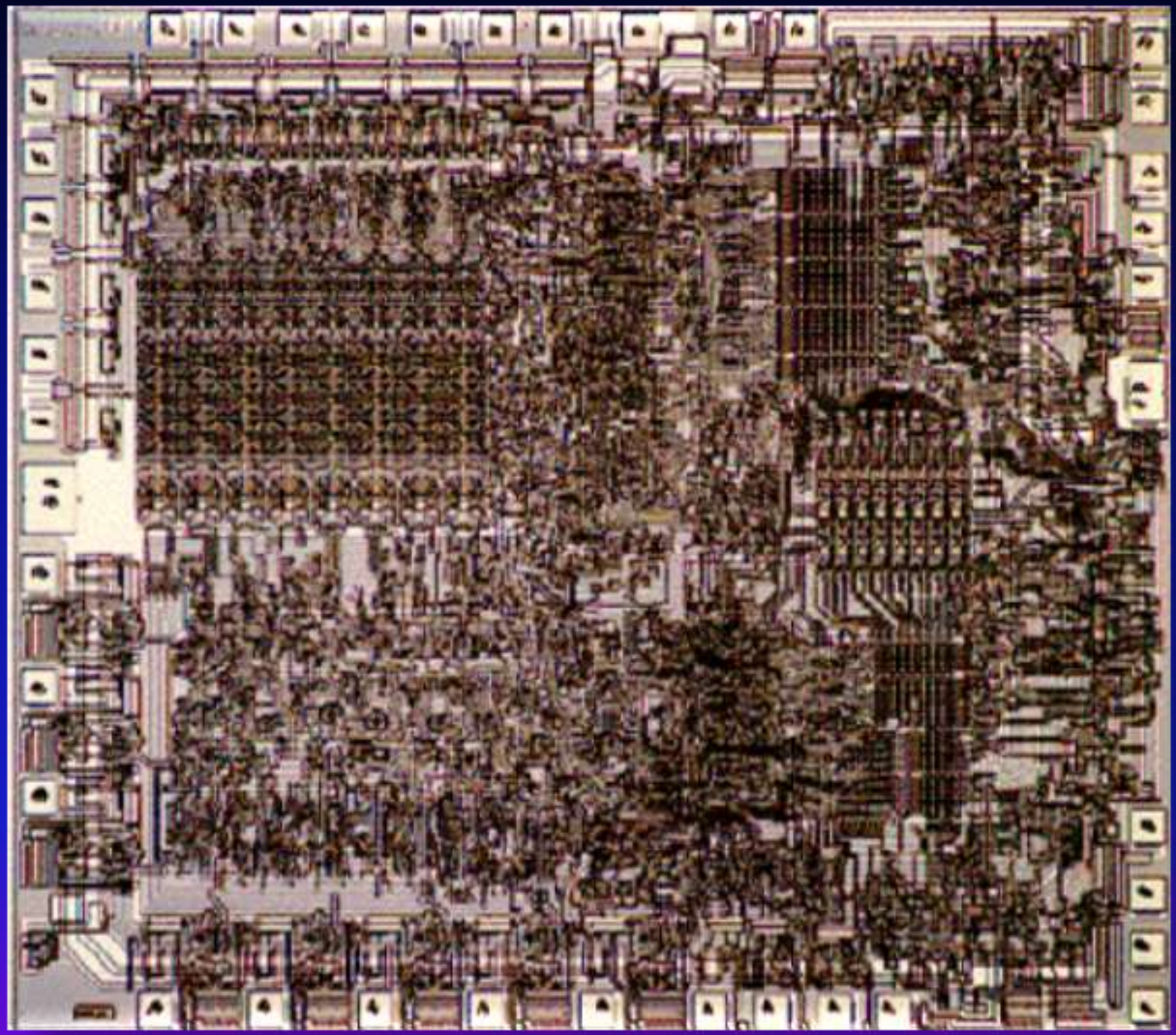
1972: First generation of LSI



Intel 4004

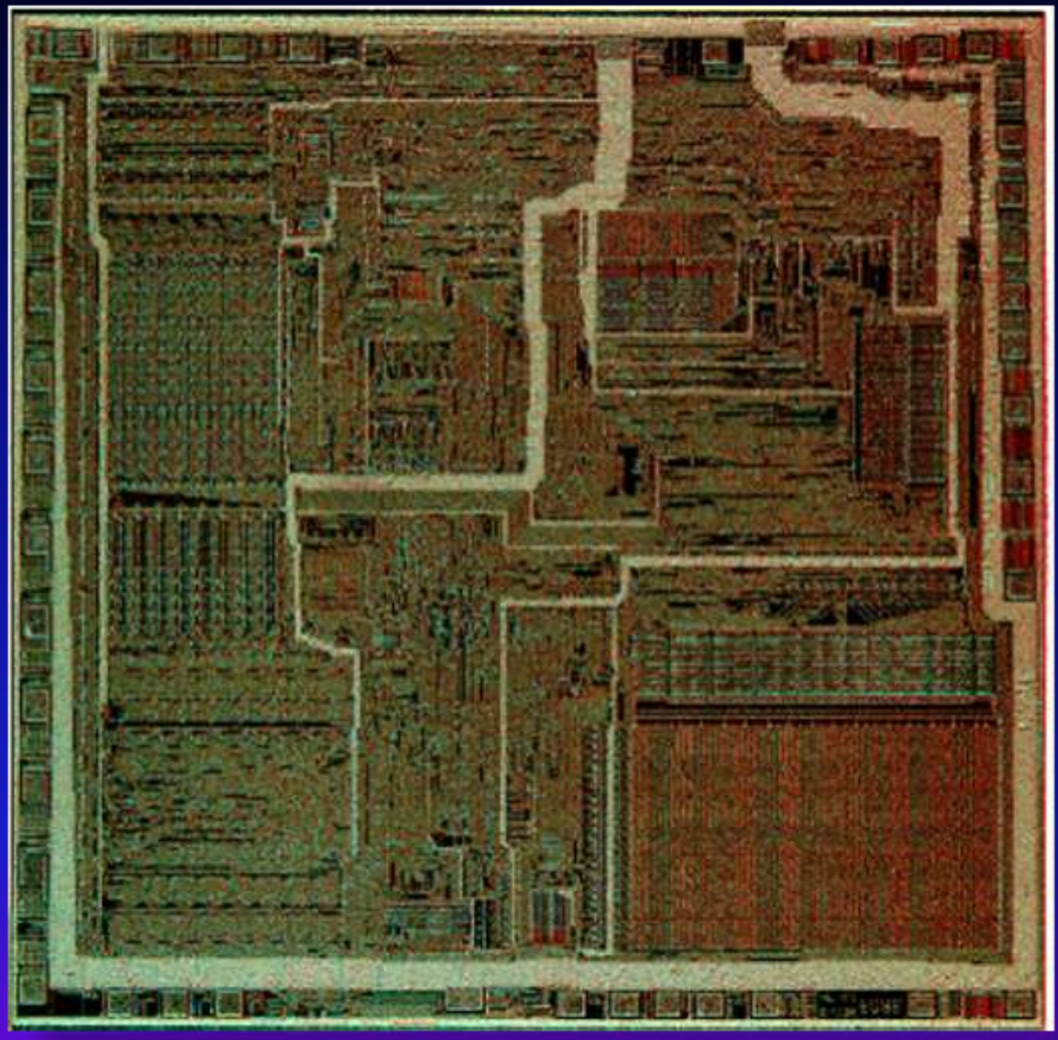
3,500 transistors
Line width: 10µm   Clock speed: 500-800 kHz

1974: Intel 8080



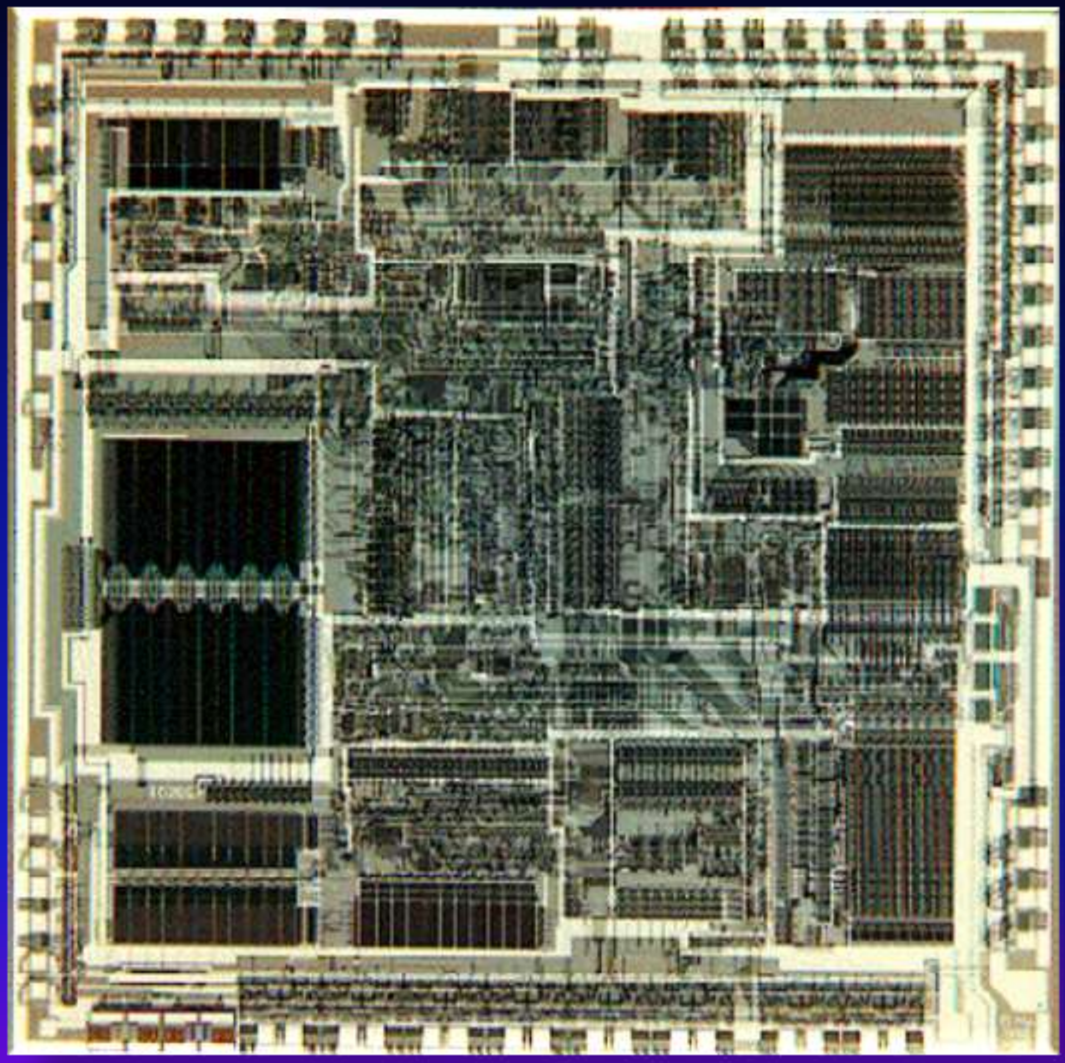
4,500 transistors
Line width: 6μm   Clock speed: 2 MHz

1978: Intel 8086



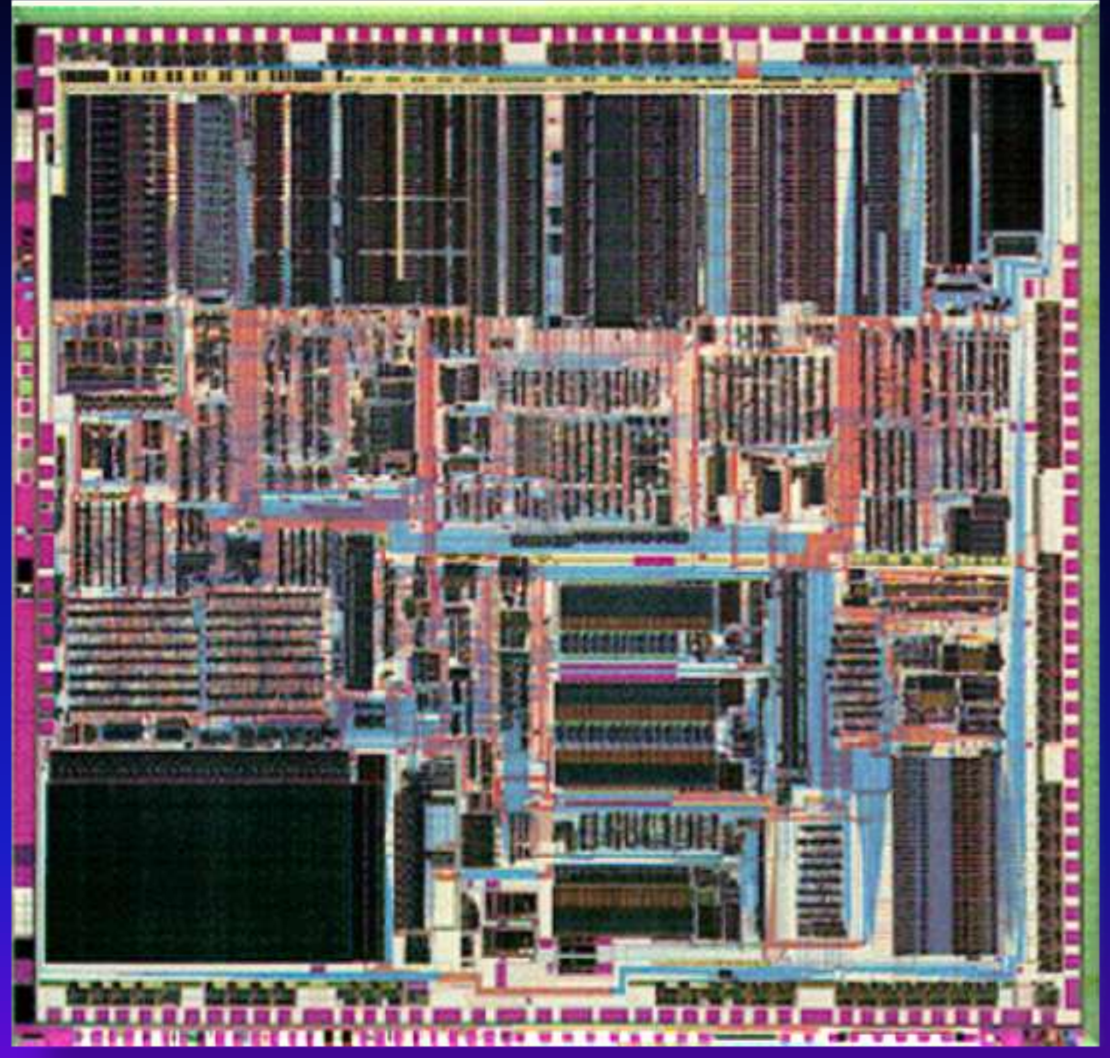
29,000 transistors
Line width: 3μm Clock speed: 5 MHz

1982: Intel 80286



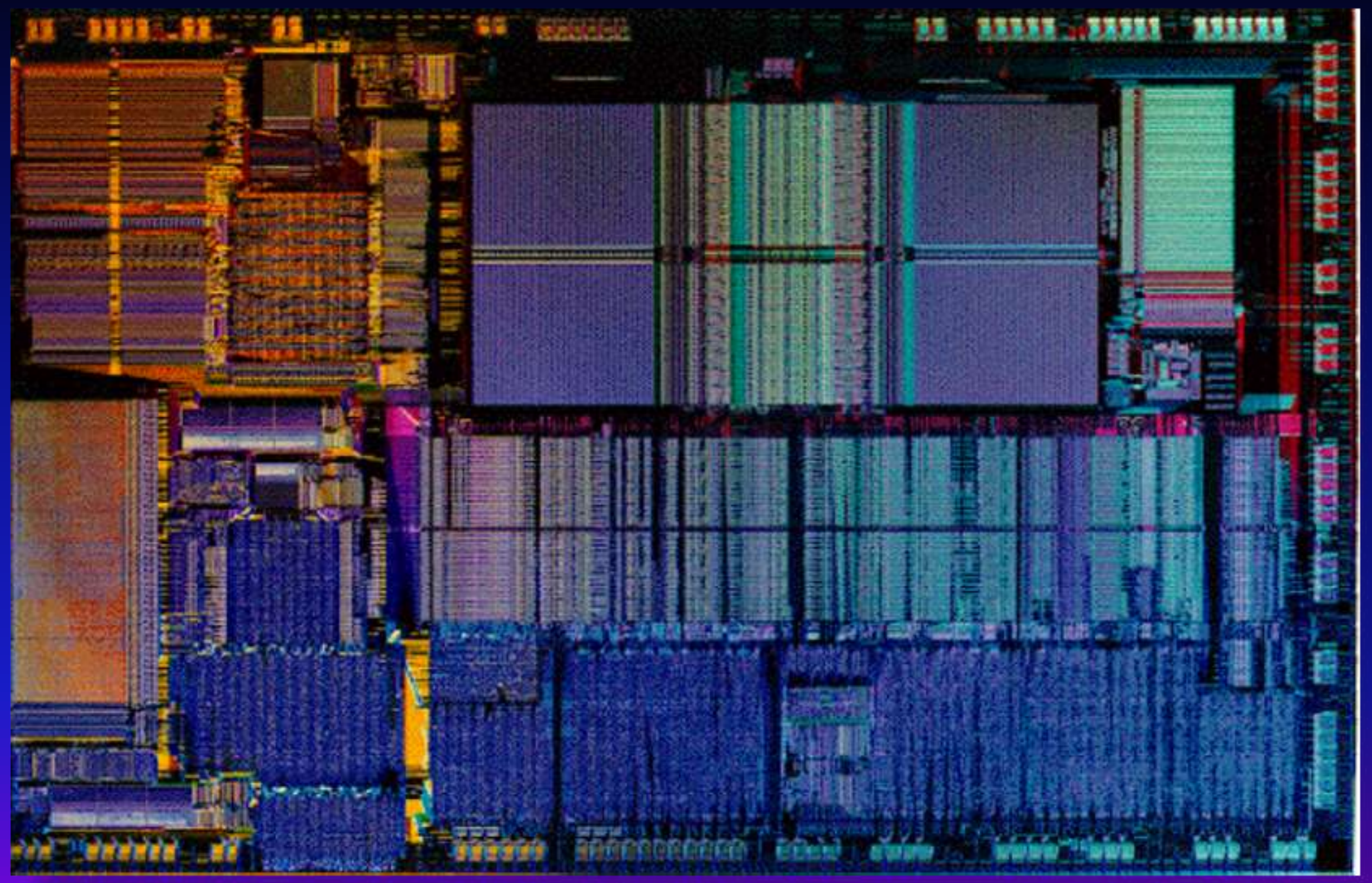
90,000 transistors
Line width: µm   Clock speed: MHz

1985: Intel 386



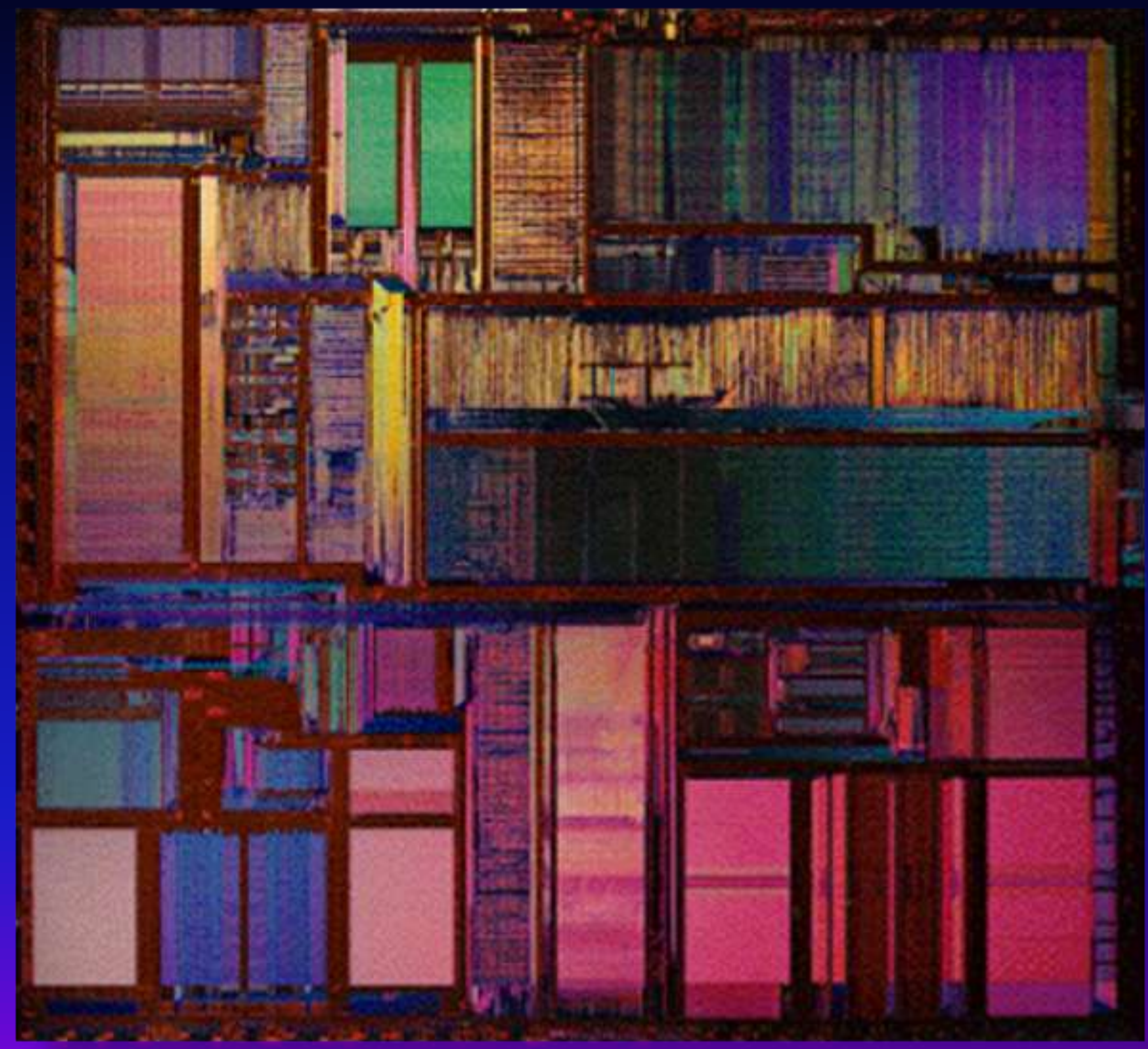
275,000 transistors
Line width: 1.5µm   Clock speed: 16 MHz

1989: Intel 486



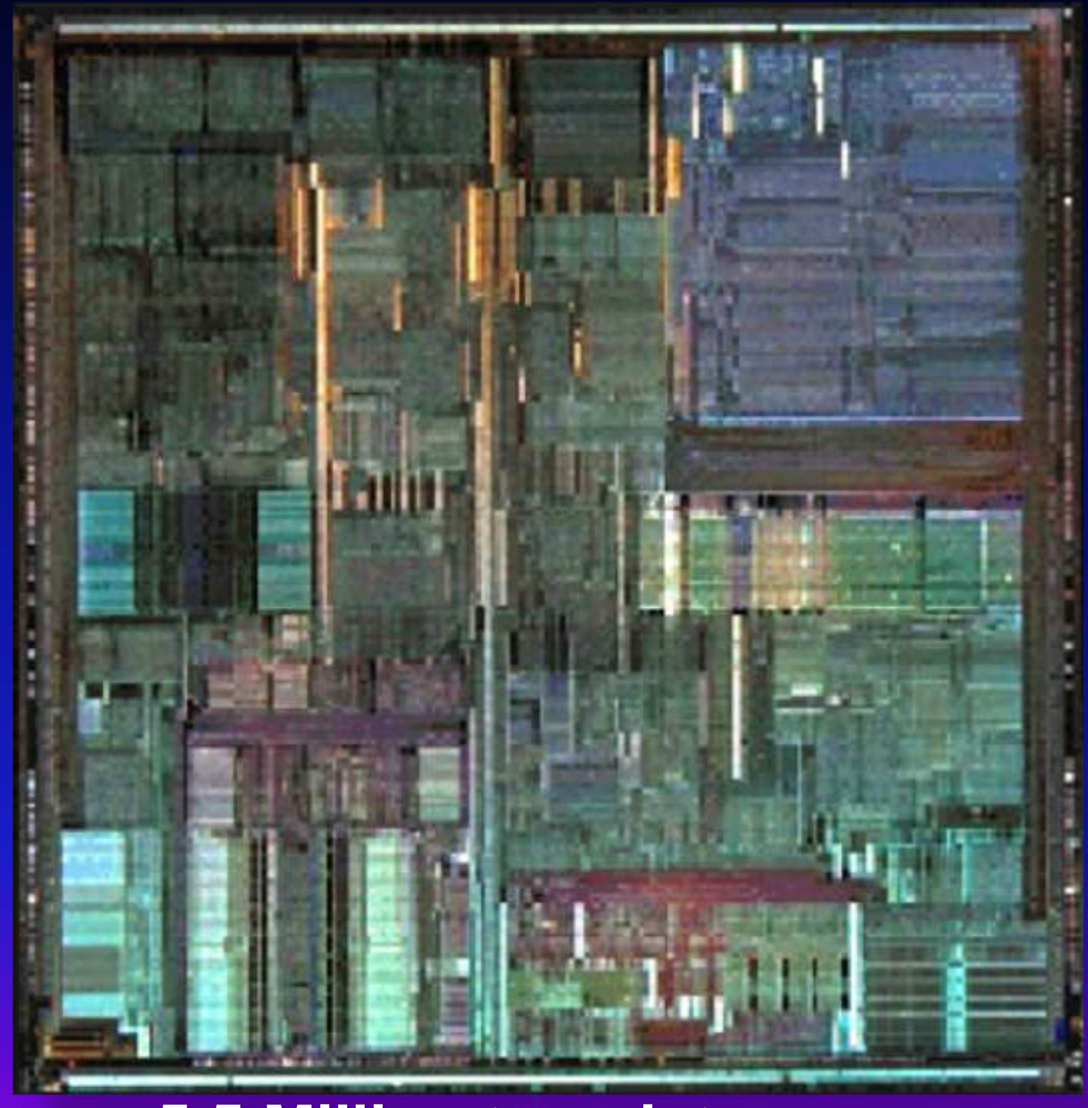
1.2 Million transistors
Line width: 1μm   Clock speed: 25 MHz

1993: Intel Pentium



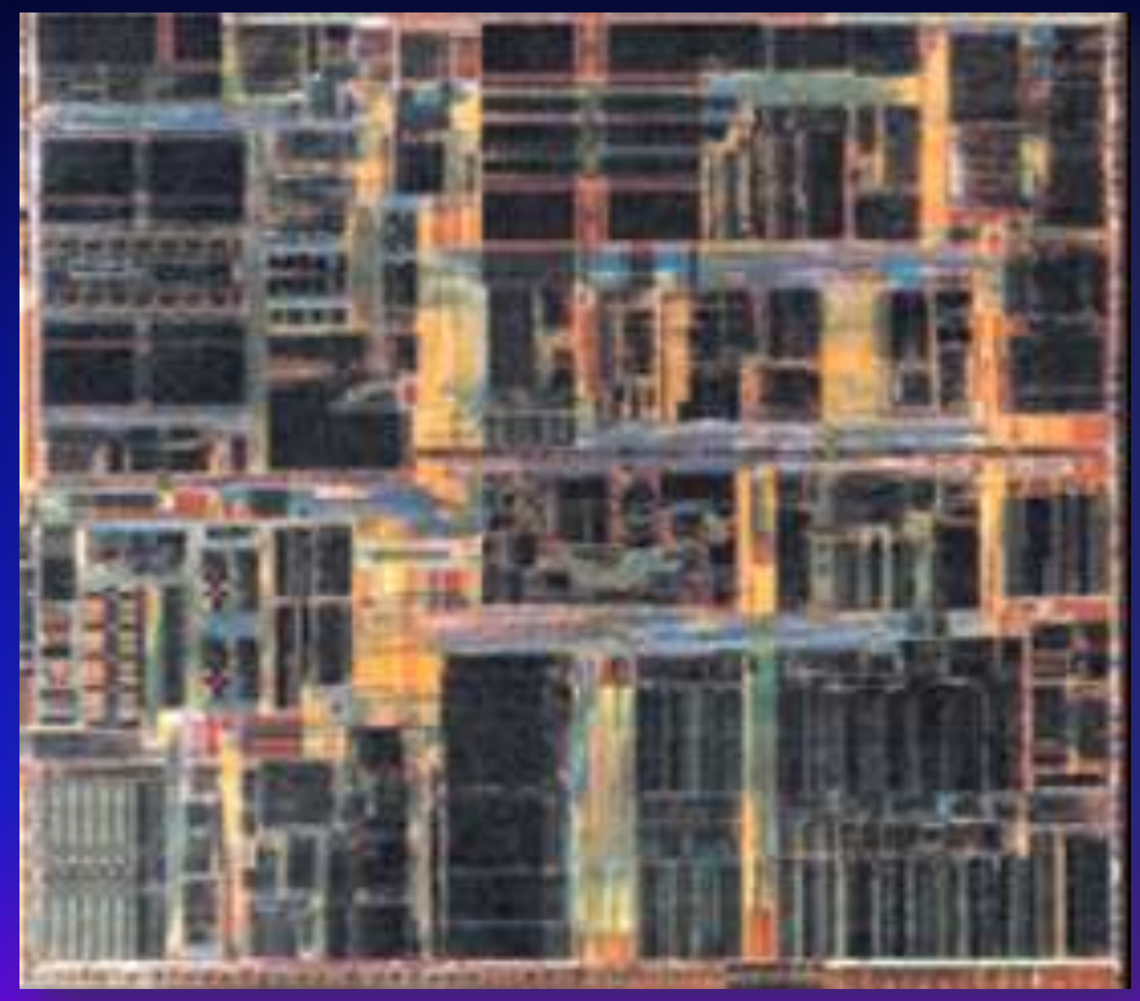
3.1 Million transistors
Line width: 0.8µm   Clock speed: 66 MHz

1995: Intel PentiumPro



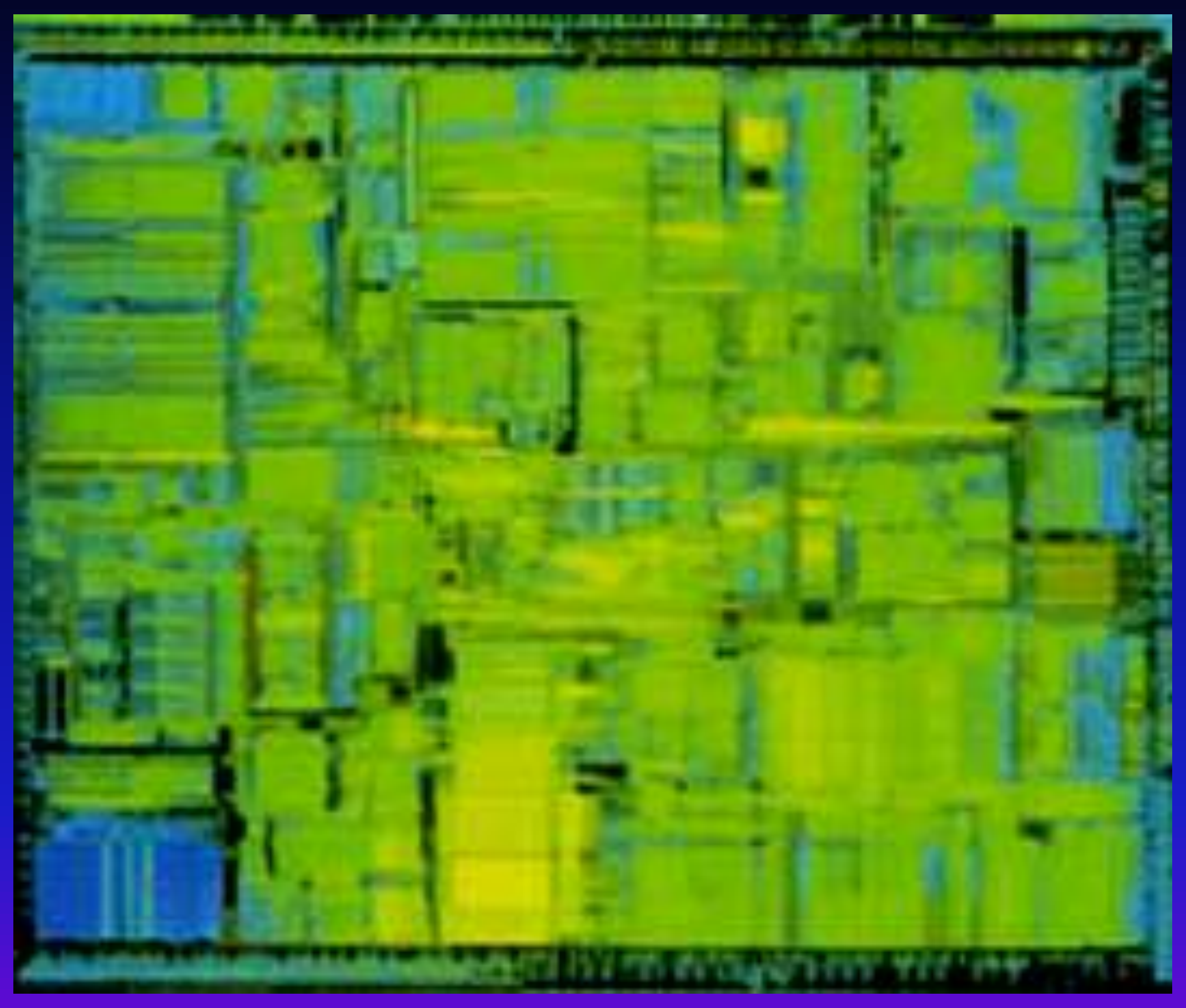
5.5 Million transistors
Line width: 0.35μm   Clock speed: 200 MHz

1997: Intel Pentium II



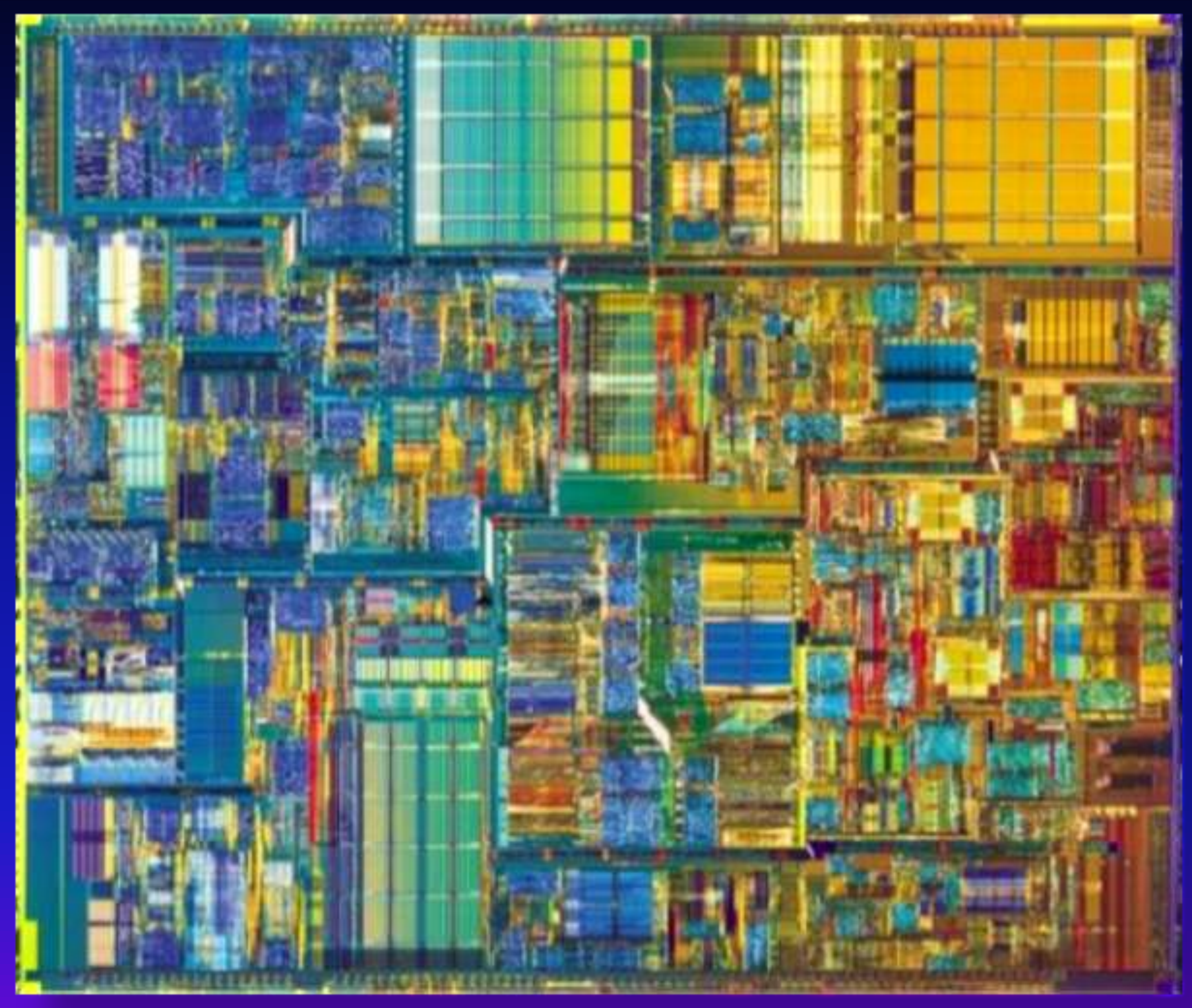
7.5 Million transistors
Line width: 0.25μm   Clock speed: 300 MHz

1999: Intel Pentium III



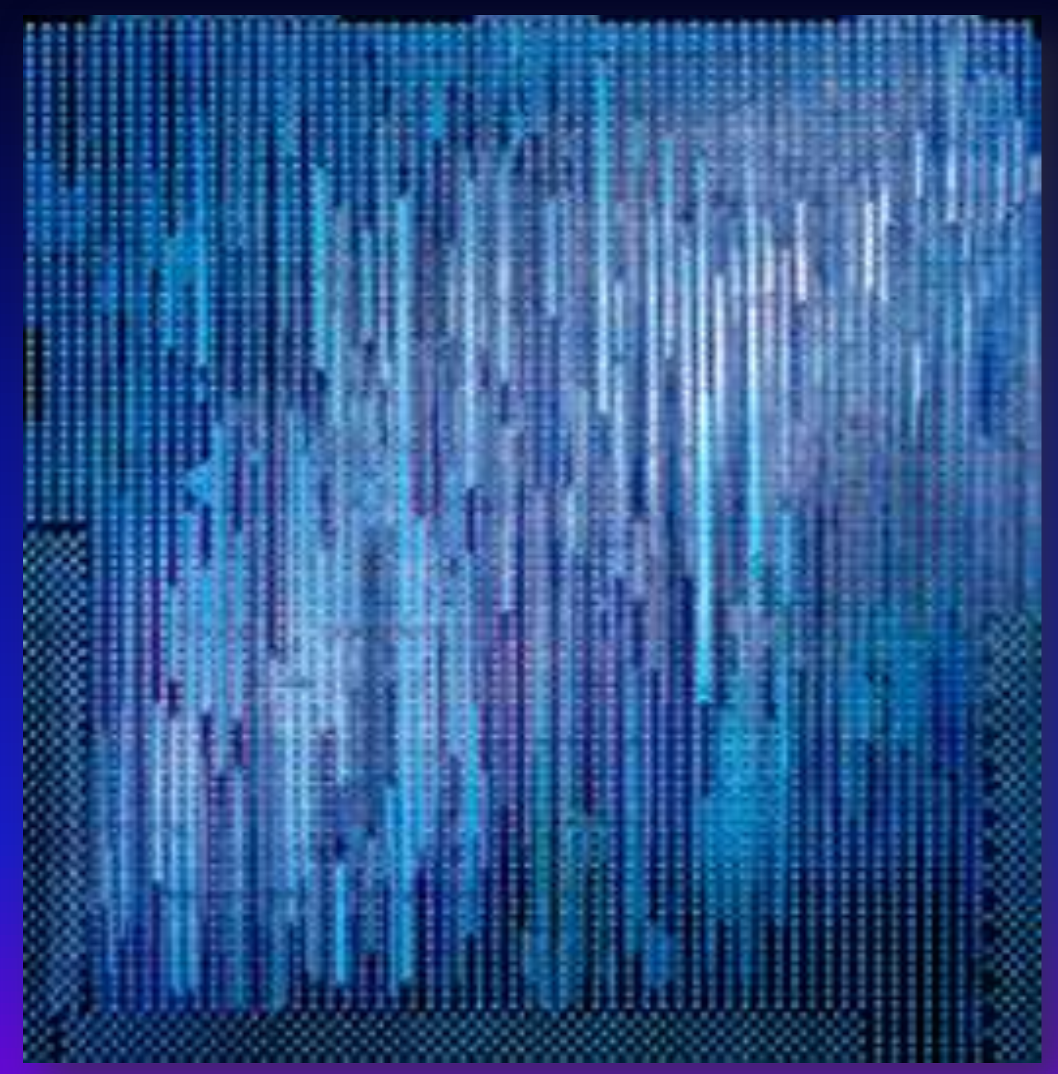
9.5 Million transistors
Line width: 0.25μm   Clock speed: 500 MHz

2000: Intel Pentium 4



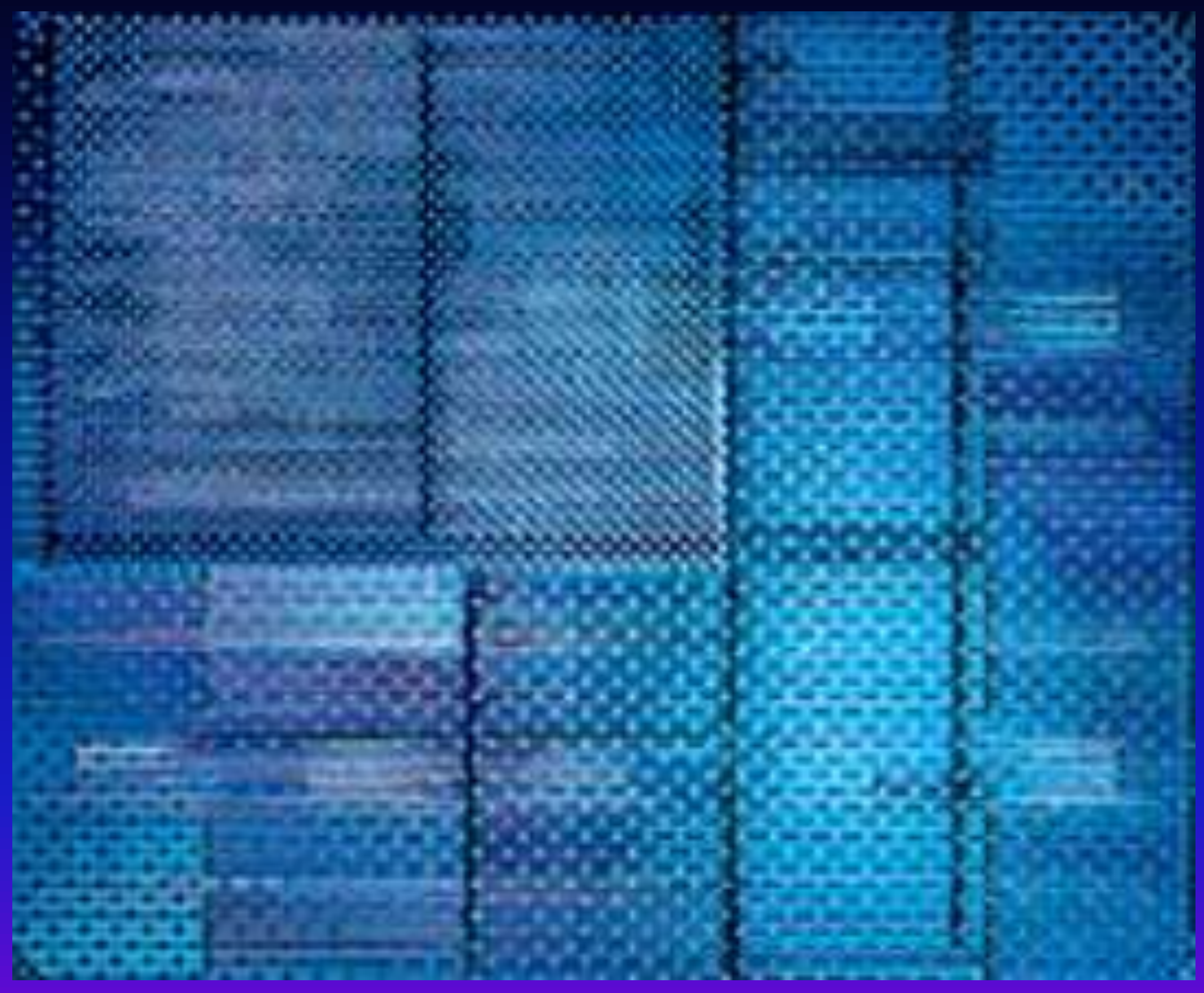
42 Million transistors
Line width: 0.18μm Clock speed: 1.5 GHz

2001: Intel Itanium



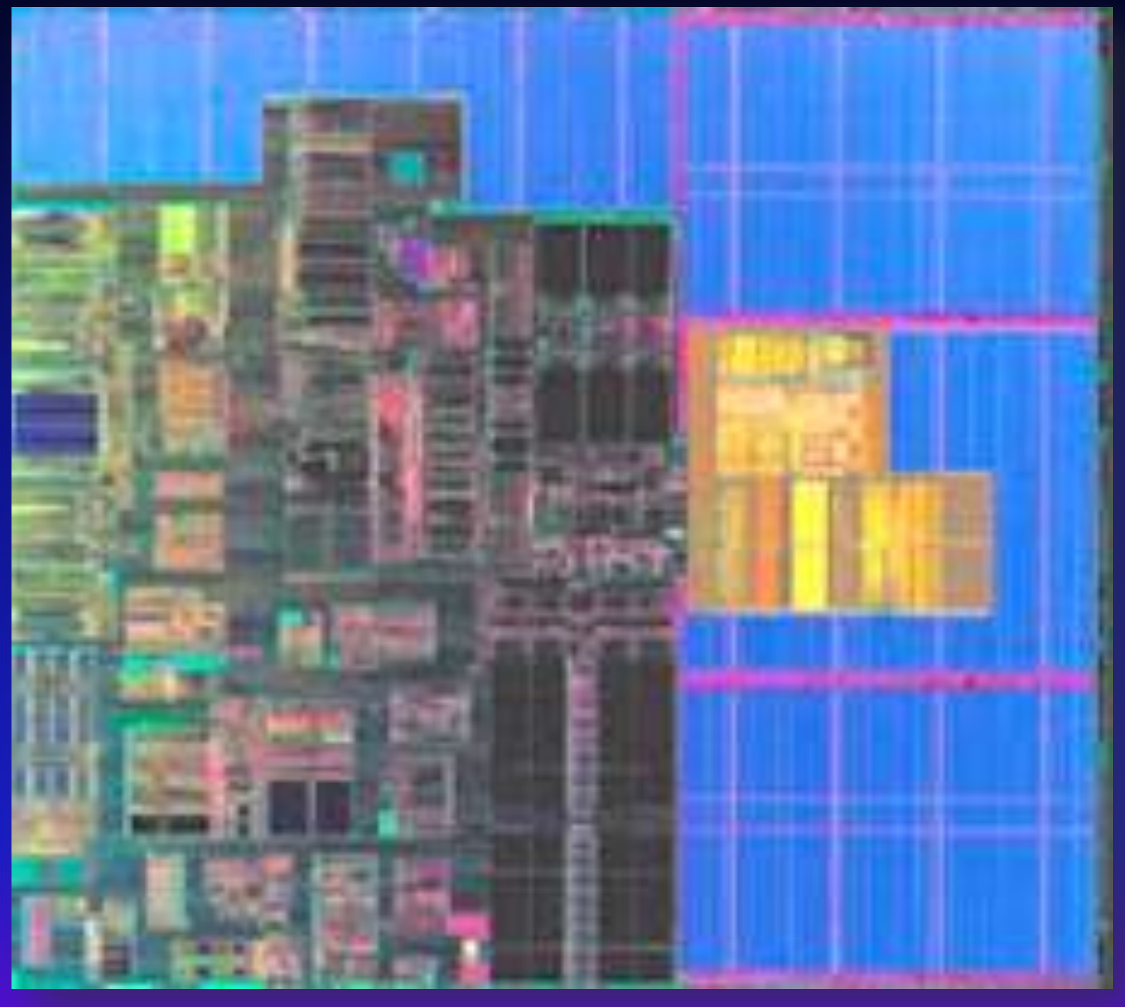
25 Million transistors
Line width: 0.18μm   Clock speed: 800 MHz

2001: Intel Xeon



42 Million transistors
Line width: 0.18μm   Clock speed: 1.7 GHz

2002: Intel Itanium 2

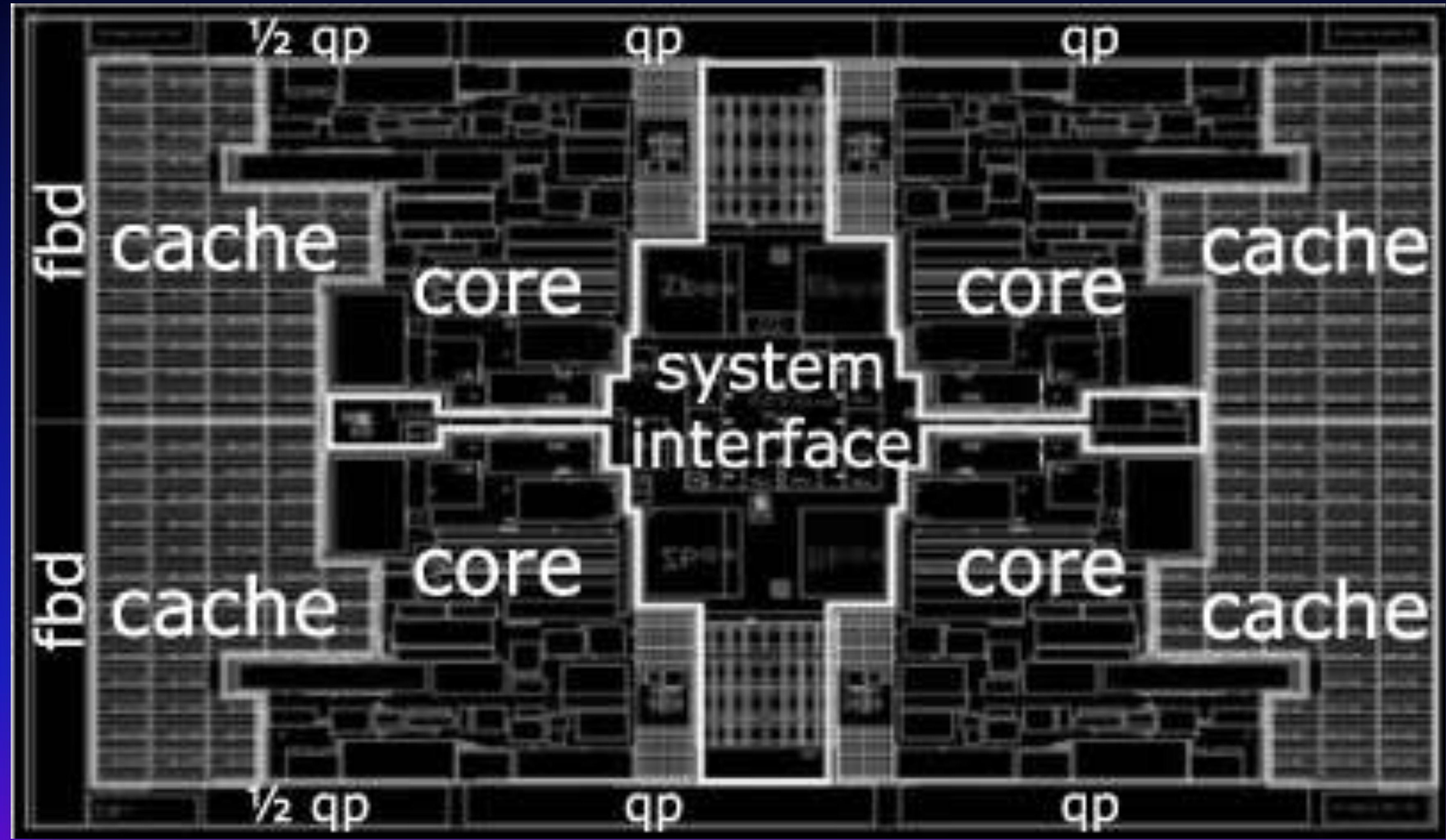


220 Million transistors
Line width: 0.18μm   Clock speed: 1 GHz

2006: Dual-Core Intel Itanium “Montecito”

1,700,000,000 transistors

2008: Quad-Core Intel Itanium "Tukwila"



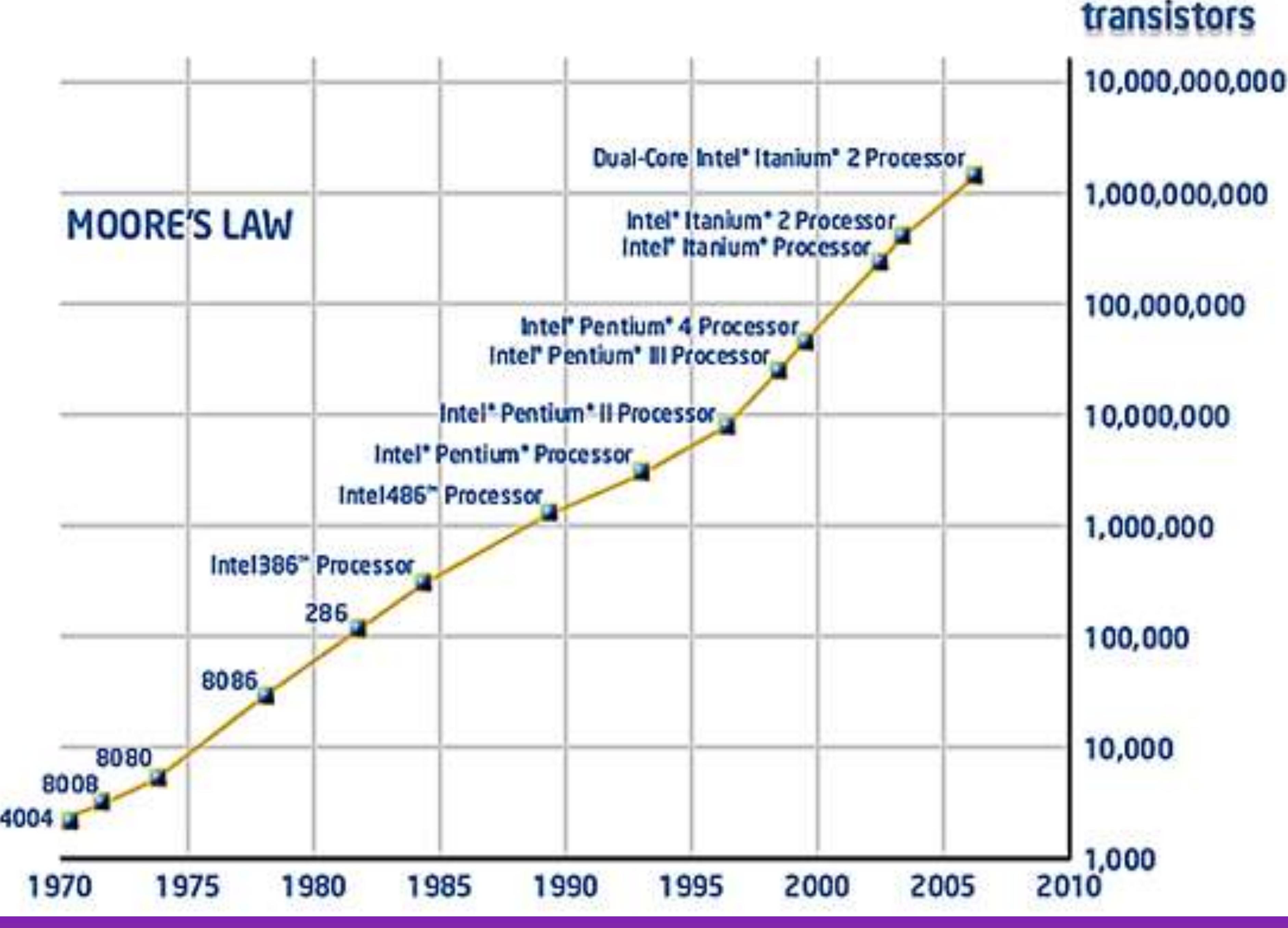
Micrograph of Tukwila.
Source: Intel

2,046,000,000 transistors
65 nm technology   Clock speed ~2 GHz

2009-2011: Intel Itanium code-named:

"Poulson"

of cores > 4 (?)
> 2,000,000,000 transistors
32 nm technology   Clock speed : ?


transistors
MOORE'S LAW
Dual-Core Intel* Itanium* 2 Processor
Intel* Itanium* 2 Processor
Intel* Itanium* Processor
Intel* Pentium* 4 Processor
Intel* Pentium* III Processor
Intel* Pentium* II Processor
Intel* Pentium* Processor
Intel486™ Processor
Intel386™ Processor
286
8086
8080
8008
4004
10,000,000,000
1,000,000,000
100,000,000
10,000,000
1,000,000
100,000
10,000
1,000
1970
1975
1980
1985
1990
1995
2000
2005
2010

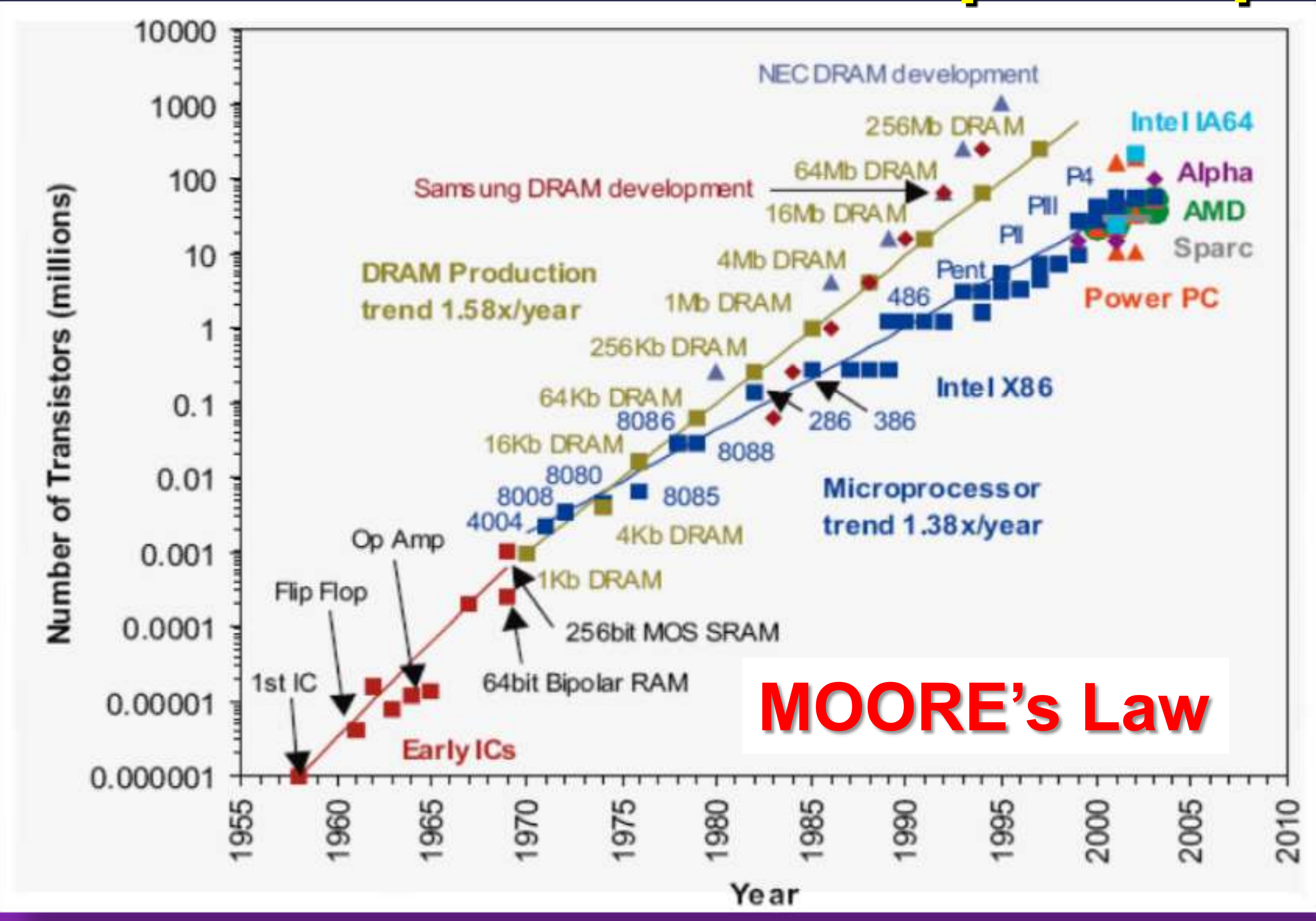
Historic Evolution of microelectronics:

The number of transistors per chip has doubled approximately every 18 to 24 months, as predicted by:

Moore's Law,

as the result of the continuous shrinking of transistors' feature size (another form of Moore's Law).

Historic evolution of the number of transistors per chip …



Scaling down the MOSFET:

Until very recently, miniaturization was being applied to conventional MOSFETs whose typical main characteristics have been:

1. Transistor type:
   a. Bulk, type planar, or
   b. Partially depleted (PD) SOI (Silicon-On-Insulator).
2. Channel : doped (100) Silicon.
3. Gate dielectric: SiO_2 based.
4. Gate electrode: highly doped single polysilicon gate.

Ref: N. Barin, et al, Analysis of Scaling Strategies for Sub-30nm Double-Gate SOI N-MOSFETs, *IEEE Trans. Nanotechnology*, Vol. 6, pp. 421-430, July 2007

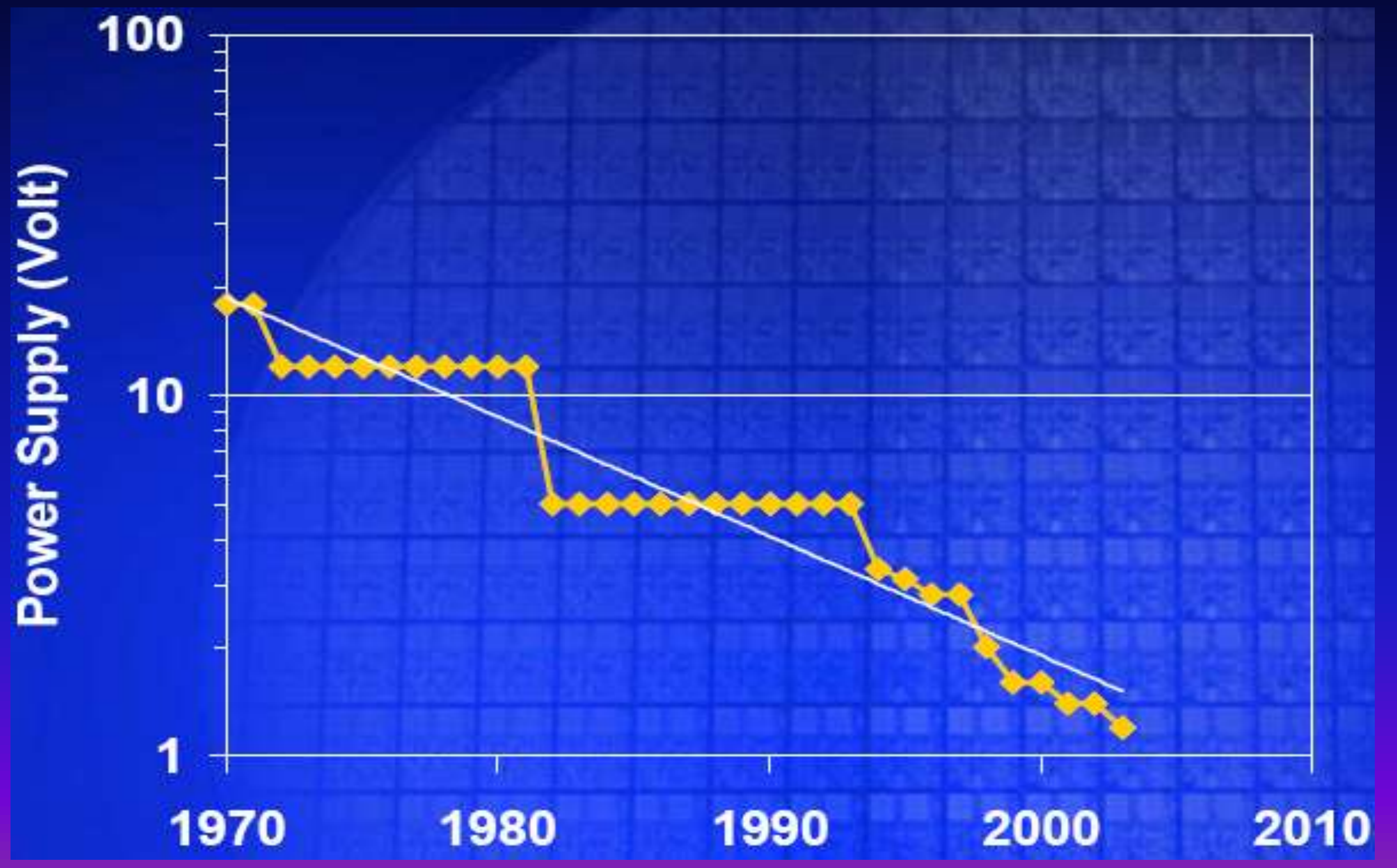
Conventional Scaling of MOSFETs:

α is the dimensional scaling factor, and
$E = V/\alpha$ the normalized electric field.

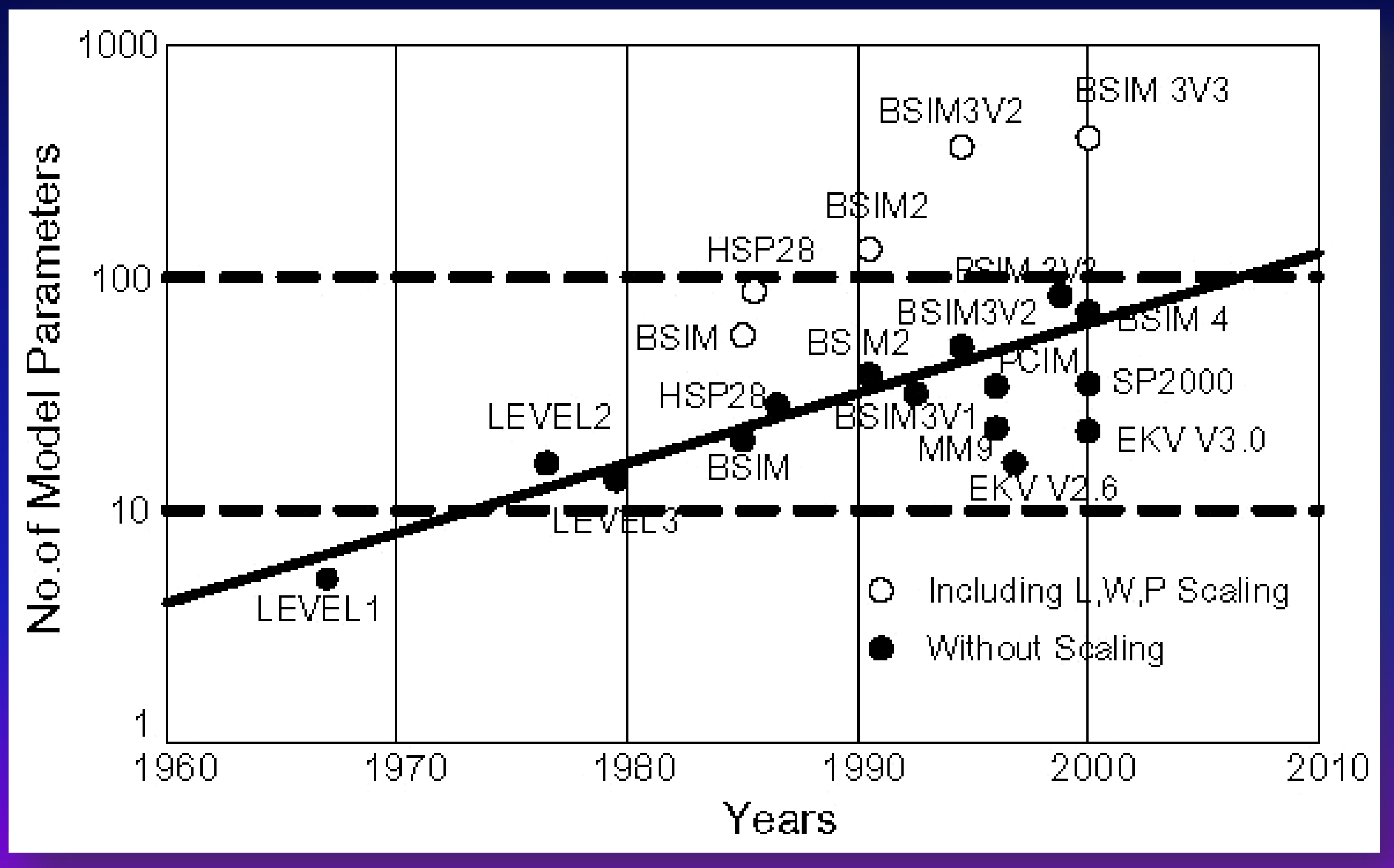
Parameter	*Constant-field scaling*	*Generalized field scaling*
Physical dimensions, L, W, T_{ox}, wire pitch	$1/\alpha$	$1/\alpha$
Body doping concentration	α	E/α
Voltage	$1/\alpha$	E/α
Circuit density	$1/\alpha^2$	$1/\alpha^2$
Capacitance per circuit	$1/\alpha$	$1/\alpha$
Circuit speed	α	α (goal)
Circuit power	$1/\alpha^2$	E^2/α^2
Power density	1	E^2
Power–delay product (energy per operation)	$1/\alpha^2$	E^2/α^3

Ref: W. Haensch, et al, Silicon CMOS devices beyond scaling, *IBM Journal of Research and Development,* vol. 50, n.4/5, pp. 339-362, 2006.

The supply voltage has been coming down



… likewise, the number of parameters in devices' compact models grows …



Ref: J.J. Liou, F. Schwierz, Solid-State Electronics, 47, pp. 1881–1895, 2003

… but the cost keeps decreasing.

Ref: WSTS/Dataquest

Are there limits?

It seems to be getting harder to continue the path of "top-down" miniaturization because we are approaching fundamental physical and technological limitations, as well as increasing economic burdens.

According to the "International Technology Roadmap for Semiconductors" (ITRS), the physical gate length of high performance MOSFETs (commercial) should reach dimensions of about

10nm around 2016

Are there limits?

The main impediments to continue shrinking the conventional transistor are:

- Size itself
- Speed
- Power consumption
- Fabrication complexity
- Cost of technology

Are we reaching the end of Moore's Law?

… not yet, but

Moore's Law, such as we have understood it up to now, is indeed reaching its end.

The miniaturization of conventional transistors will reach its limit approximately within one decade (or less).

⇒ Moore's "Law" was not really a law, but only a temporary rule applicable to a specific technology: the fabrication of monolithic Si microcircuits through conventional optical photolithography.

Today, for the first time since 1965, it is becoming increasingly complicated, or even **impossible, to predict** the development of electron devices much farther than a decade (22nm technology node?).

However, we may imagine some probable **tendencies:**

Tendencies:

For the time being… (about 10 years)

- **The miniaturization** of conventional technology MOSFETs **will continue** to its natural limit (22nm or 15nm?), by way of the development of **new materials** (oxides, metals, others) **and structures** (3D MOSFETs), and the use of advanced lithography (immersion, EUV, etc)

MOSFETs' technology Nodes

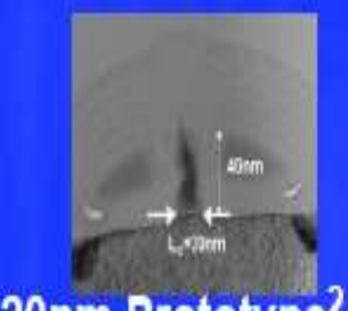
90nm Node
2003

50nm Length
(IEDM2002)

65nm Node
2005

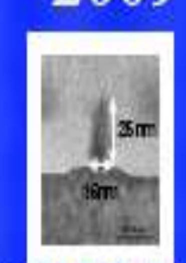
30nm Prototype[1]

45nm Node
2007



20nm Prototype[2]

32nm Node
2009



15nm Prototype[3]

22nm Node
2011

10nm Prototype[4]

References
1. IEDM, R. Chau et al., 12/00
2. 2001 Silicon Nanoelectronics Workshop, R. Chau et al., 6/01
3. TeraHertz Transistor press briefing, G. Marcyk & R. Chau, 11/01
4. 61st Device Research Conference, R. Chau et al., 6/03

Si wafer diameter:

For the time being… 300mm

According to the 2007 ITRS, the target for introduction of 450 mm wafers (in production) has been set for 2012 to 2016.

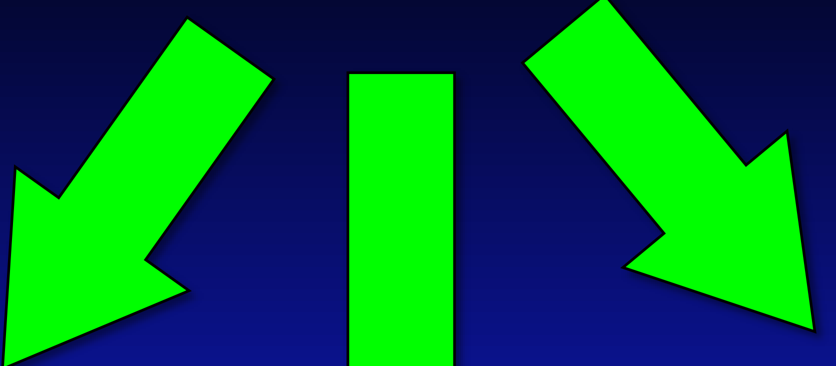
Directions

more Moore

more than Moore

beyond CMOS

Directions



miniaturization
("More Moore")

functional diversification
("More than Moore")

heterogeneous integration
("Beyond CMOS") non-charge-based devices
(spin, quantum, molecular approaches, etc)

Miniaturization (More Moore) *through…*

1. **Geometrical** (constant field) **Scaling:**
   Continue shrinking horizontal and vertical physical feature sizes to improve:
   a) density (cost per function reduction)
   b) performance (speed, power)
   c) reliability.

2. **Equivalent Scaling:**
   a) 3-D device structure improvements
   b) new non-geometrical process techniques
   c) new materials that affect the electrical performance of the chip.

… and what might come after *conventional miniaturization has reached its limit ?*

At the device level:

- new unconventional devices.

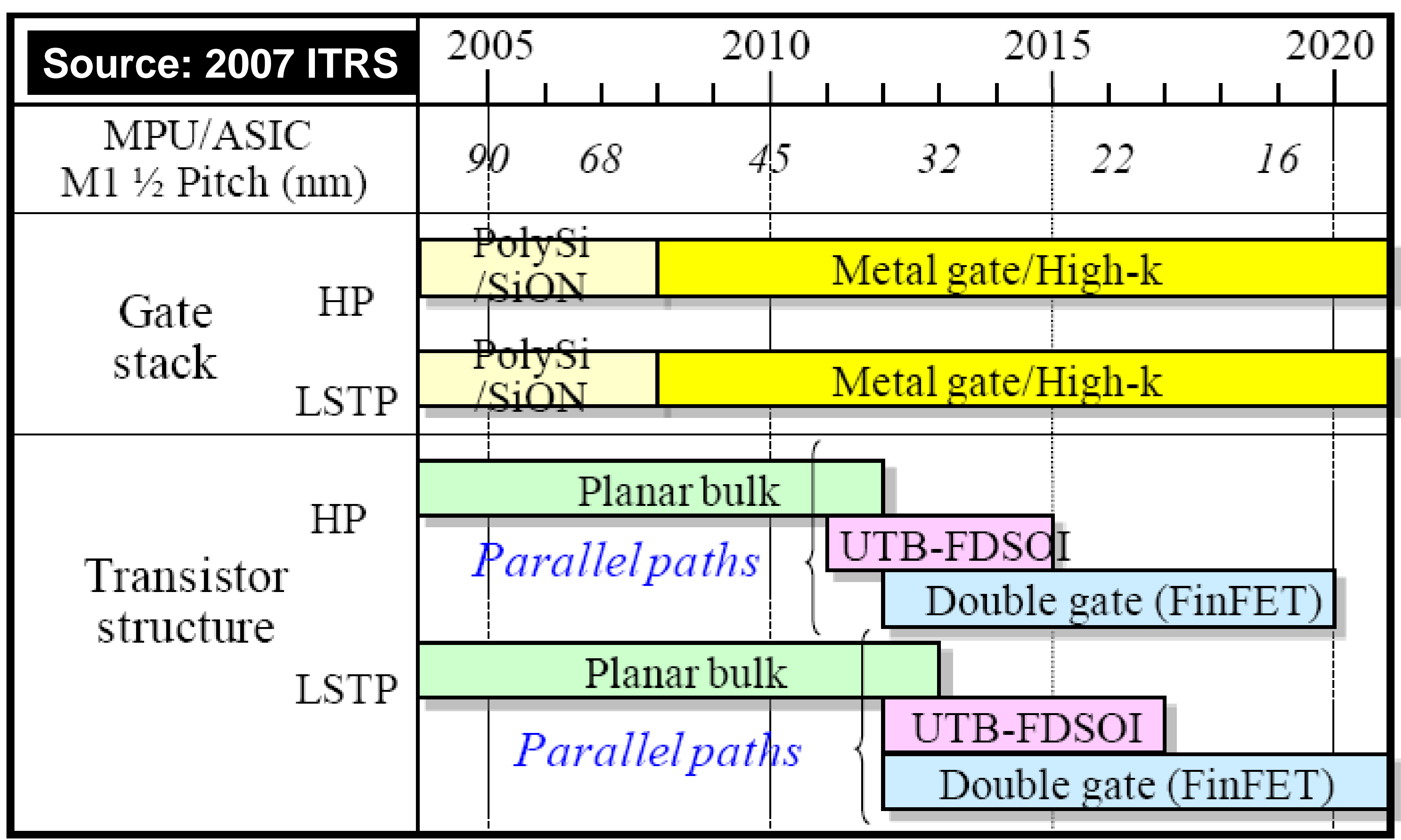
At the technology level:

- self assembly (bottom-up).

At the system level:

- more development of advanced architectures (multi-parallelism).
- more development of innovative processing software.

Major technology innovations required over the next few years



Functional Diversification

("More than Moore")

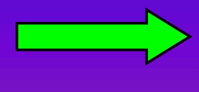
1. Integrate into devices more functionalities to provide added value to end customer.
2. Transfer non-digital functionalities from the system board-level to package-level (SiP) or chip-level (SoC).

(for example: RF communication, power control, passive components, sensors, actuators)

Beyond…

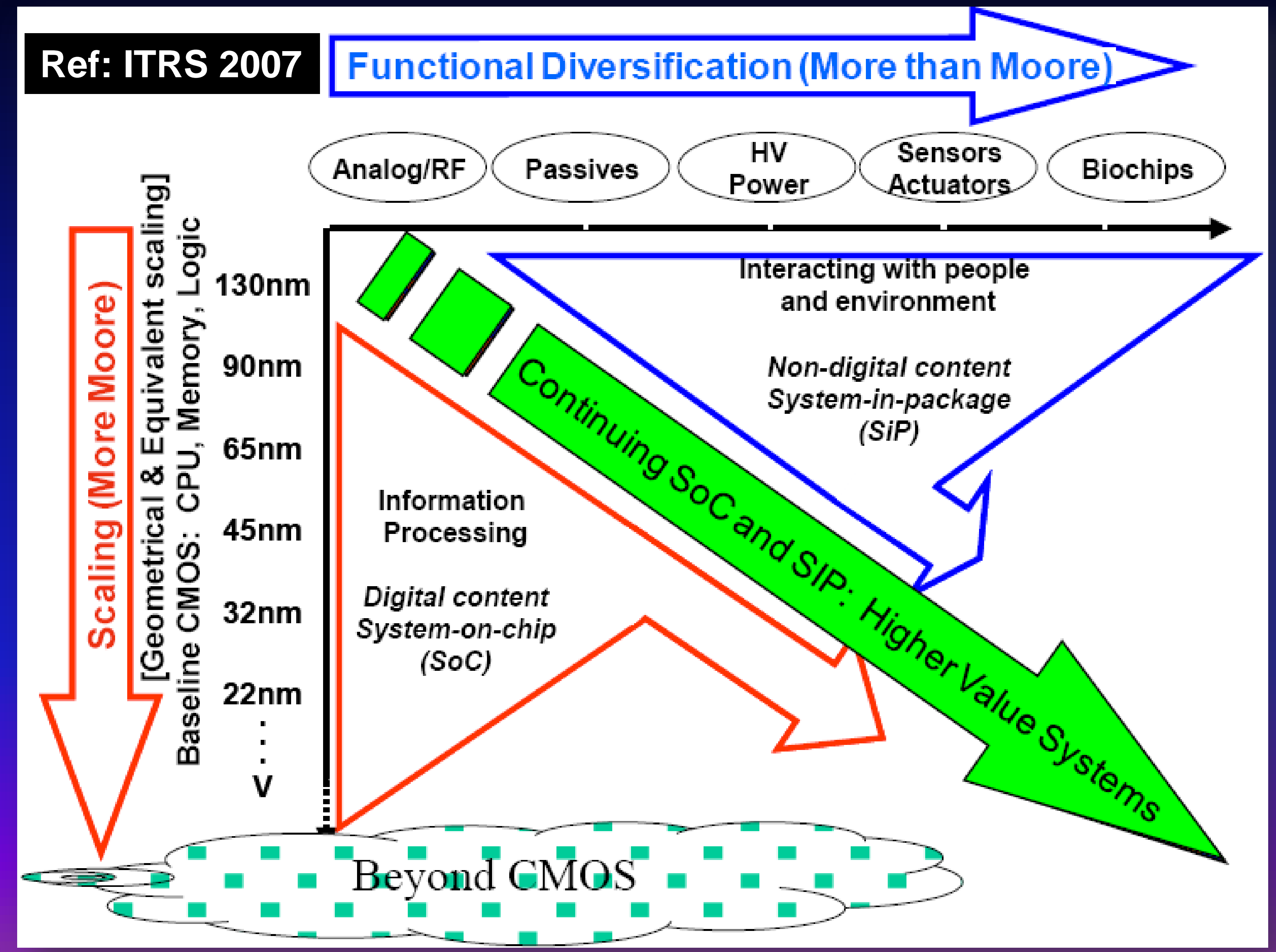
the development of new unconventional devices not based on the massive flow of electrons, and preferably made "bottom-up" by self-assembly:

molecular electronics?



Biology, Organic Chemistry

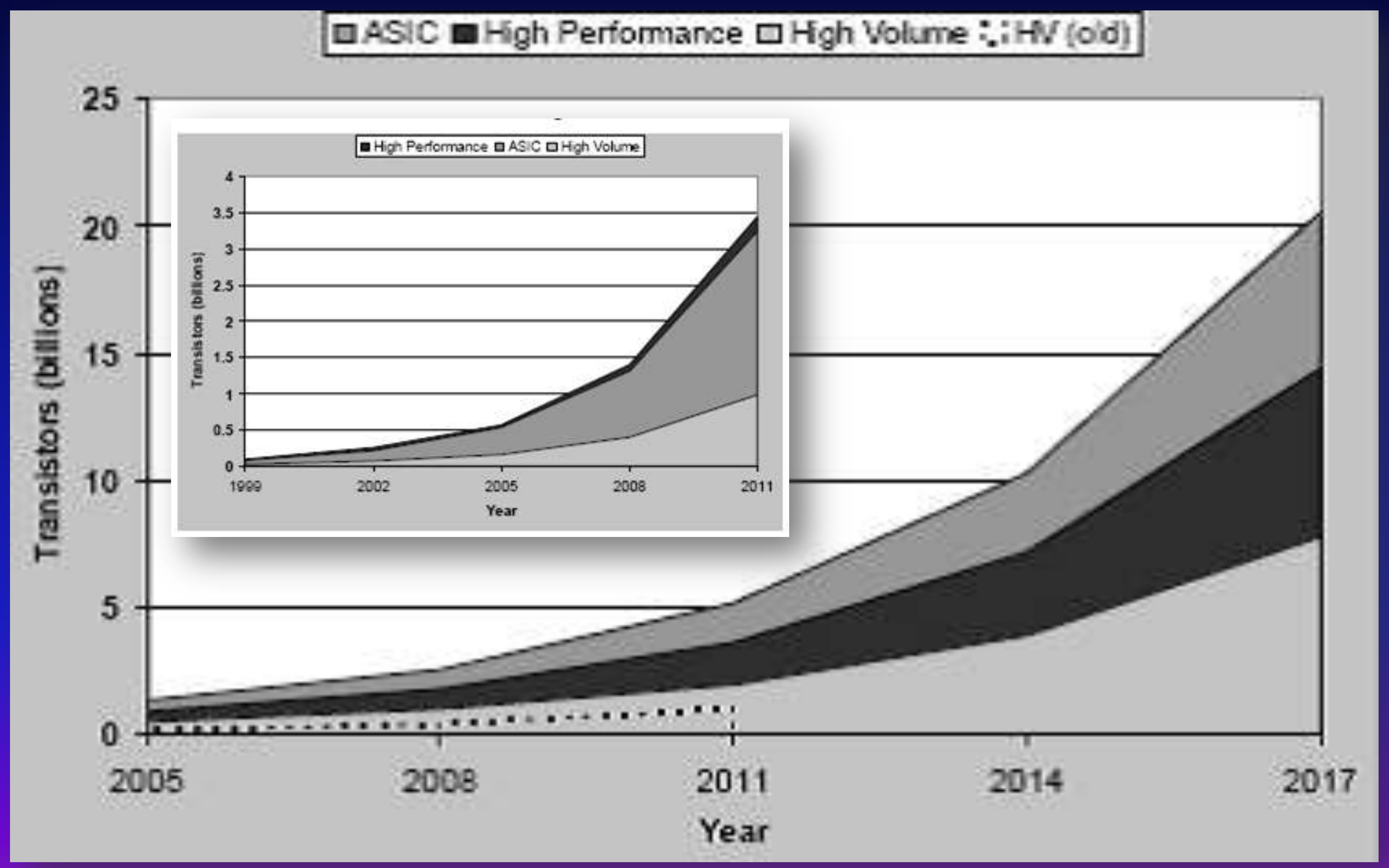
Directions



Oportunities:

- New materials
  - New structures
    - New fabrication methods
      - New devices
        - New models

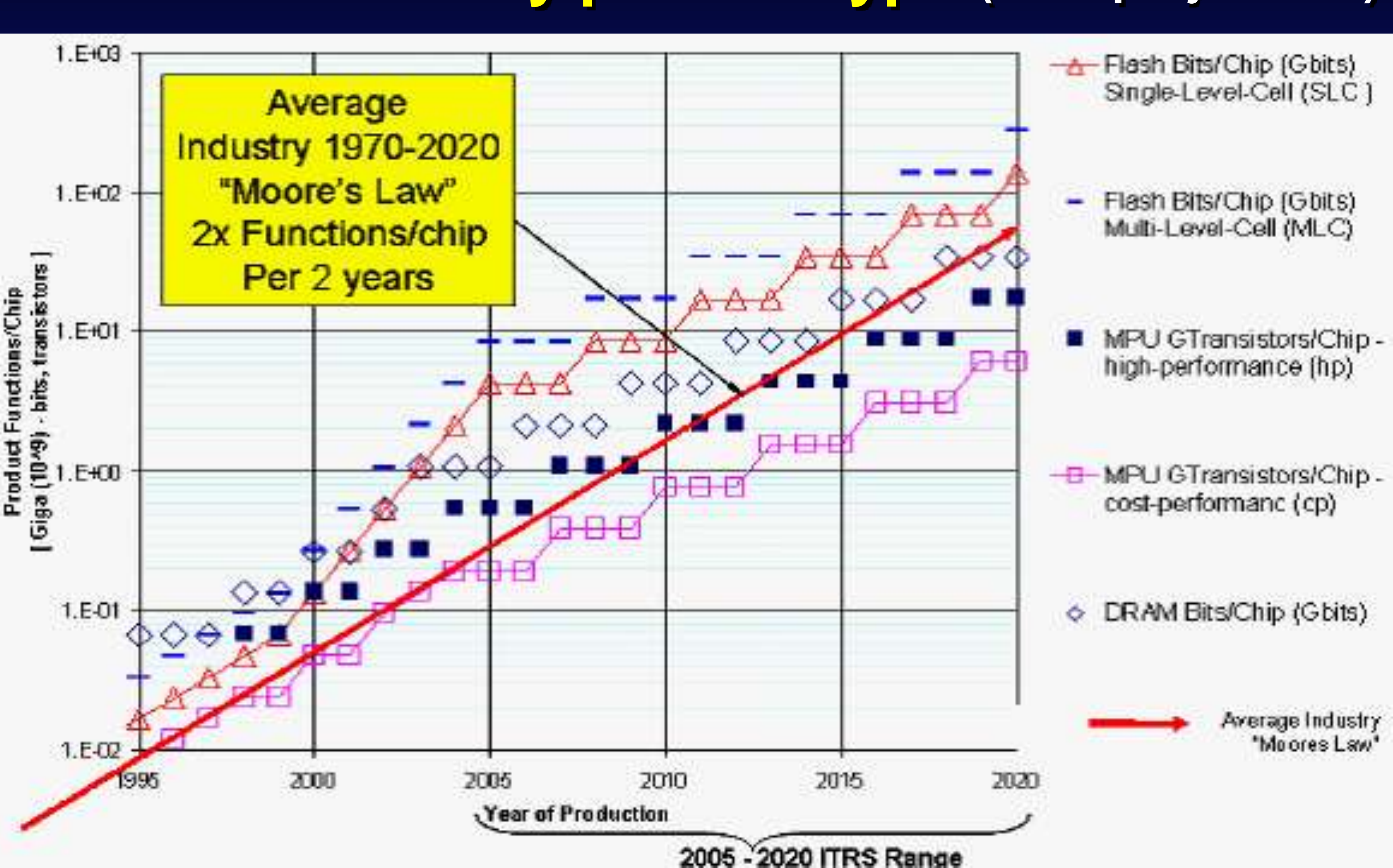
Recent projections of the number of transistors per chip



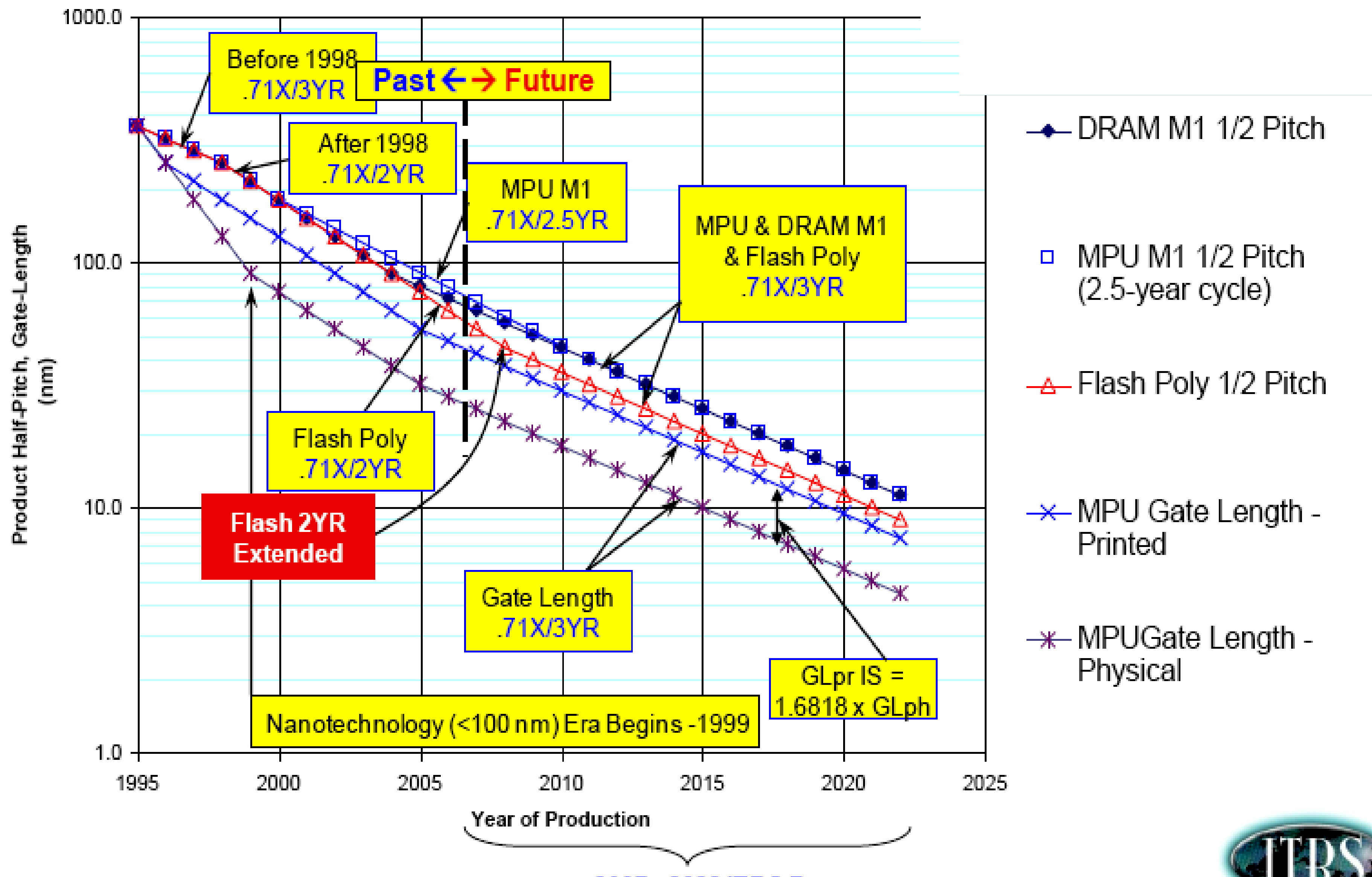
Ref: ITRS - 2007

(in an area of 400mm²)

Tendencies: Functions per chip
by product type (ITRS projections)

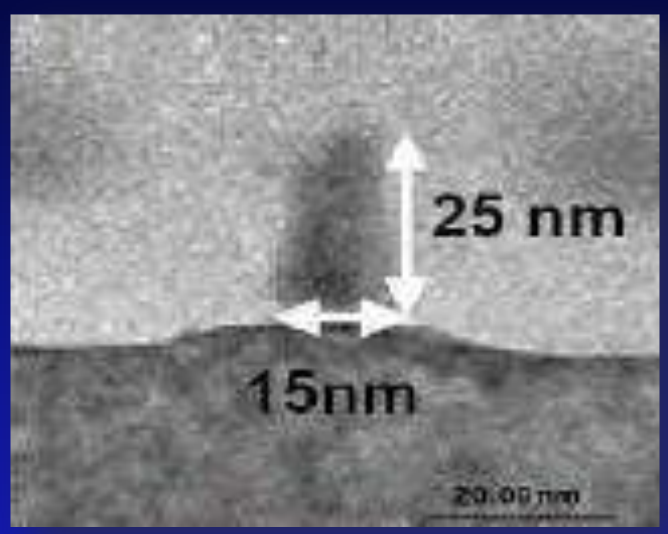


ITRS Product Technology Trends



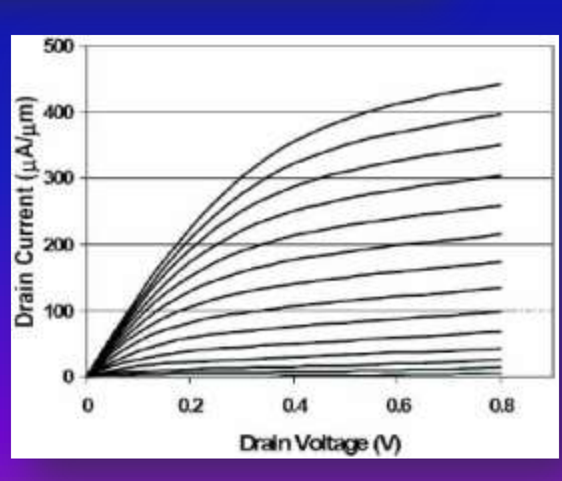
This is Nanoelectronics

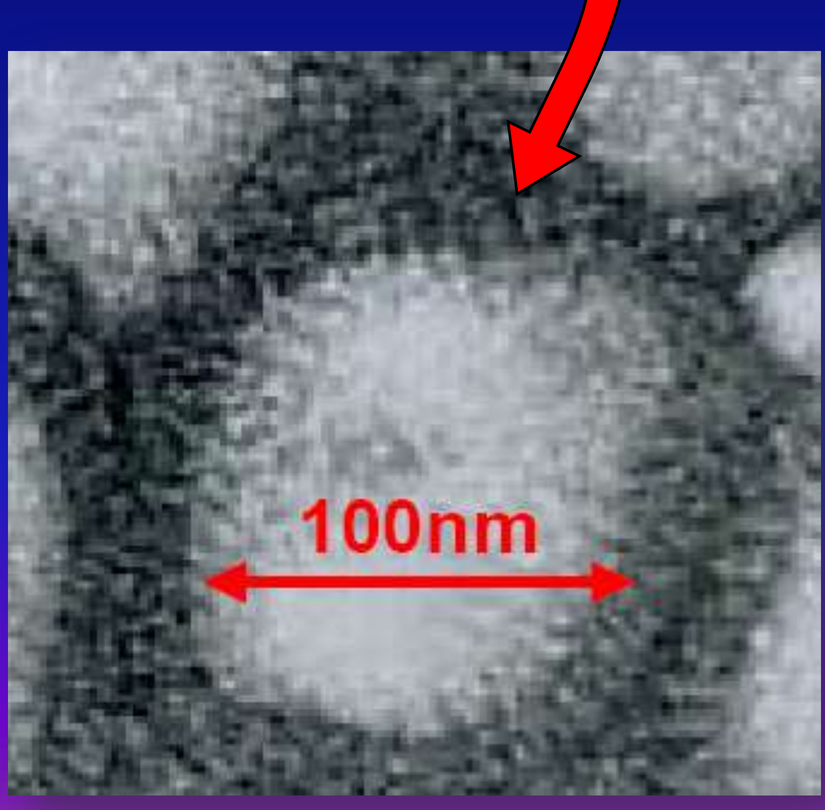
The Semiconductor Industry is the true pioneer of Nanotecnology !!!



One quarter the size of an Influenza virus

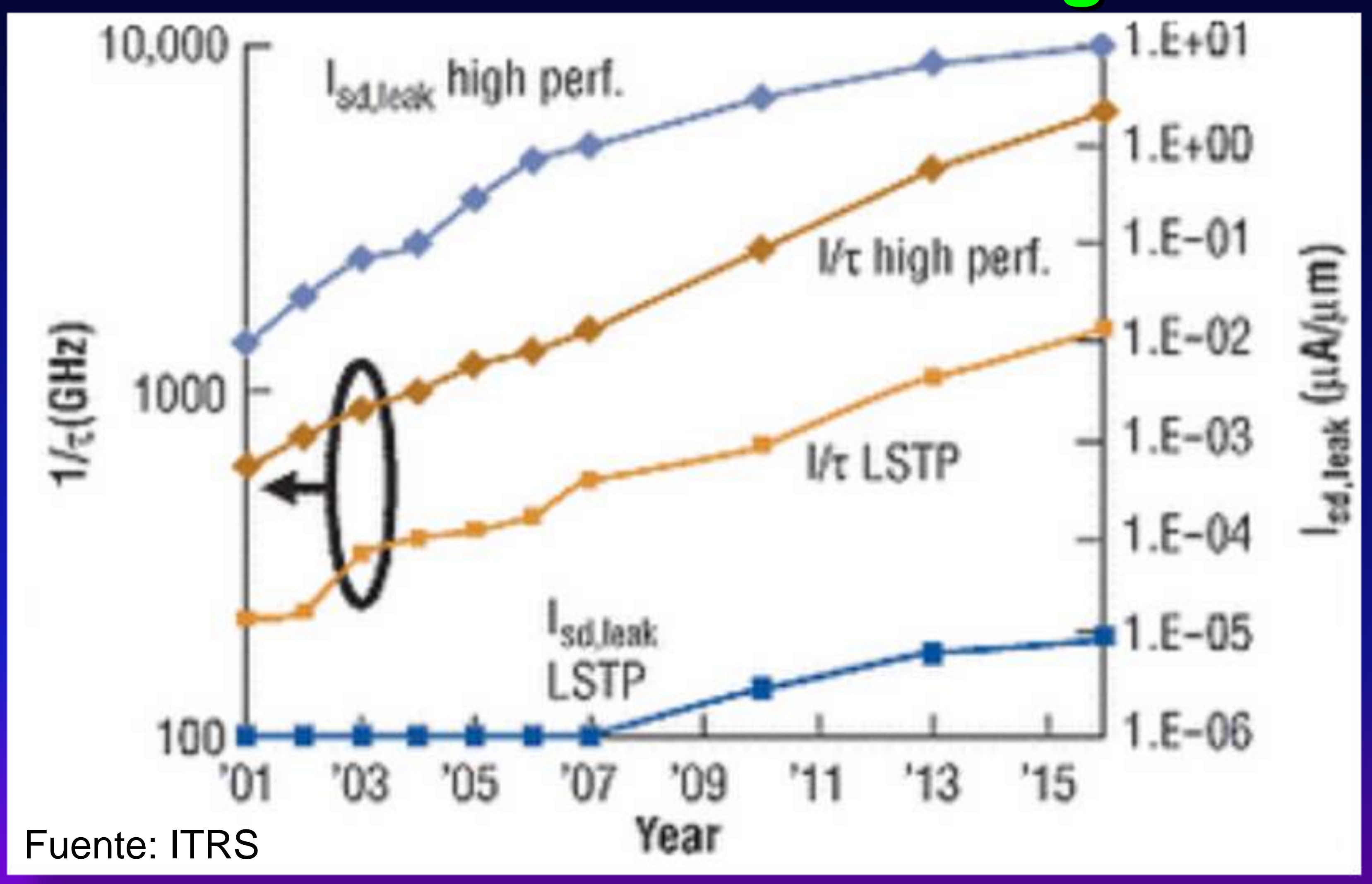
15nm NMOS transistor. 2.63THz@ 0.8V



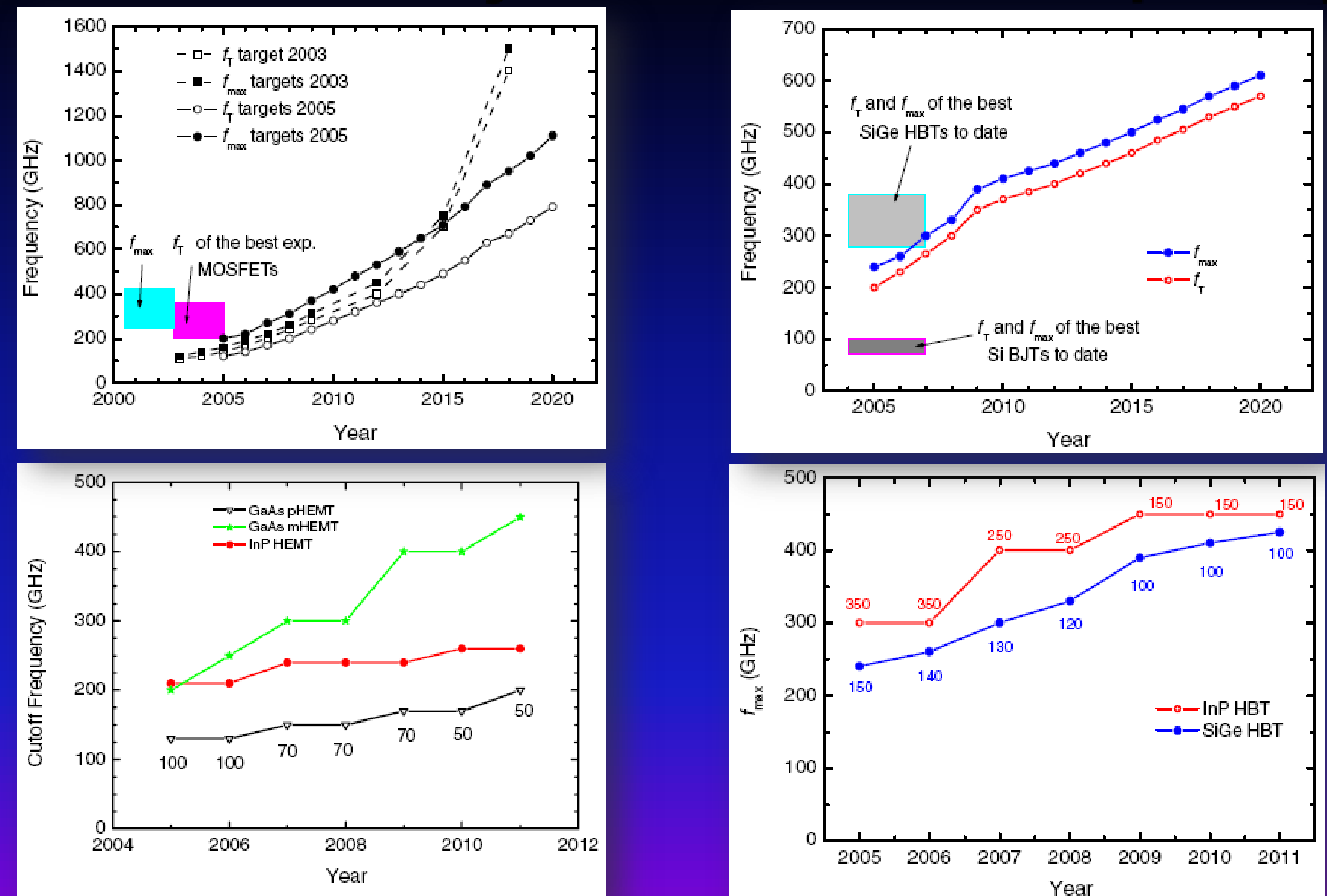


Ref: Intel

Projections for speed and leakage current

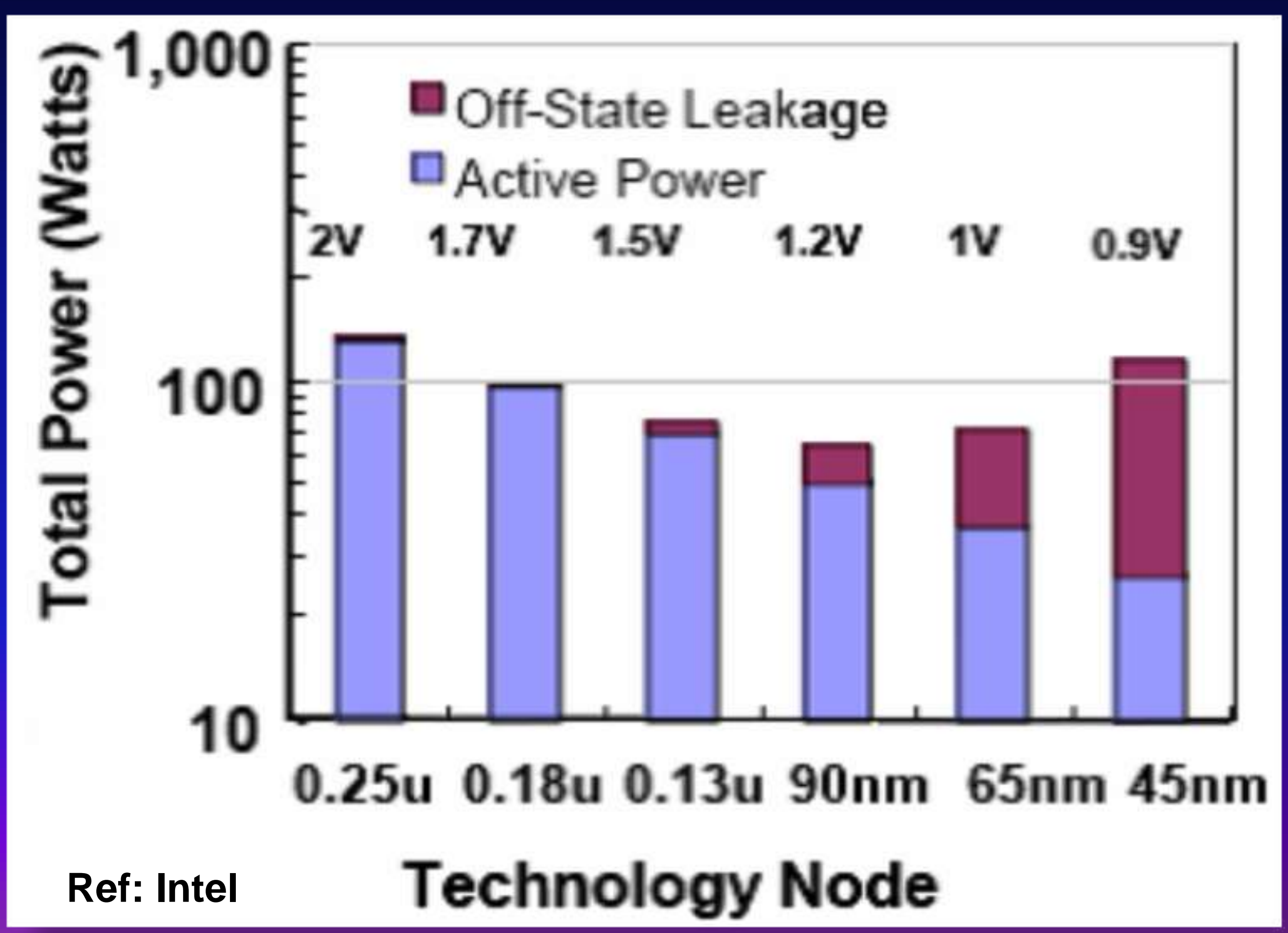


Projections about frequency



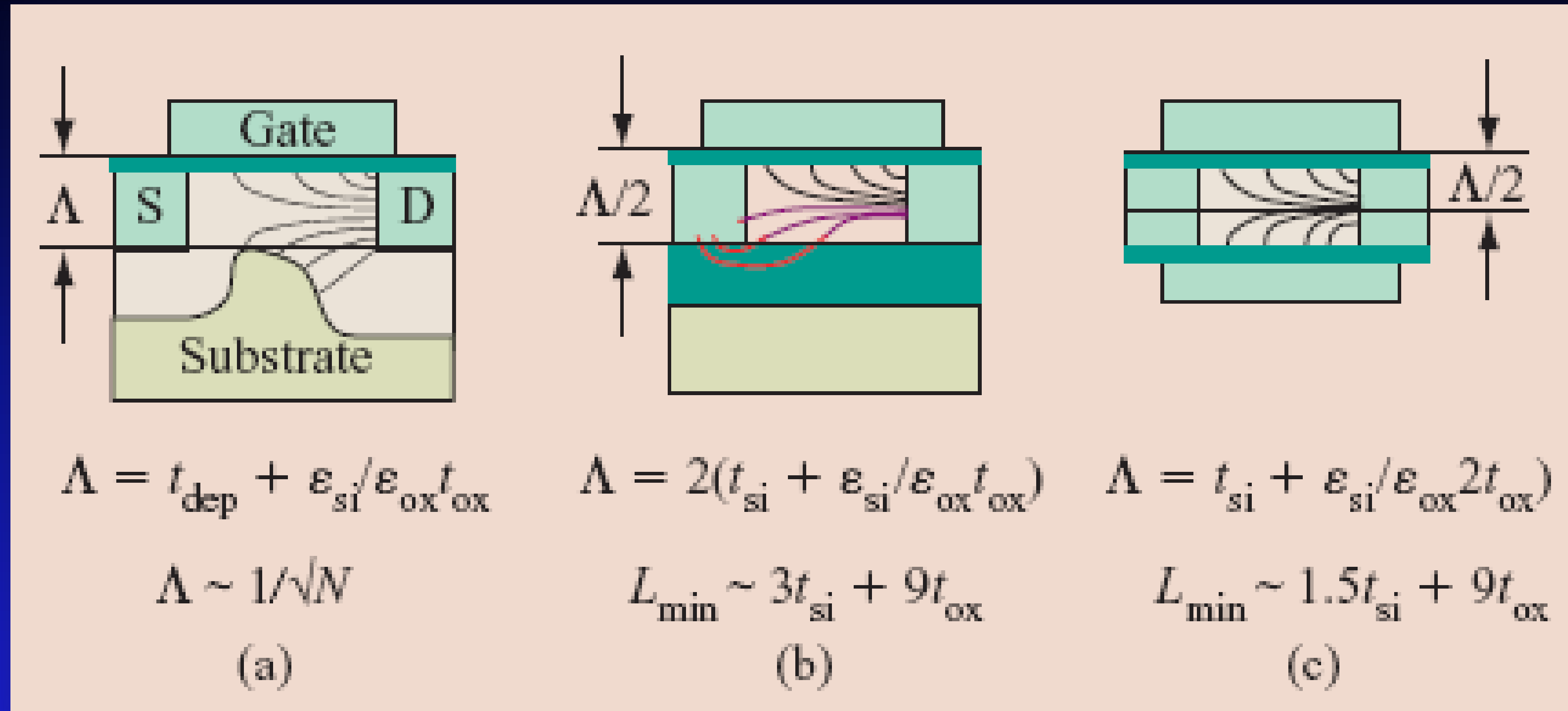
Ref: F. Schwierz a, J.J. Liou, RF transistors: Recent developments and roadmap toward terahertz applications, *Solid-State Electronics , vol.* 51, pp.1079–1091, 2007.

Evolution of relación entre Active to Passive Power as function of size



Extending
MOORE's
Law
(more) Nanoelectronics
but nanotechnology implies
more than just miniaturization

Scaling potencial



Types of MOSFETs: (a) Bulk
(b) FD SOI
(c) FD double-gate device.

Ref: D. J. Frank, et al, "Device Scaling Limits of Si MOSFETs and Their Application Dependencies," *Proc. IEEE* 89, 259–288 (2001).

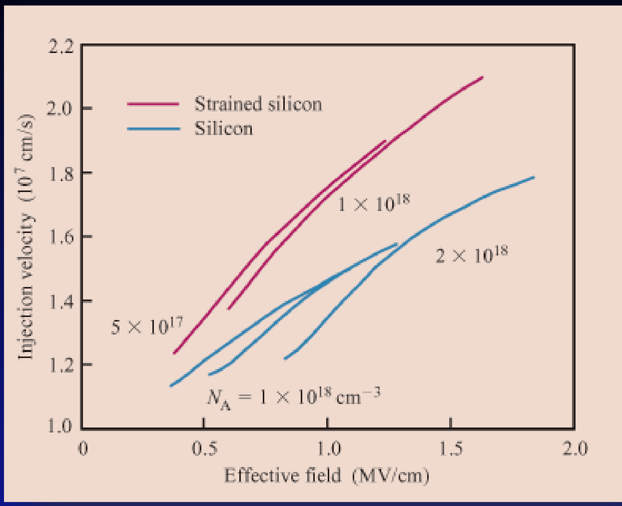
Some emerging MOSFET structures

Transport-enhanced FETs	*Ultra-thin Body SOI FETs*		*Source/Drain Engineered FETs*	
Strained Si, Ge, SiGe; buried oxide; Silicon Substrate	BOX	FD Si film; S; D; Ground Plane; BOX (<20nm); Bulk wafer	silicide; nFET; pFET; Silicon; Schottky barrier isolation	S; D; Non-overlapped region
Strained Si, Ge, SiGe, SiGeC or other semiconductor; on bulk or SOI	Fully depleted SOI with body thinner than 10 nm	Ultra-thin channel and localized ultra-thin BOX	Schottky source/drain	Non-overlapped S/D extensions on bulk, SOI, or DG devices

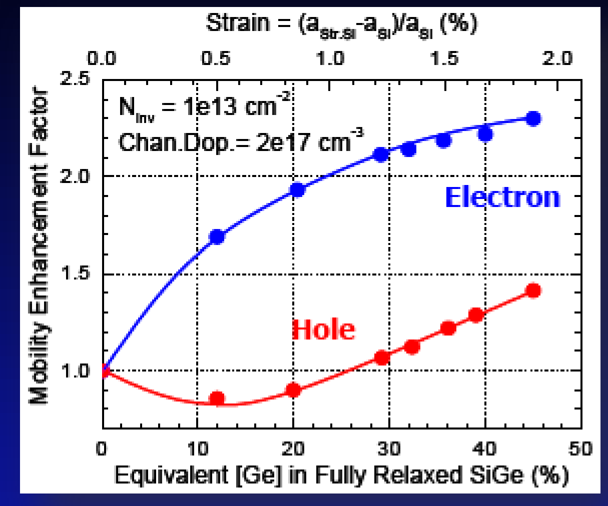
Multiple Gate FETs				
N-Gate (N>2) FETs	*Double-gate FETs*			
L_g; W_{Si}; T_{Si}	Gate; Source; Drain	GATE; SOURCE; DRAIN; Si-substrate; STI		Gate; Gate; Drain
Tied gates (number of channels >2)	Tied gates, side-wall conduction	Tied gates planar conduction	Independently switched gates, planar conduction	Vertical conduction

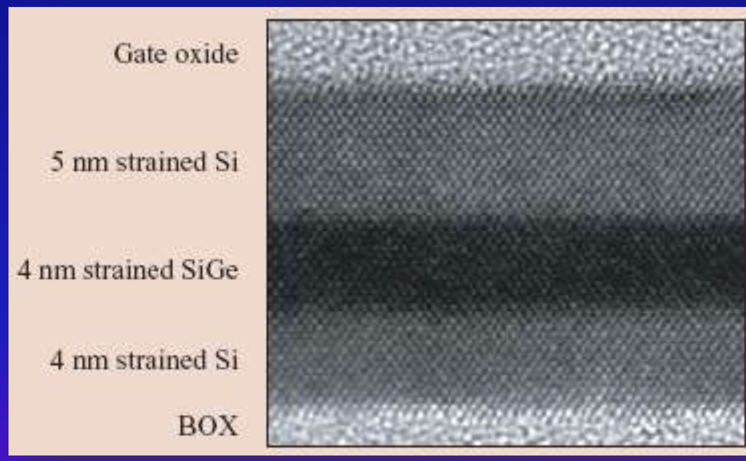
Ref: ITRS

"Strain Engineering"



1% biaxially strained bulk Si

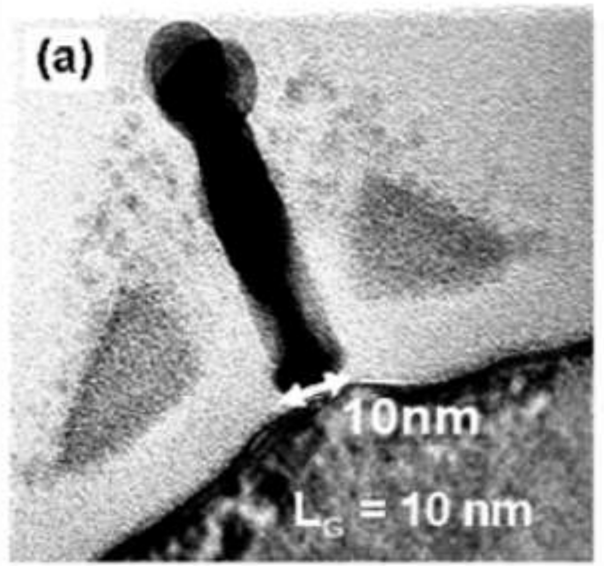


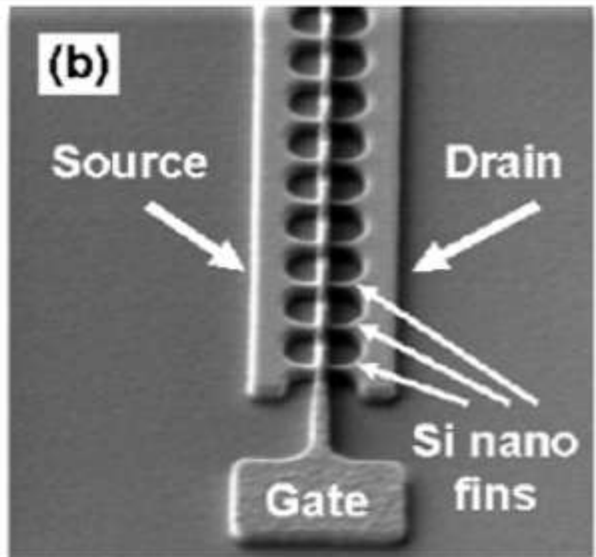


Ref: D.A. Antoniadis, et al, *IBM J. Research and Development*, vol. 50, n.4/5, pp. 363-376, 2006.

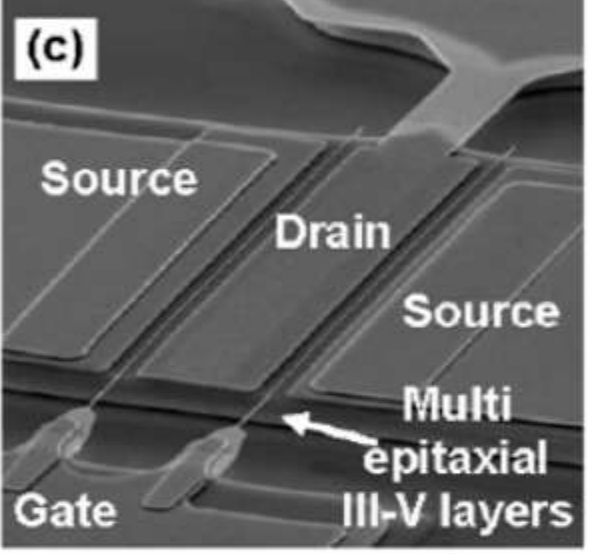
Ref: Rim, et al, *IBM*

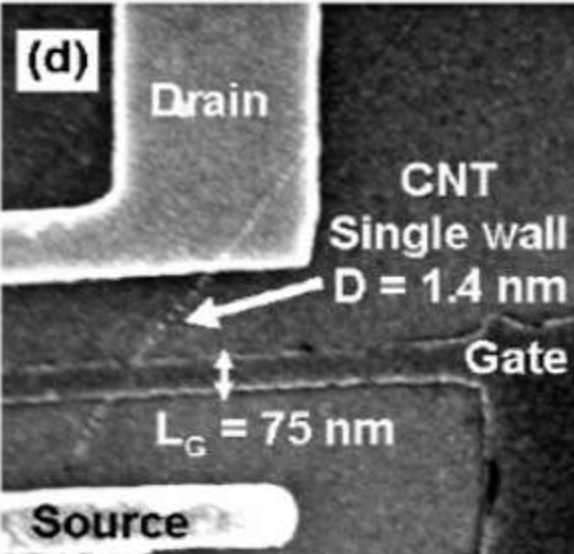
Some examples of emerging nanoscale MOSFETs

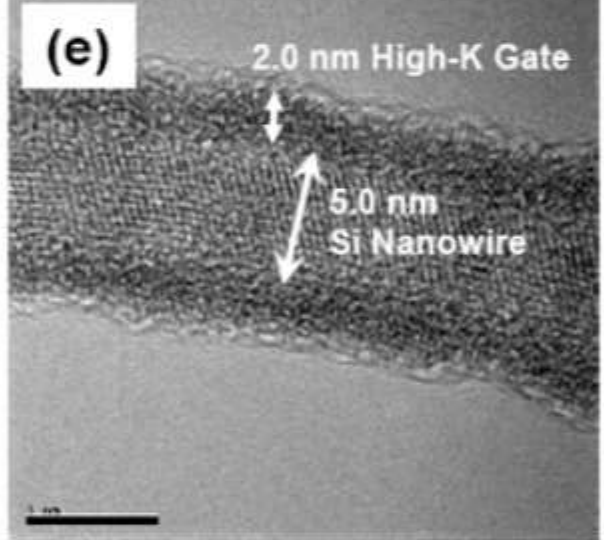




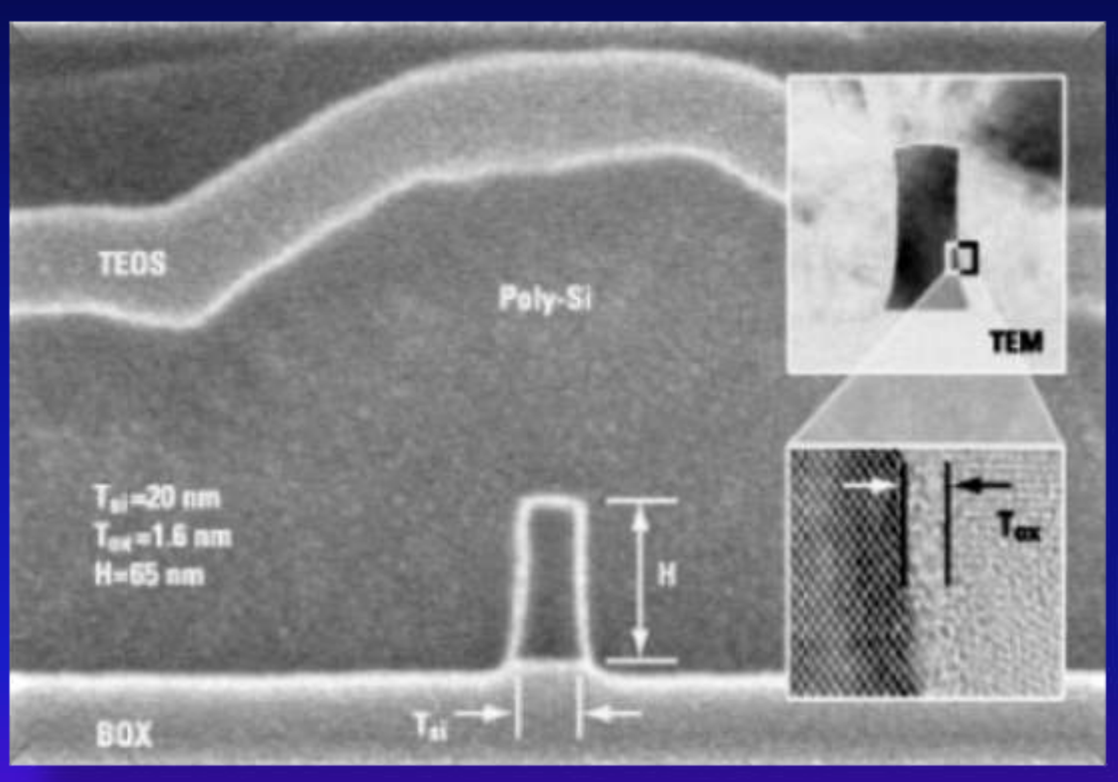
(a) FET planar de 10nm
(b) Tri-Gate FET
(c) QWFET
(d) carbonanotubo
(e) nanoalambre

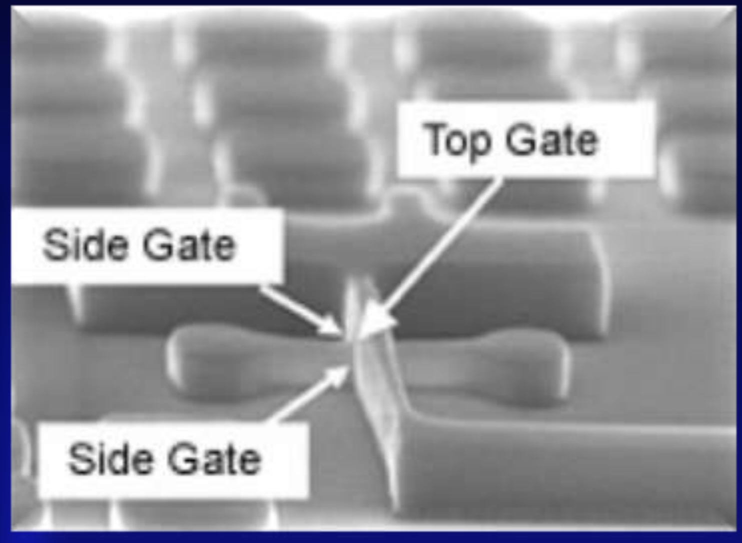






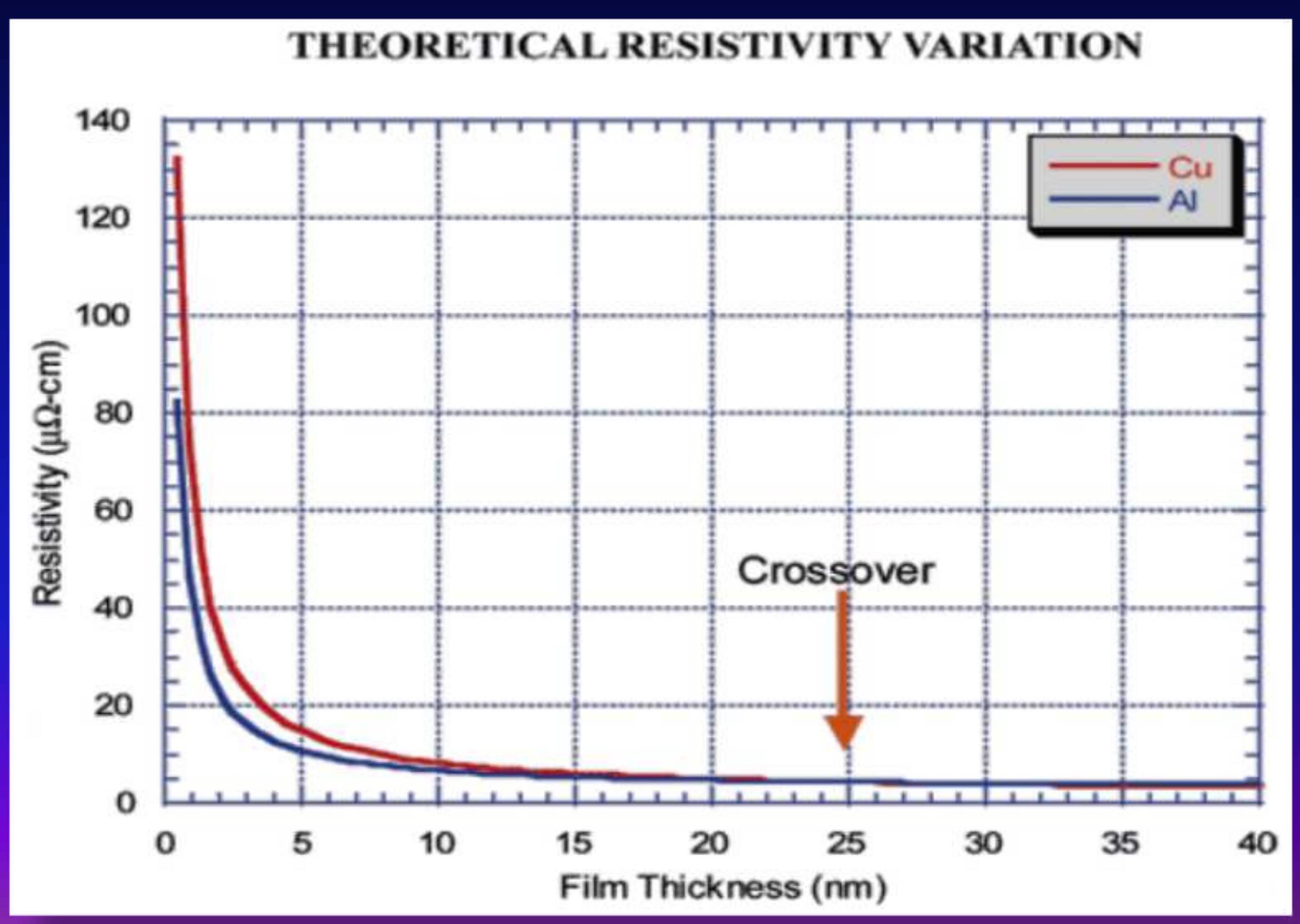
symmetric FinFETs



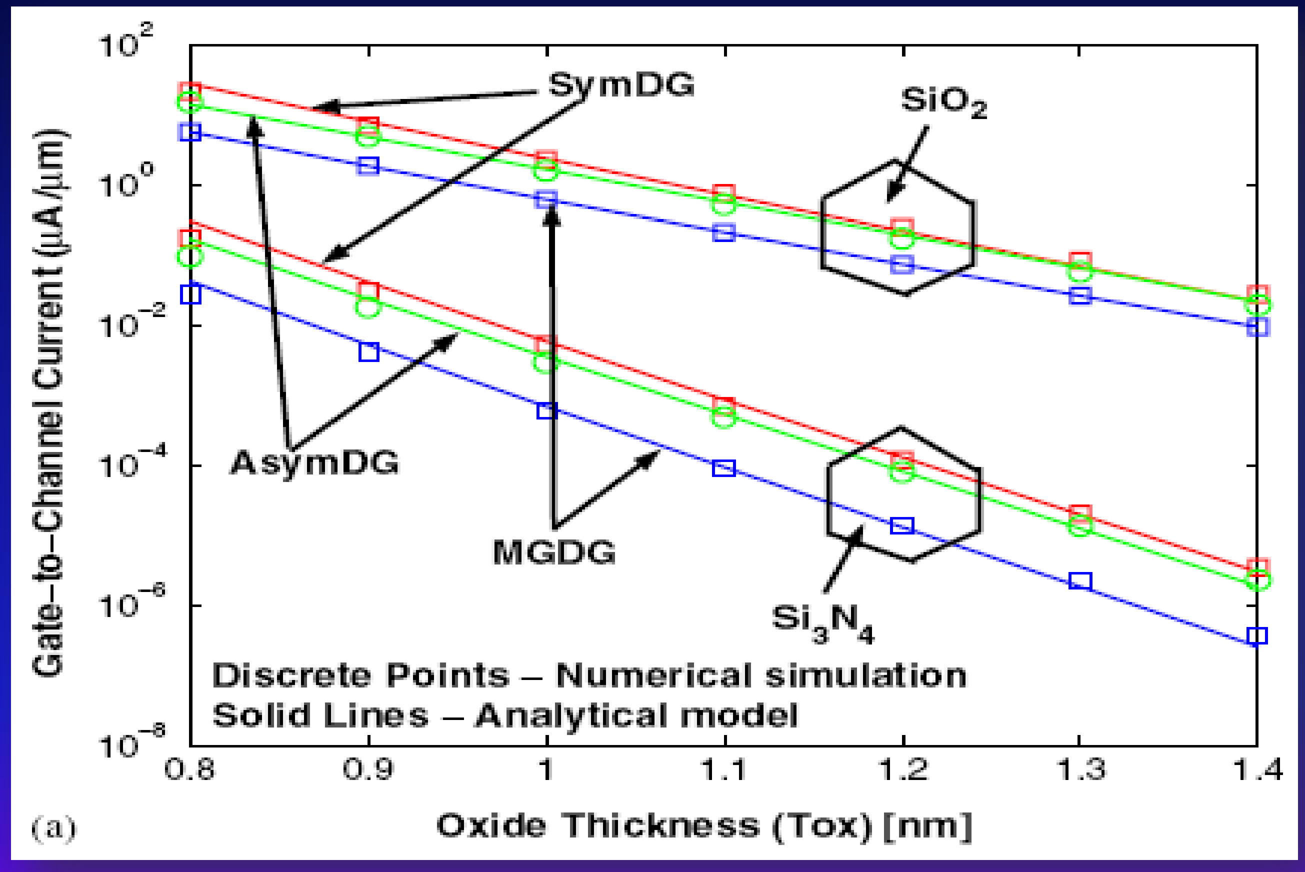


Source: IBM

New problem arises:
Increase of resistivity with shrinking thickness of metal interconnects

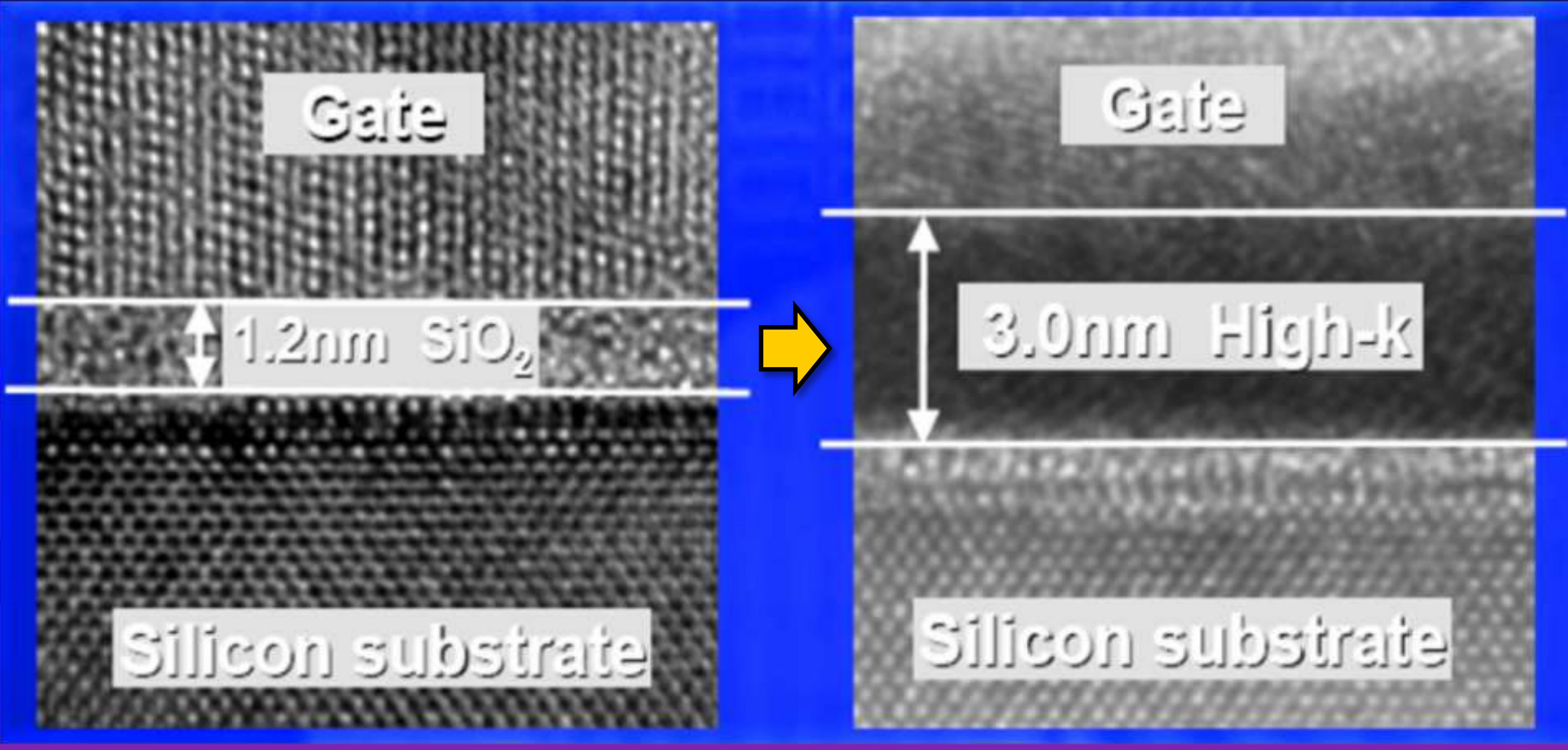


New serious problem: Gate leakage current increases as gate oxide thickness decreases.



Ref: S. Mukhopadhyay, et al, Estimation of gate-to-channel tunneling current in ultra-thin oxide sub-50nm double gate devices, *Microelectronics Journal* (2007)

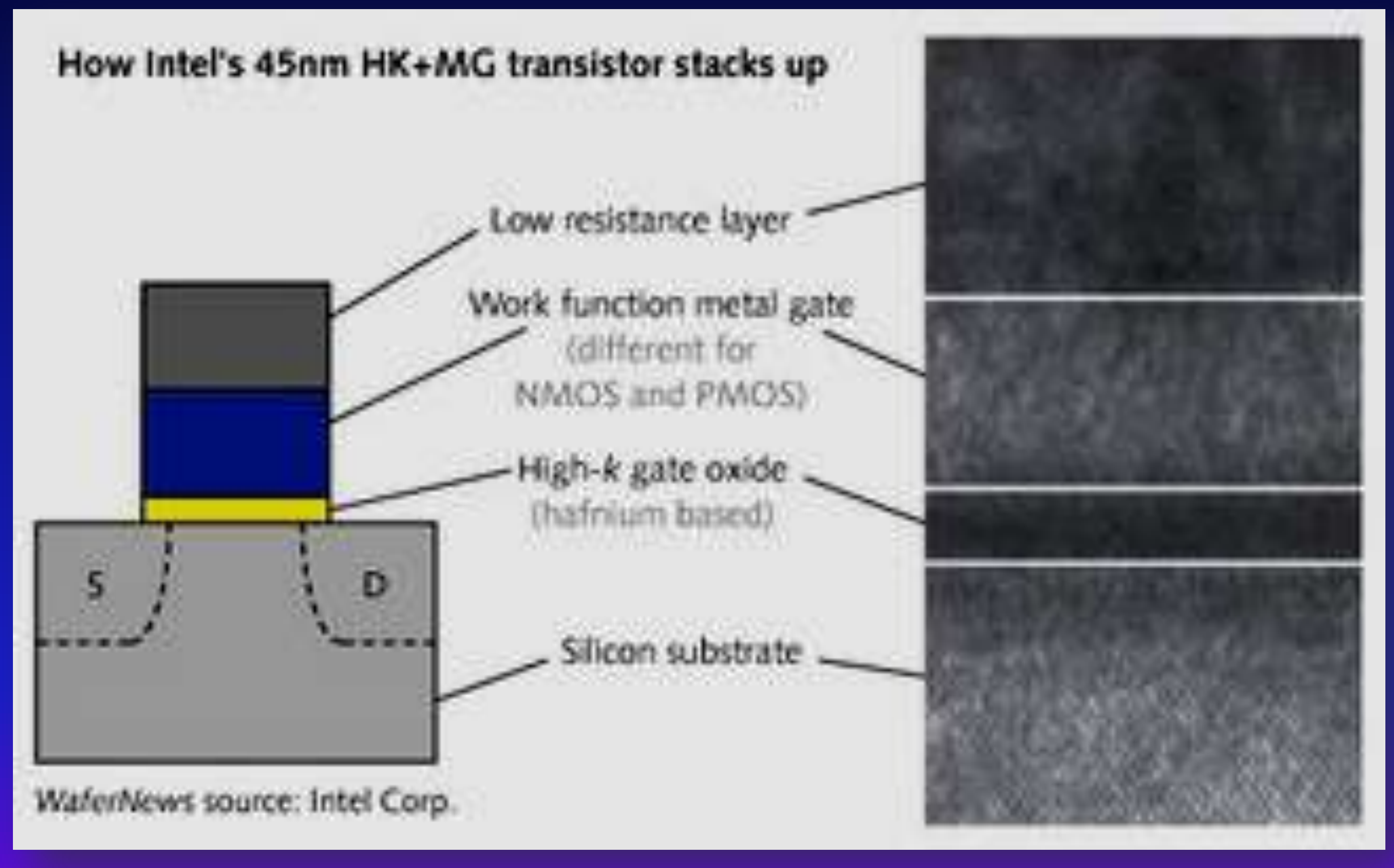
Solution ⇒ replace SiO_2 with thicker dielectrics of higher permitivity than SiO_2



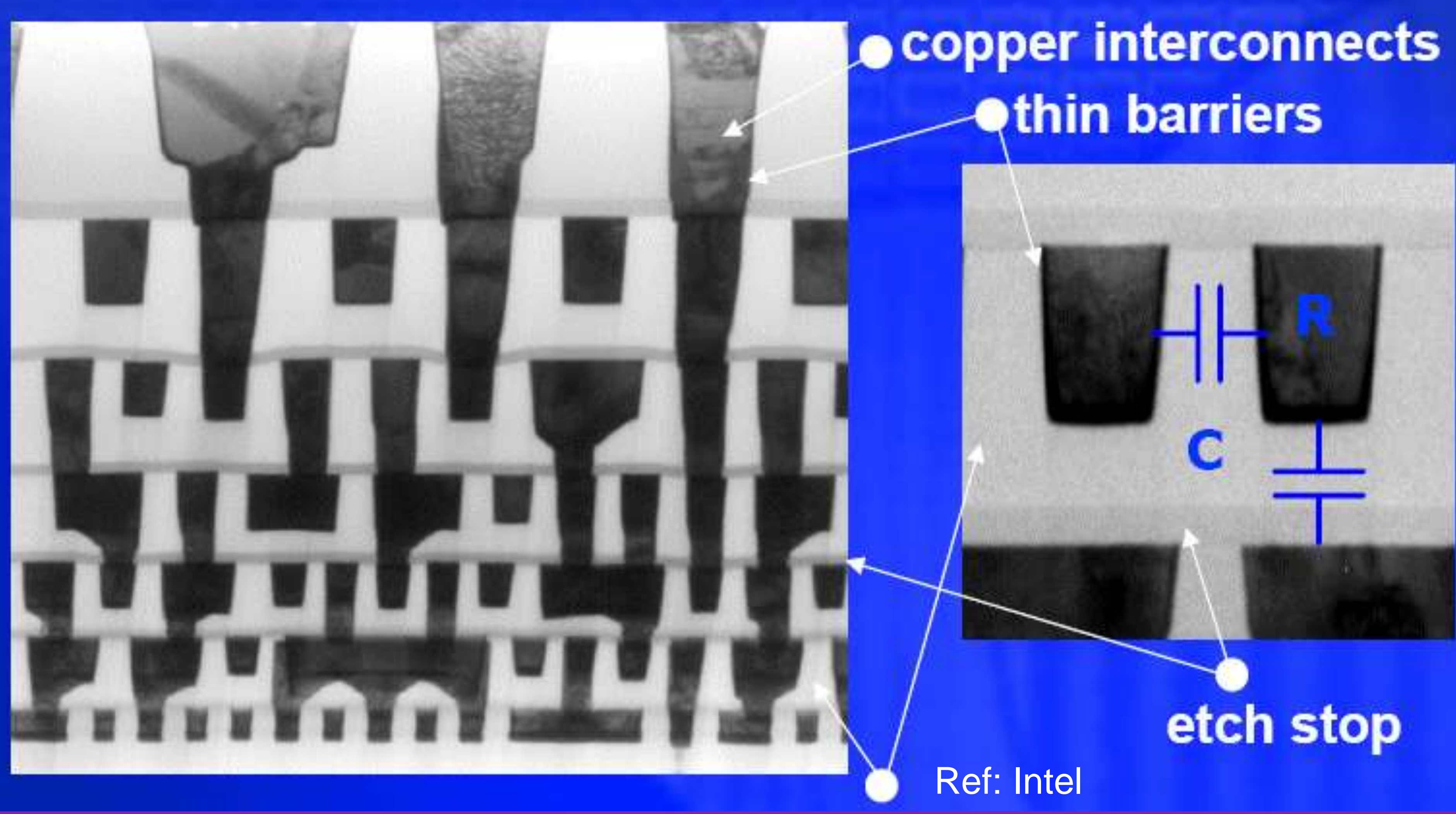
High permitivity (high "*k*") dielectric materials

Dielectric	*Dielectric constant (bulk)*	*Bandgap (eV)*	*Conduction band offset (eV)*	*Leakage current reduction w.r.t. SiO_2*	*Thermal stability w.r.t. silicon (MEIS data)*
Silicon dioxide (SiO_2)	3.9	9	3.5	N/A	>1050°C
Silicon nitride (Si_3N_4)	7	5.3	2.4		>1050°C
Aluminum oxide (Al_2O_3)	~10	8.8	2.8	10^2–10^3 ×	~1000°C, RTA
Tantulum pentoxide (Ta_2O_5)	25	4.4	0.36		Not thermodynamically stable with silicon
Lanthanum oxide (La_2O_3)	~21	6*	2.3		
Gadolinium oxide (Gd_2O_3)	~12				
Yttrium oxide (Y_2O_3)	~15	6	2.3	10^4–10^5 ×	Silicate formation
Hafnium oxide (HfO_2)	~20	6	1.5	10^4–10^5 ×	~950°C
Zirconium oxide (ZrO_2)	~23	5.8	1.4	10^4–10^5 ×	~900°C
Strontium titanate ($SrTiO_3$)		3.3	−0.1		
Zirconium silicate ($ZrSiO_4$)		6*	1.5		
Hafnium silicate ($HfSiO_4$)		6*	1.5		

High "*k*" dielectric & Metal Gate



Shrinking sizes also aggravate the problem of: interconnect capacitance

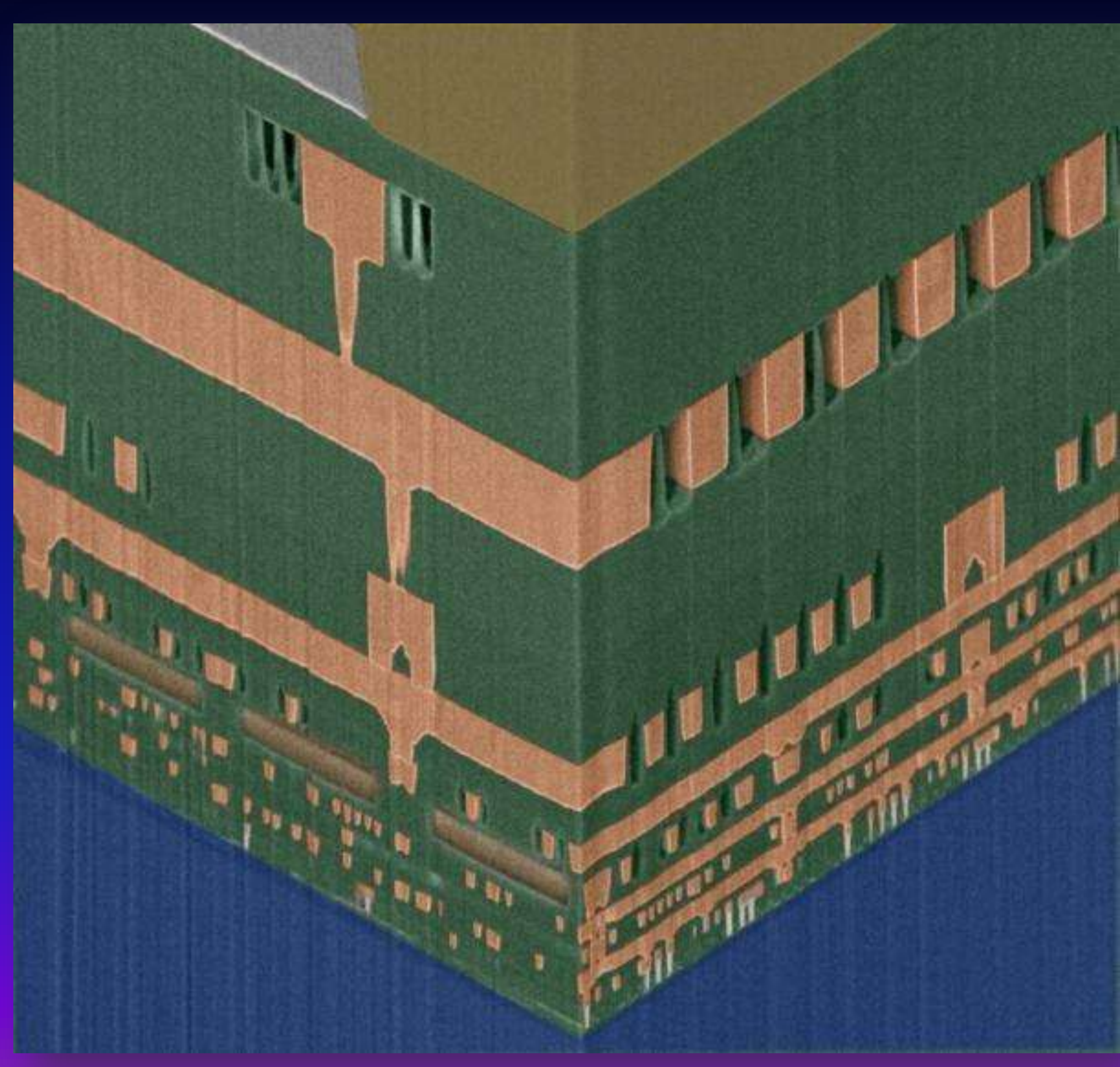


Solution: Low permitivity dielectrics ("Low *k*")

To reduce the capacitance between lines:
Use insulators with smaller effective permitivity than SiO_2 (k=3,9).

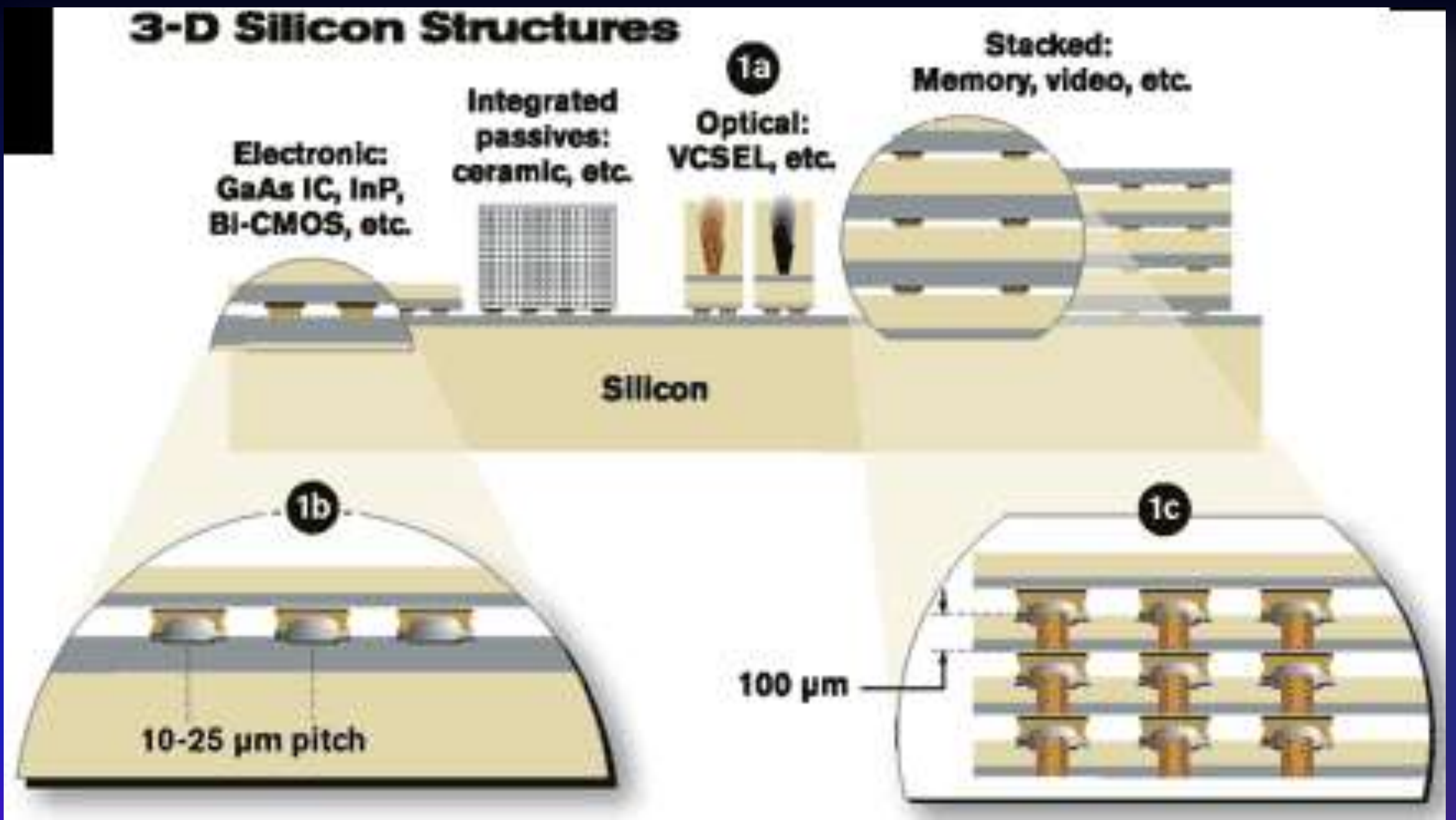
One possible way is to use “air”

IBM has started to use what they refer to as: “air-gap” technology (k=1)



Ref: IBM

3D ICs

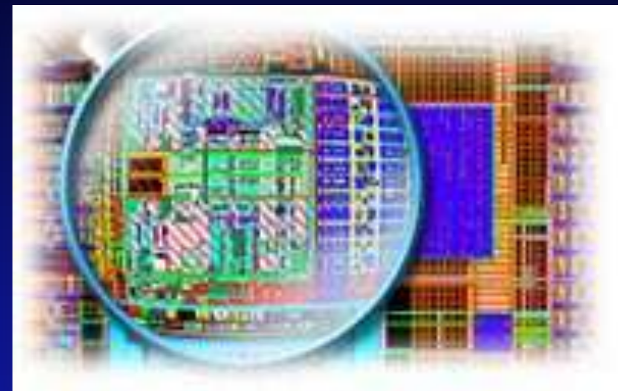


(a) 3-D silicon structures types, (b) fine-pitch die-to-die wafer post-to-pad joining method, (c) die-to-die stacking with TSVs (through-silicon via) can be combined with the post-to-pad joining.

Ref: A. Keigler, et al, Enabling 3-D Design, *Semiconductor International*, 8/1/2007

Systemic Integration high level 3D

"System-On-Chip" (SOC)
"System-In-Package" (SIP)
"Package-on-Package" (POP)



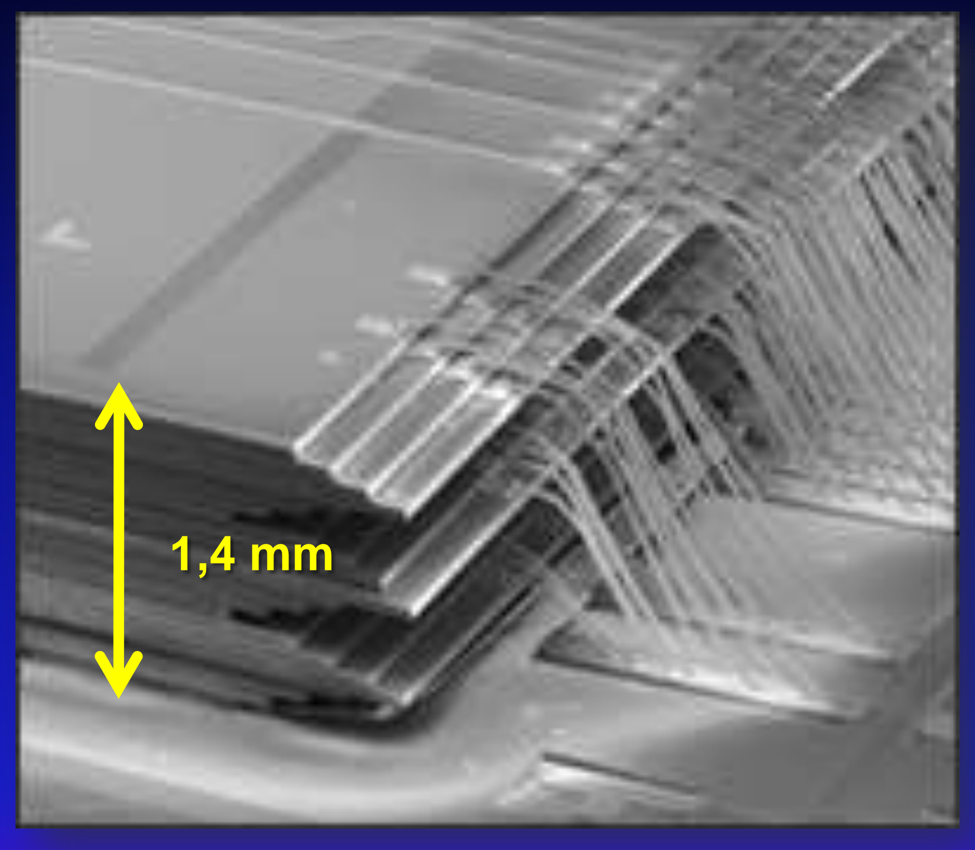
Ref: STMicroelectronics

A WLAN SiP
Ref: Agere Systems

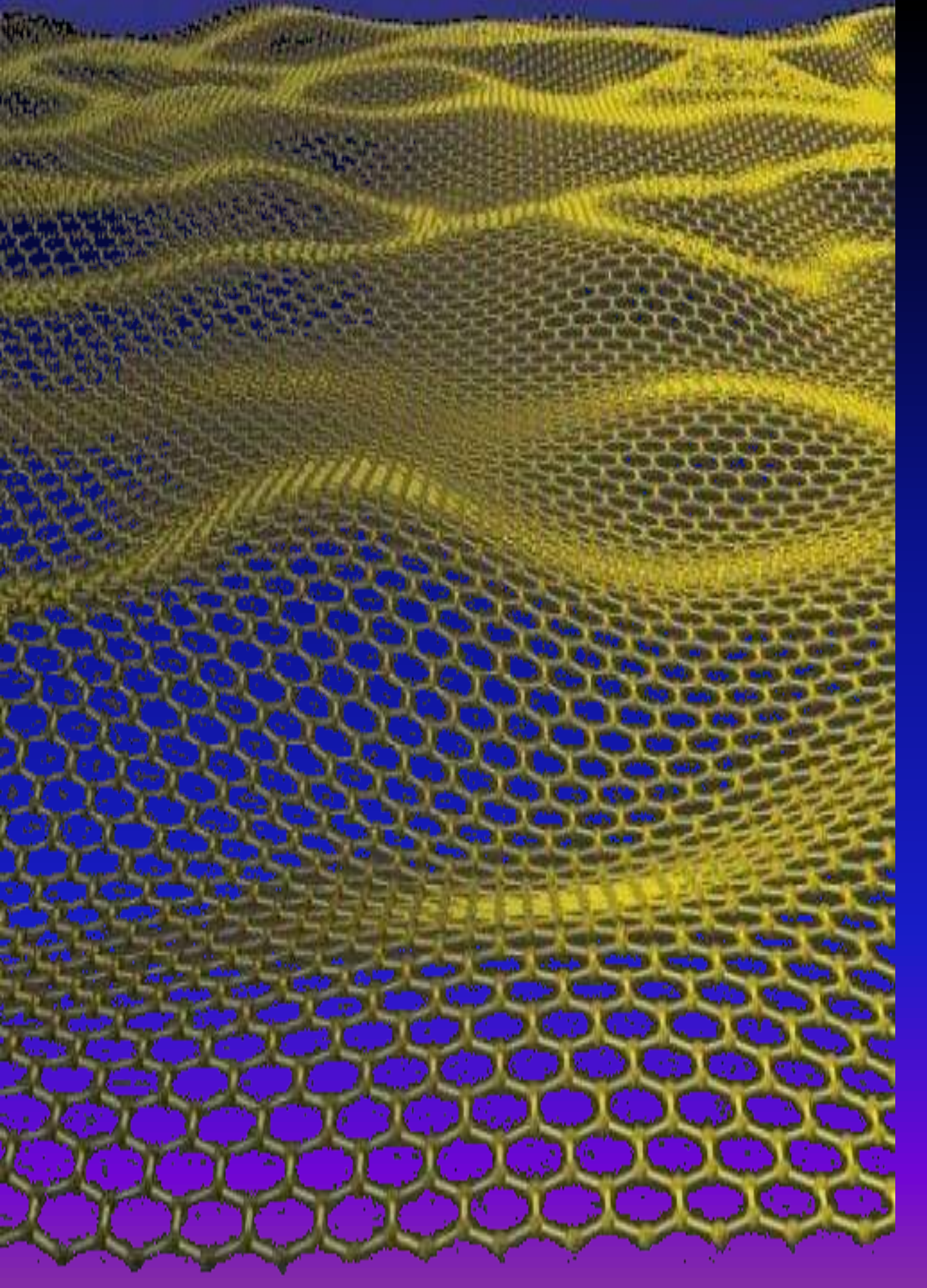
A 0.8-mm-thick four-high DRAM package-on-package (PoP) stack. (Ref: Tessera Inc.)

Even more 3D integration

Multichip package with 384GB of memory, fabricated by Hinix Semiconductor (korea) made up of 24 chips, each one with 16GB of NAND type flash memory.



Ref: The Korean Times: Biz/Finance - 05 Sept. 2007



New materials

Graphitic materials…

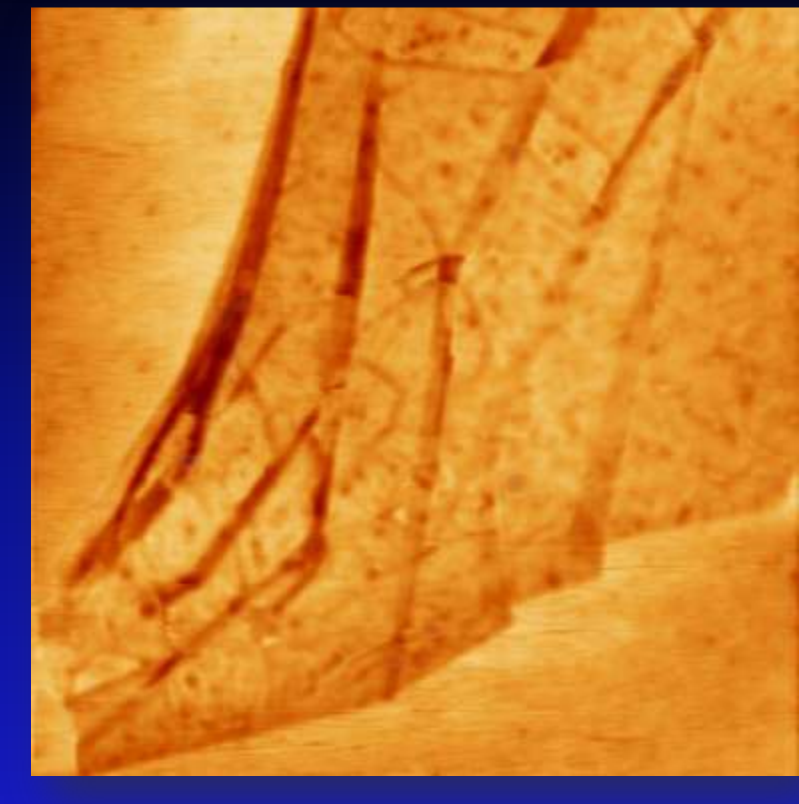
Graphene

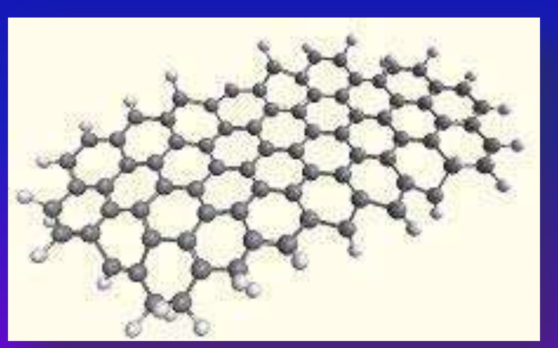
is the structural foundation of other graphitic materials:

- ✓Graphite
- ✓Fullerenes
- ✓Carbon Nanotubes
- ✓Nanoribbons

New materials: Graphene

A planar honeycomb-like hexagonal-cell crystal lattice structure, made up of a one-atom thick single sheet of carbon





Atomic Force Microscope image of a mono-atomic thick carbon nano-layer (3x3μm).

Ref: Mesoscopic Physics Group, Prof. Geim – Univ. of Manchester

New materials: Graphene

The intrinsic mobility of graphene is estimated to be around 200,000 cm^2 V^{-1}s^{-1}

(10,000 cm^2 V^{-1}s^{-1} has been measured)

about 100 times higher than that of Silicon (1500 cm^2 V^{-1}s^{-1}), and over 20 times higher than that of Gallium Arsenide (8500 cm^2 V^{-1}s^{-1}).

Graphene also has exceptional thermal conductivity: 5850 W/mK (50x more than silicon)

Ref: S. V. Morozov, *et al*, Giant Intrinsic Carrier Mobilities in Graphene and Its Bilayer, *Phys. Rev. Lett*. 100, 016602 (2008)

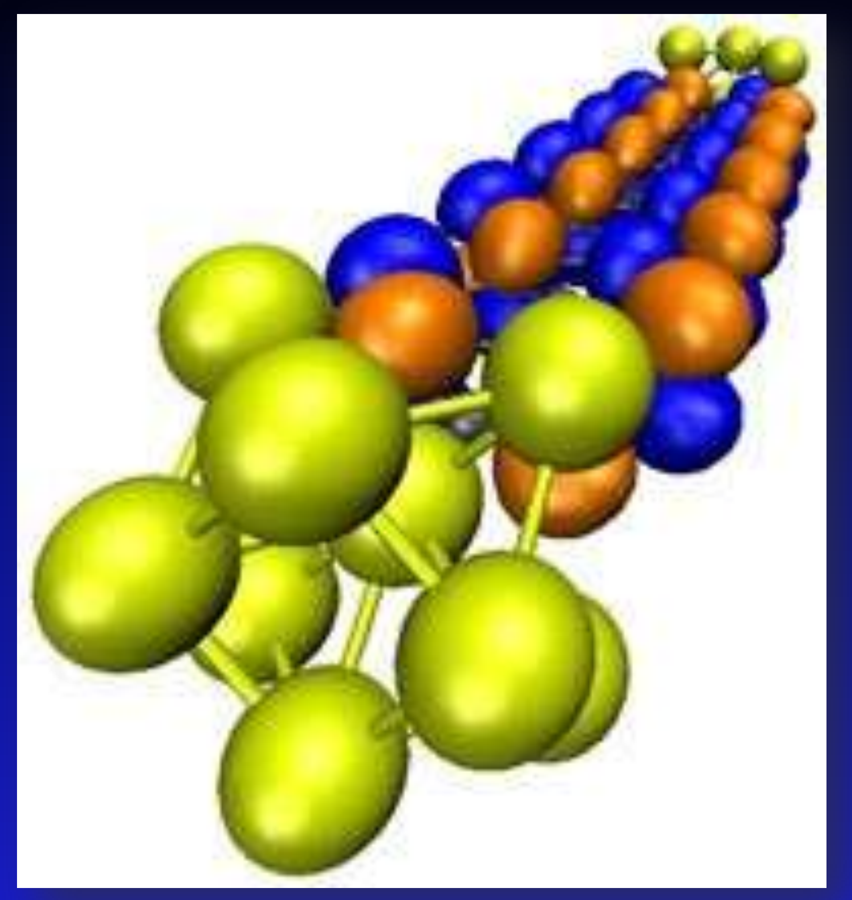
New materials: Planar Graphene FET

80nm Size

Ref: Georgia Institute of Technology (2006)

New materials:

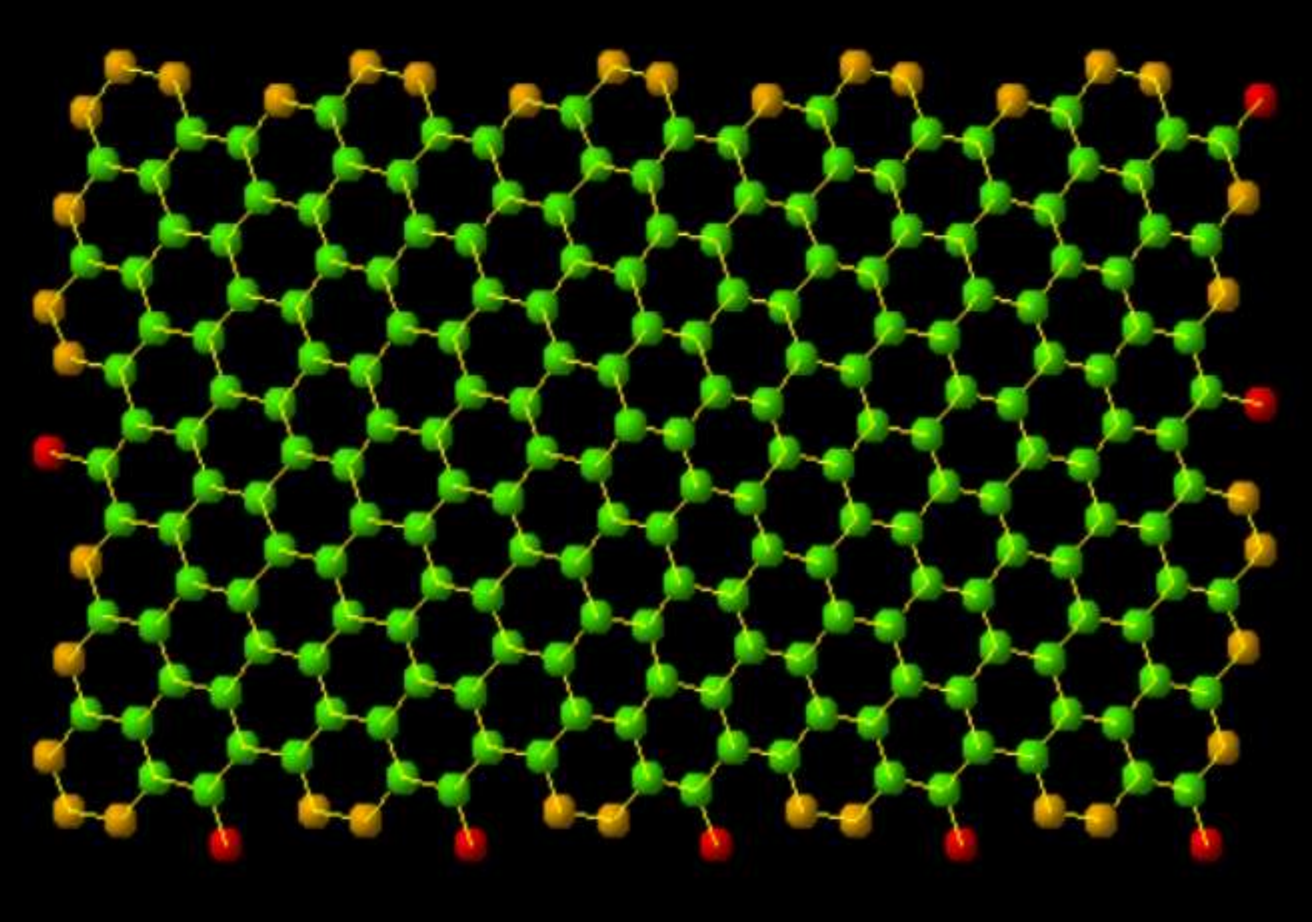
Another possible use of graphene: as highly conductive interconnect



Sketch of graphene nanoribbon interfaced with gold contacts

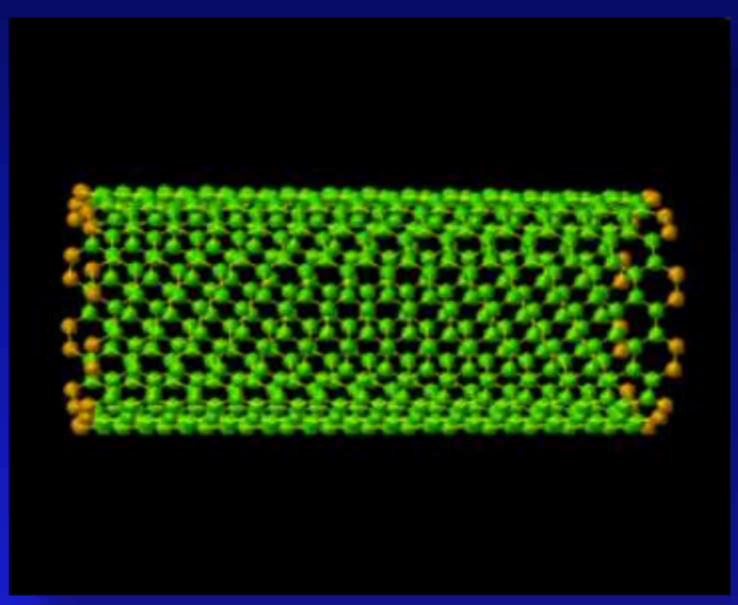
Ref: P. Shemella, at al, Energy gaps in zero-dimensional graphene nanoribbons, *Appl. Phys. Lett.* 91, 042101 (July 23, 2007)

Rolled up Graphene:
Carbon Nano Tubes (CNTs)



CNTs

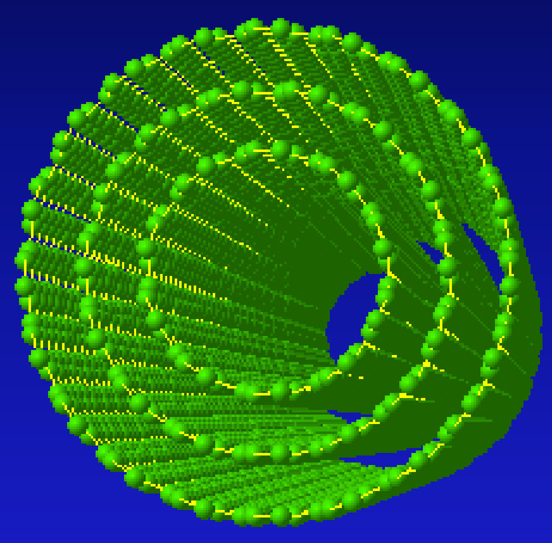
Single-wall



Diameter = 0.35 - 2 nm

Typical lengths: 1~100 μm

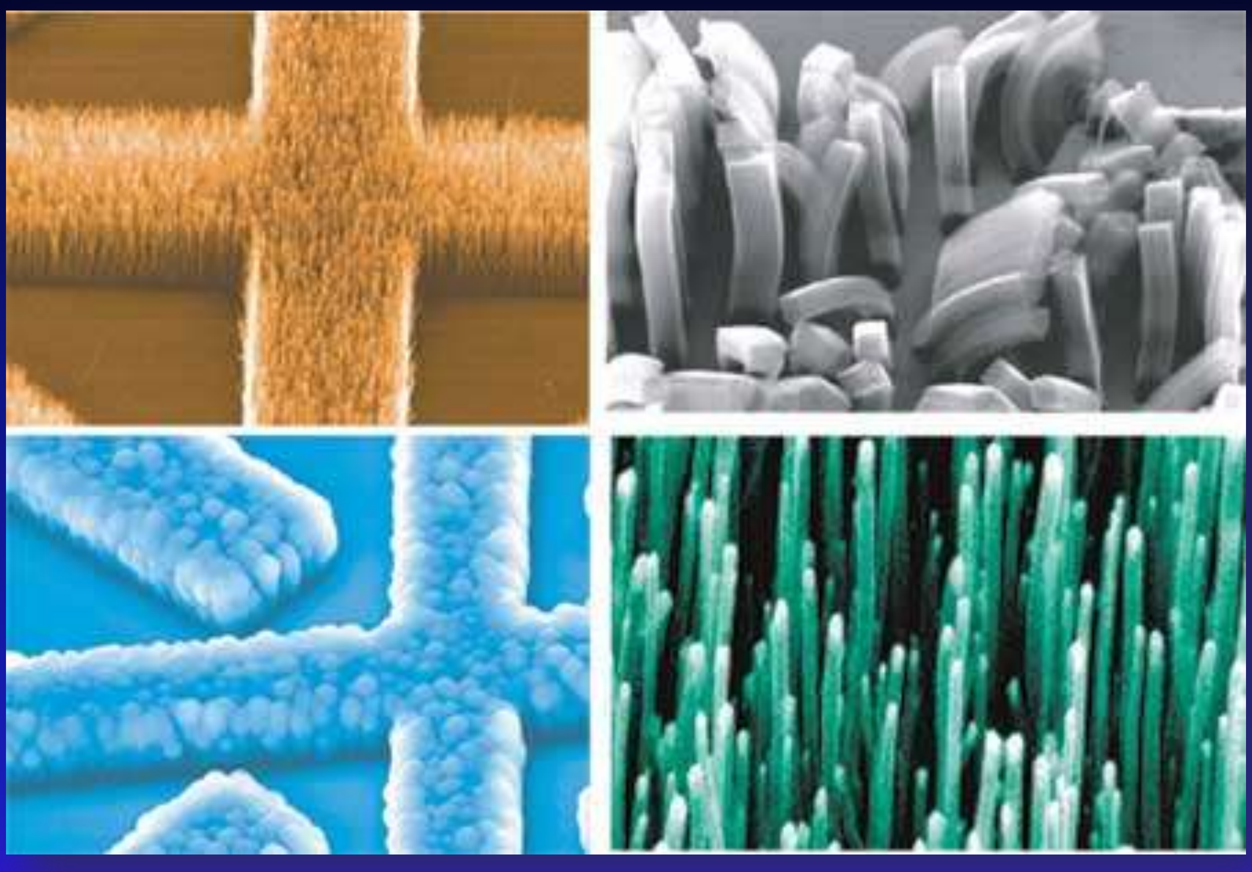
Multi-wall



Diameter = 3 - 50 nm

Interlaminar spacing: ~0.34 nm
(similar to Graphite's spacing)

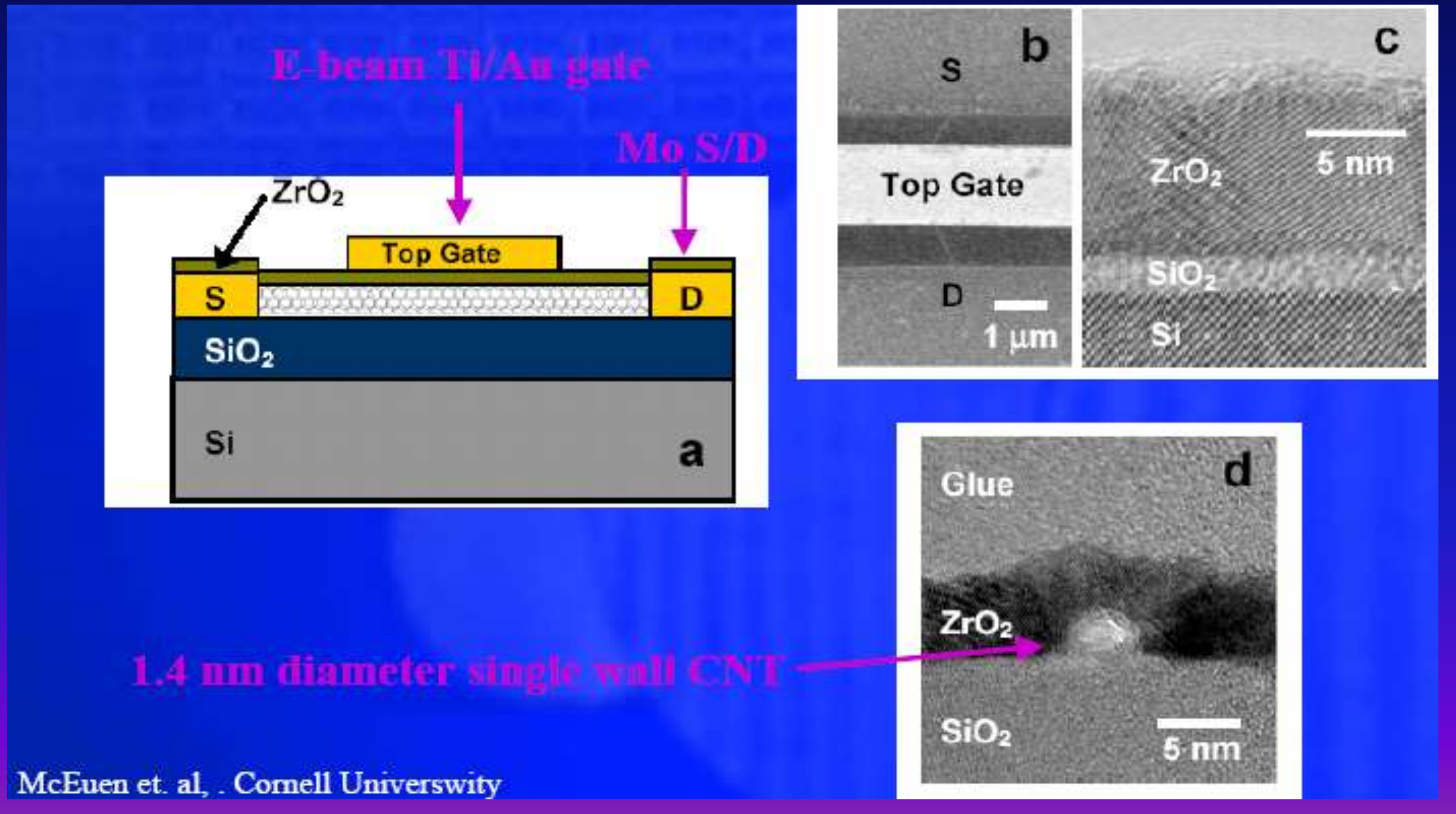
CNTs



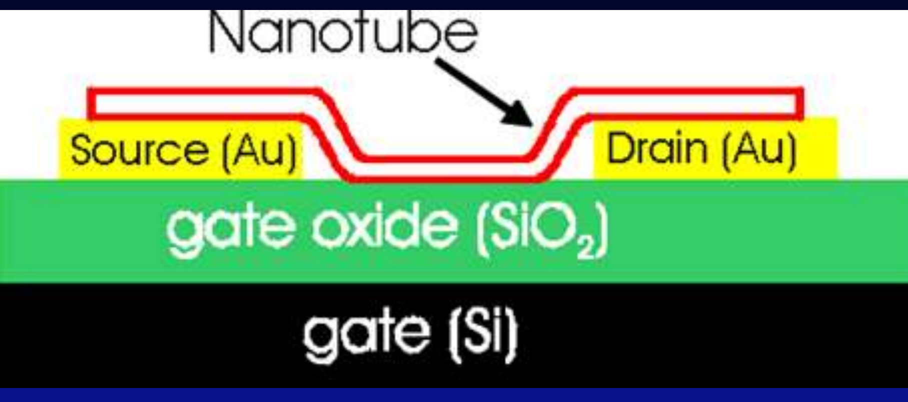
Photos from NASA

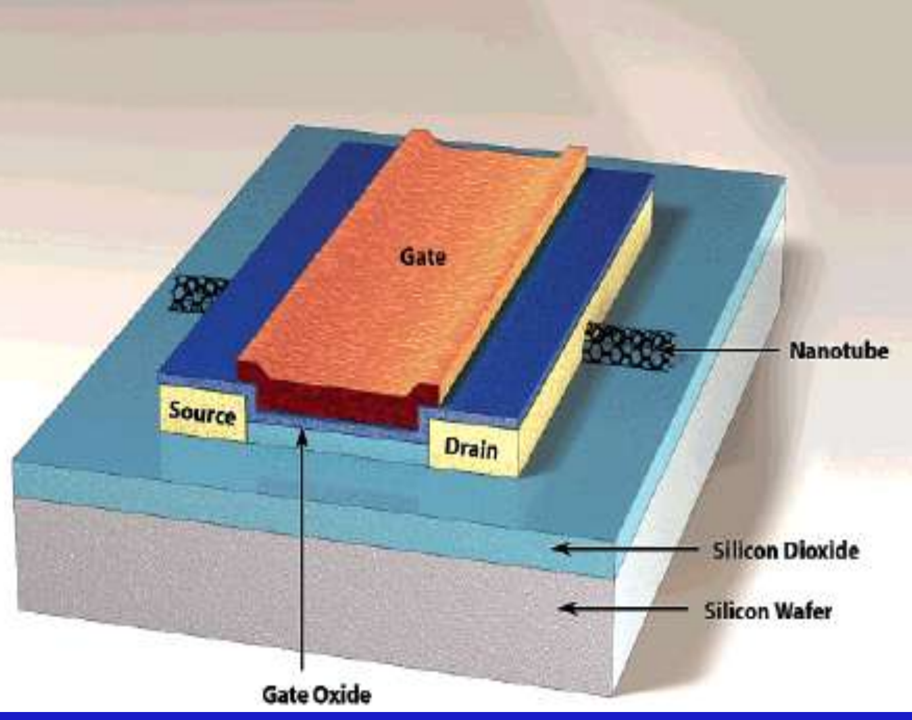
Some people claim that CNT transistors should be capable of operating at THz frequencies.

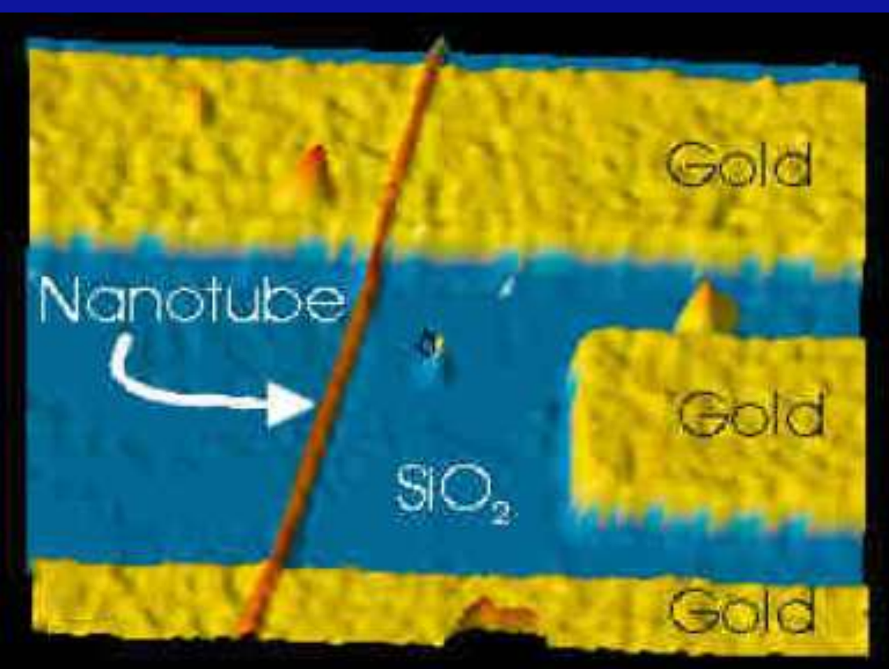
Field Efect Transistor using Carbonanotube (CNT)



Another CNTFET

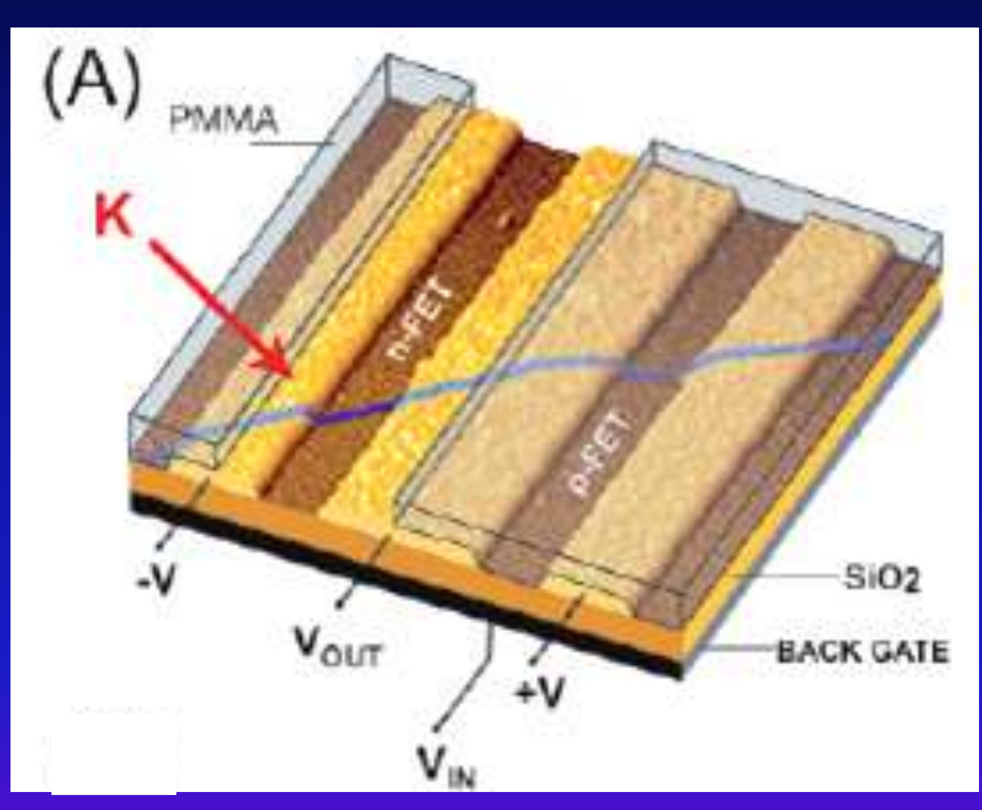


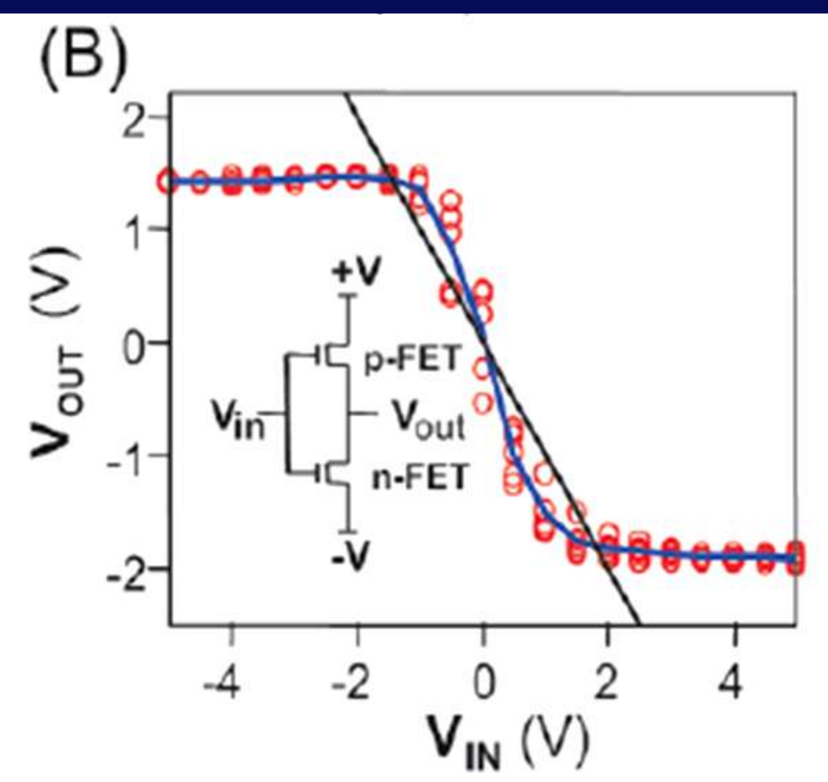




Ref: IBM

A CNTFET logic gate

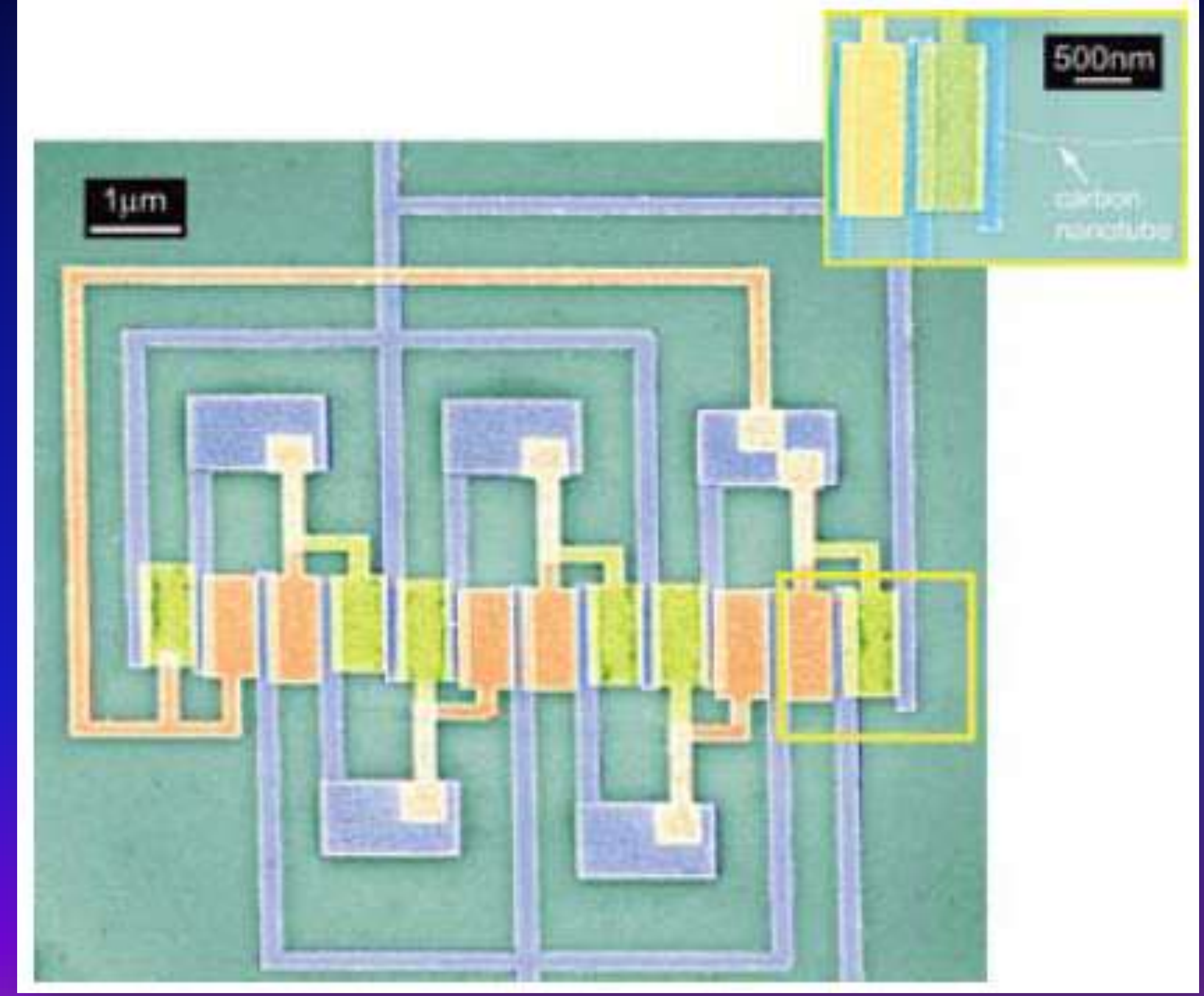




Ref: IBM

Integrated Circuit with 12 CNTFETs (ring oscillator)

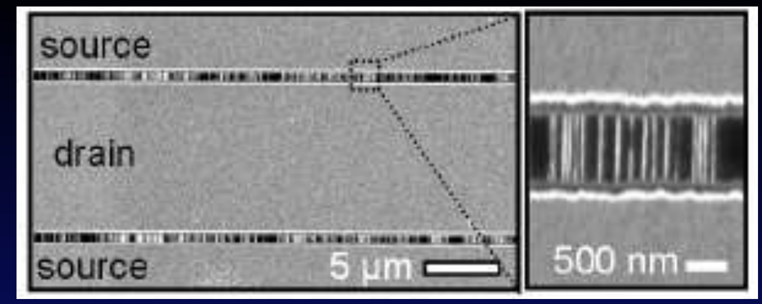
CNT length =18nm
CNT diameter =1nm

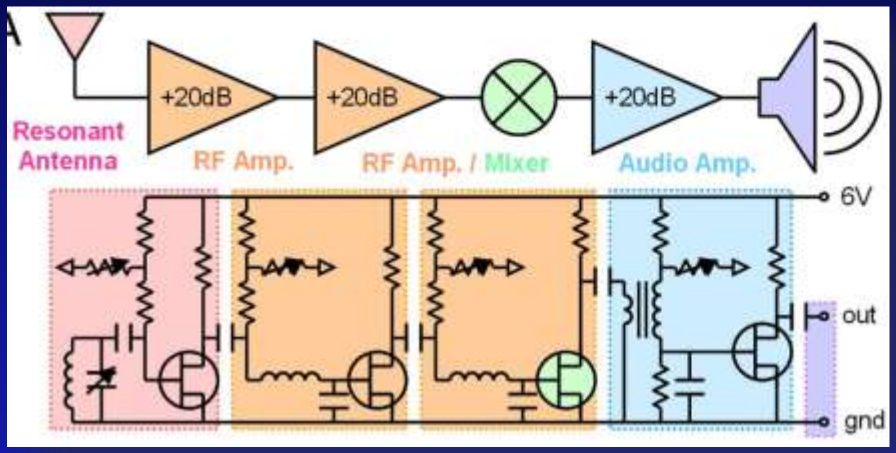


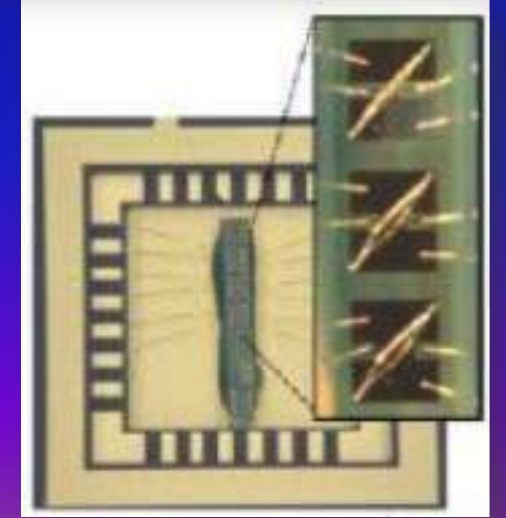
Ref: IBM (2006)

CNT radio

in which parallel, aligned arrays of Single-Wall NT devices provide all of the key functions, including resonant antenna, two fixed RF amplifiers, an RF mixer, and an audio amplifier.



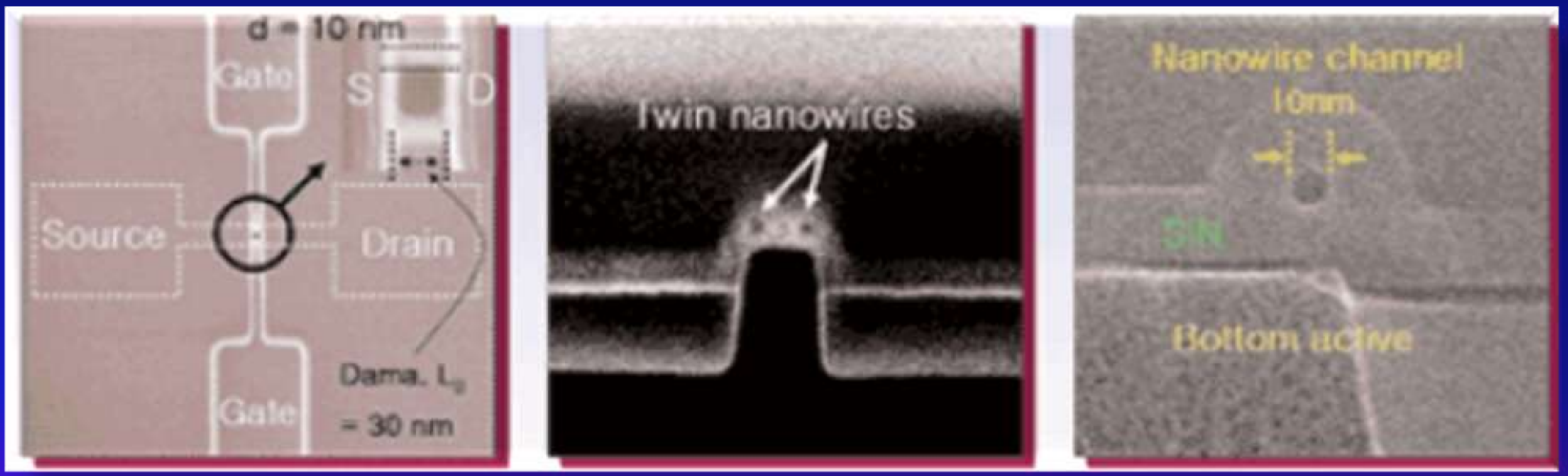




Ref: C. Kocabas, *et al*, Radio frequency analog electronics based on carbon nanotube transistors, *Proc Nat Acad Sci,* February 5, 2008 vol. 105, no. 5, 1405–1409.

Silicon nanowire Transistor

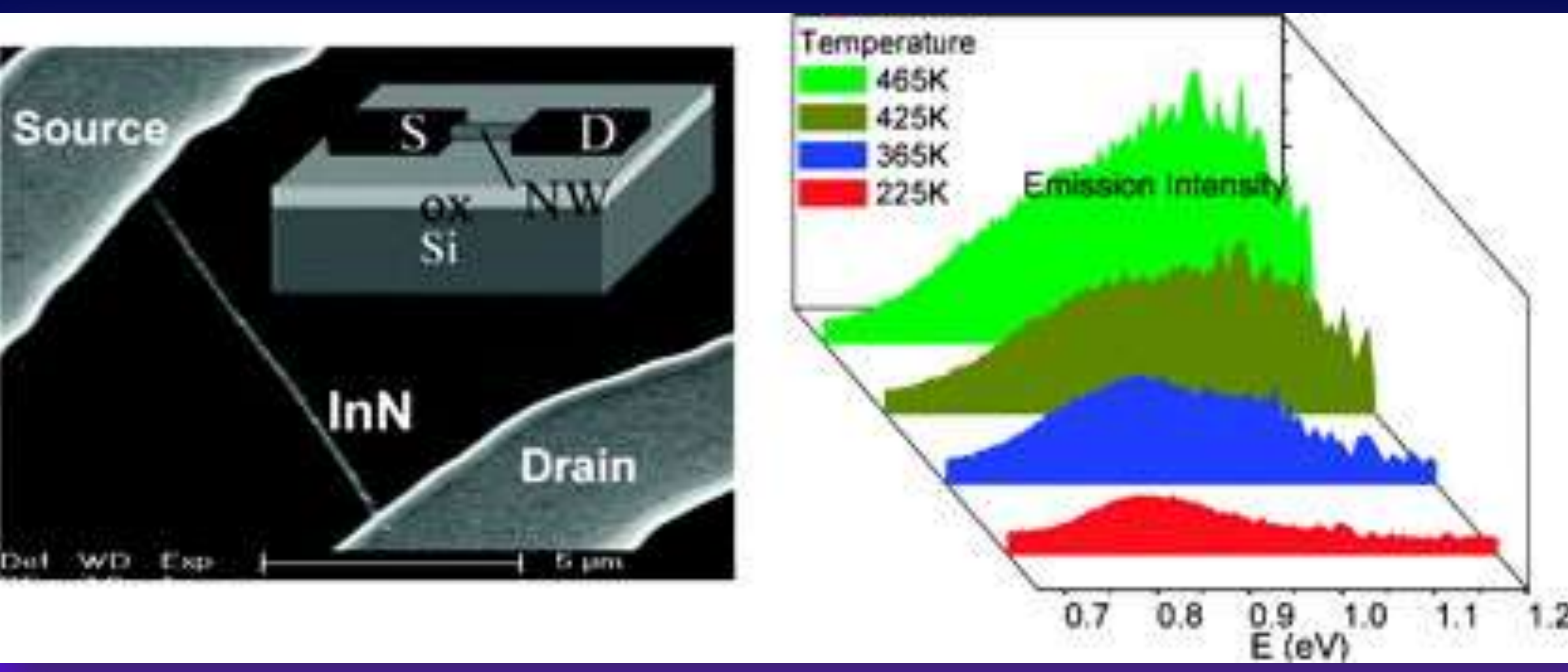
diameter = 10nm



Ref: Samsung (2006)

infrared emitter

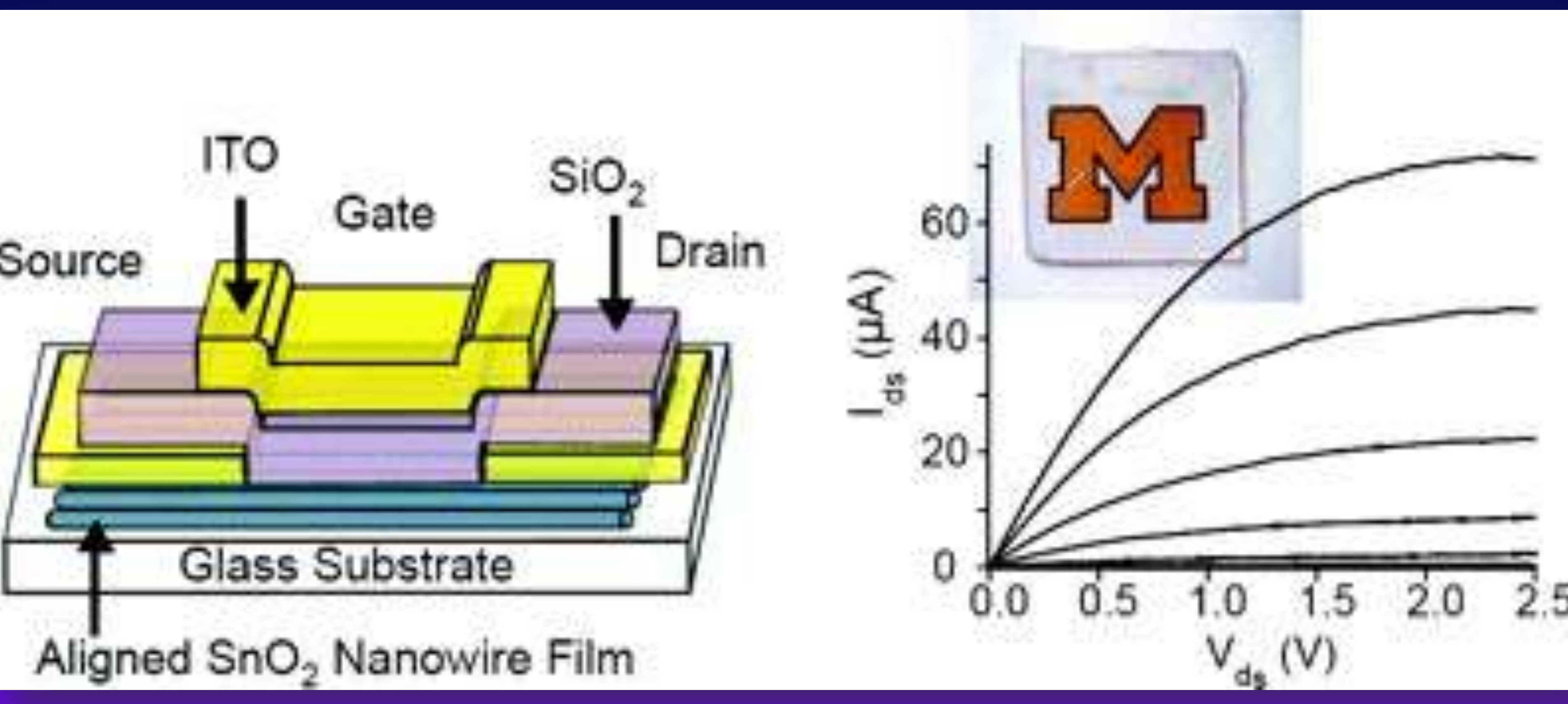
Indium Nitride nanowire over Silicon



diameter = 100nm
Length = 10µm

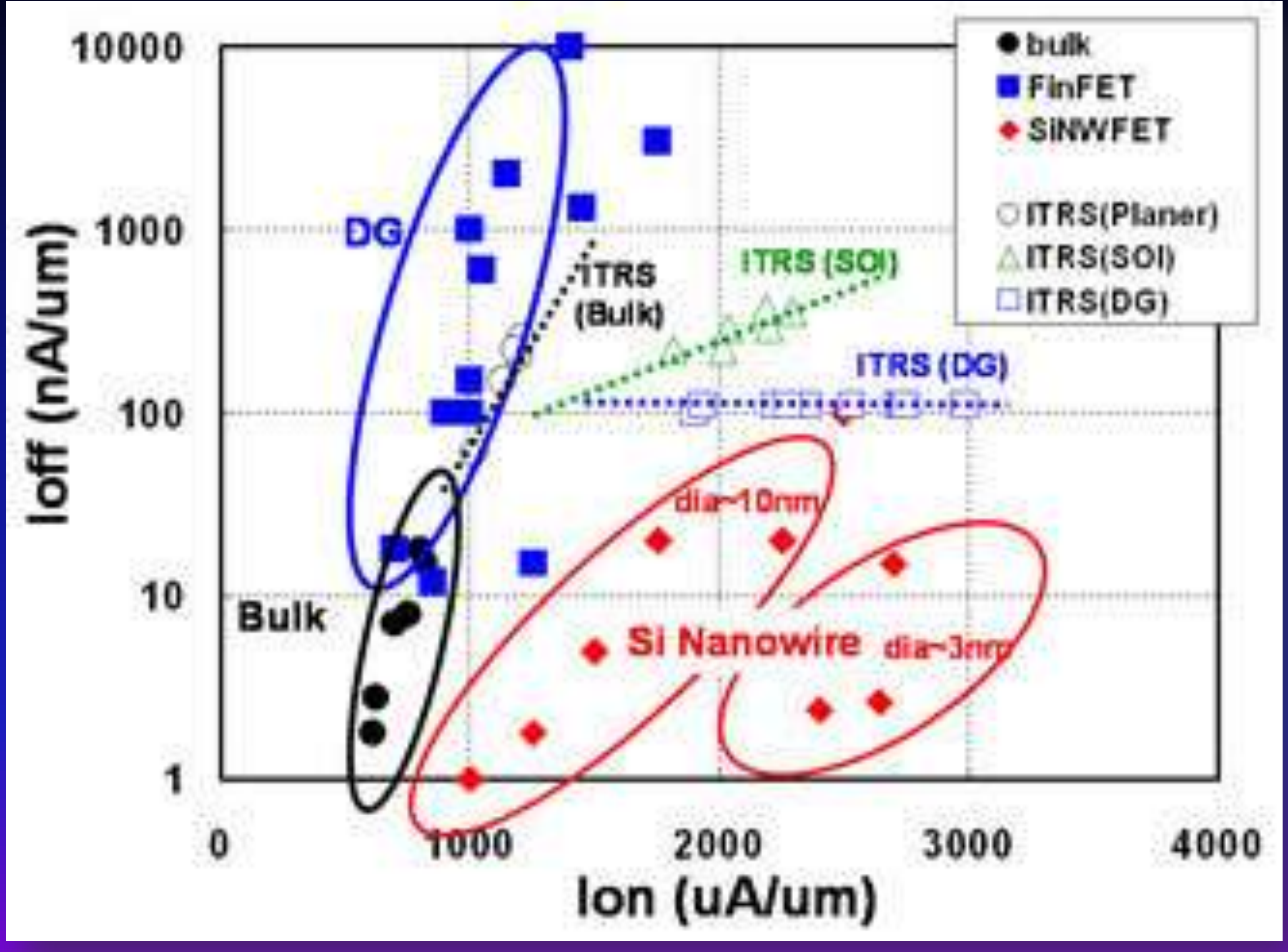
Ref: IBM Research (2007)

transparent TFT:
Tin Oxide nanowires (doped with Ta)



Ref: Fully Transparent Thin-Film Transistor Devices Based on SnO_2 Nanowires, E.N. Dattoli, et al, *Nano Lett.*, 7 (8), 2463 -2469, 2007.

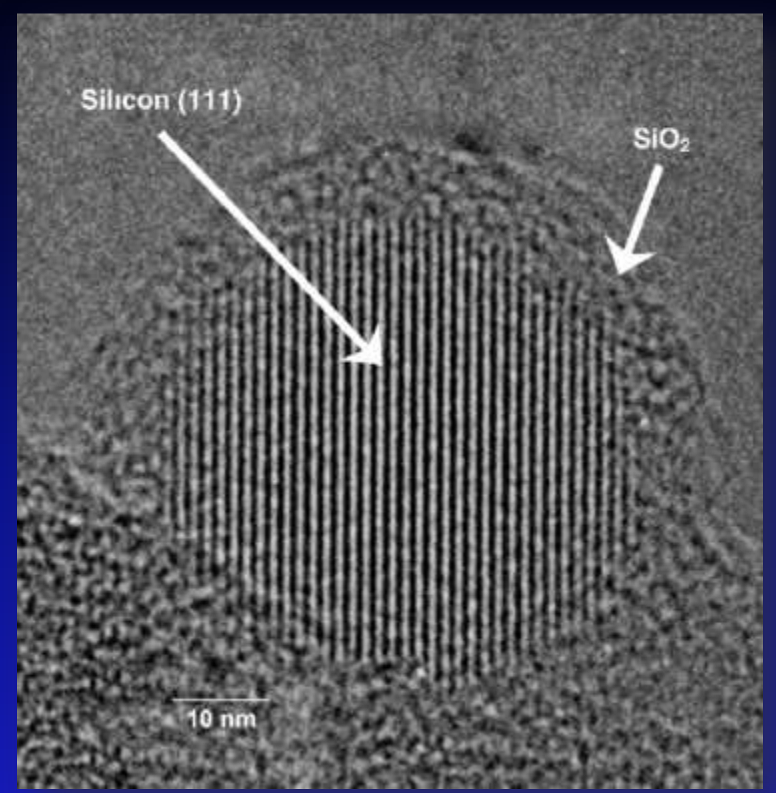
Nanowire FETs to keep off current down:

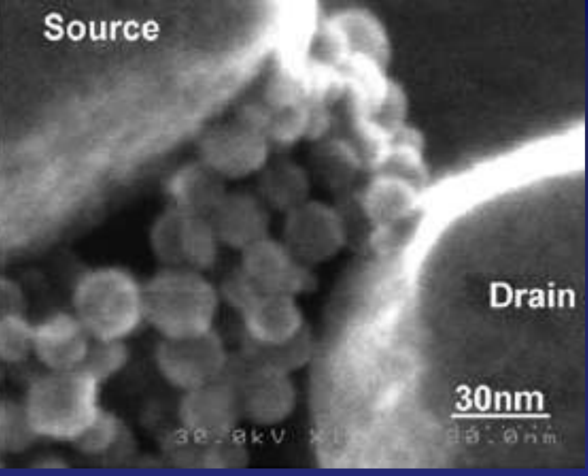


Ref: Hiroshi Iwai, 4th Intl Symp. Advanced Gate Stack Technol., 2007.

Some examples of even more exotic concepts

Silicon nanodots (SiNDs)



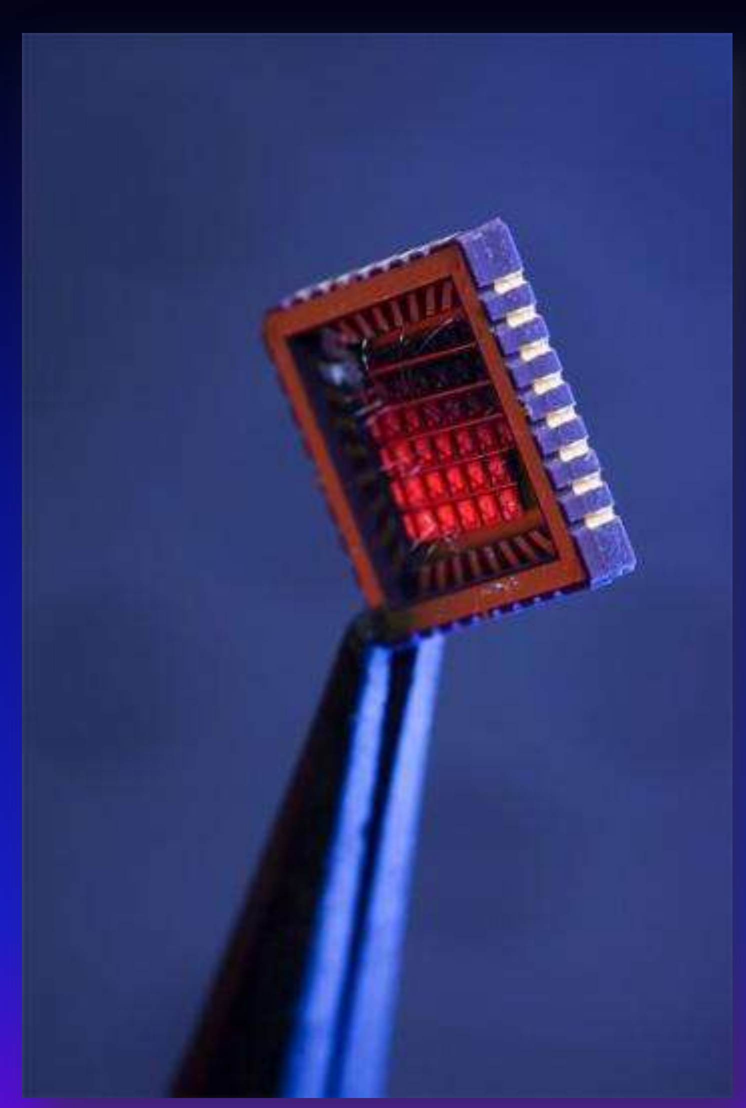


TEM image of a crystalline SiND covered with a thin layer of SiO_2

SiNDs assembled over nano-electrodes

Ref: H. Mizuta, S. Oda, Bottom-up approach to silicon nanoelectronics, *Microelectronics Journal* (2007), in press, doi:10.1016/

Spintronics



"Spin Transport Electronics" is a radical alternative to Electronics.

Logic operations with much less energy consuption.

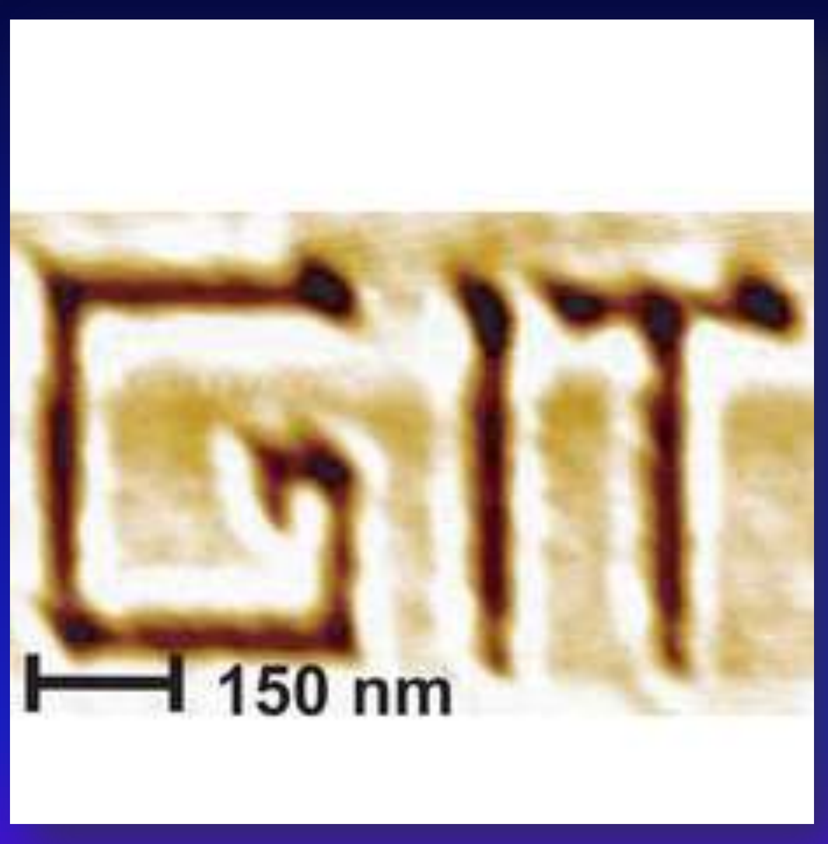
World's first Silicon spin transport device: a Silicon spin field-effect transistor (spinFET), University of Delaware & Cambridge NanoTech, Inc., Mass., US.

Ref: B. Huang, D.J. Monsma, I. Appelbaum, Experimental realization of a silicon spin field-effect transistor, *Appl. Phys. Lett*. 91, 072501 (2007)

New concepts for Nanolithography

An example: TCNL

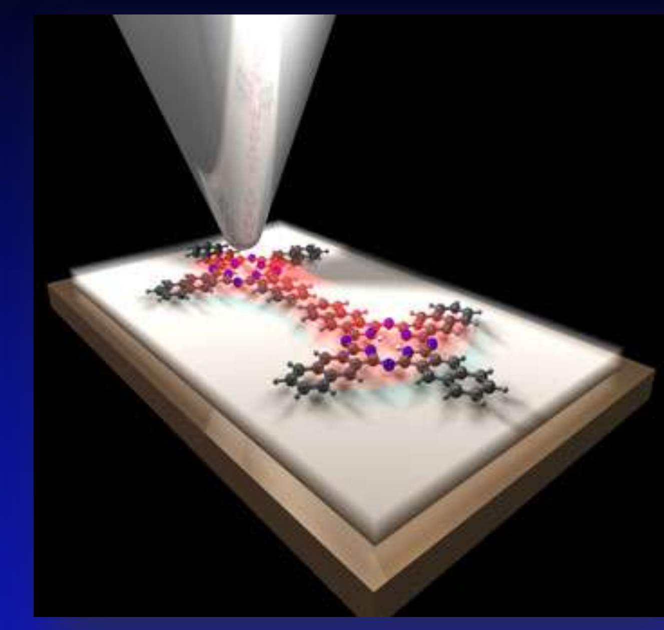
"Thermochemical Nanolithography", Presently being developed at the Georgia Institute of Technology, it uses an atomic force microscope (AFM) to induce by heating a chemical reaction on a polymeric film deposited over the Si surface. Speeds of mm per second have already been achieved.

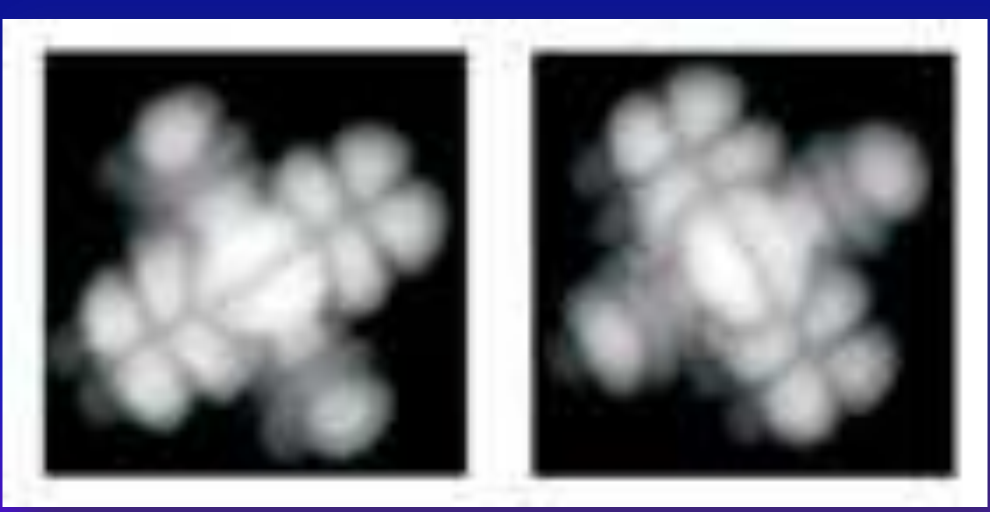


Ref: Georgia Tech. (2007).

Molecular switching

IBM Researchers have discovered a molecular material that may be switched, openning the possibility of building logic circuits.





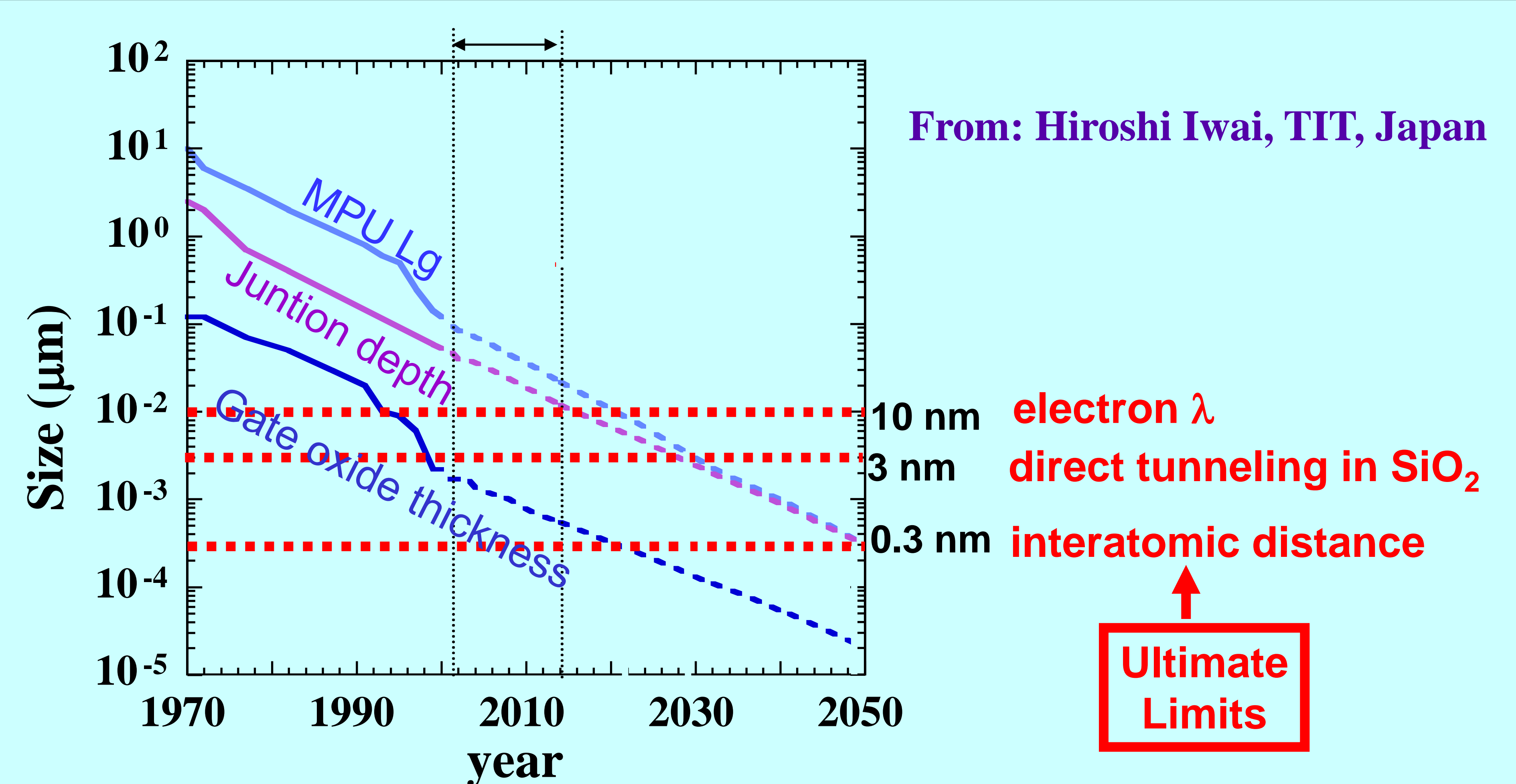
STM images of the molecule “naphthalocyanine” in the"on" and "off“ stetes.

Ref: IBM Zurich Research Laboratory (30 Aug 2007).

Conclusions

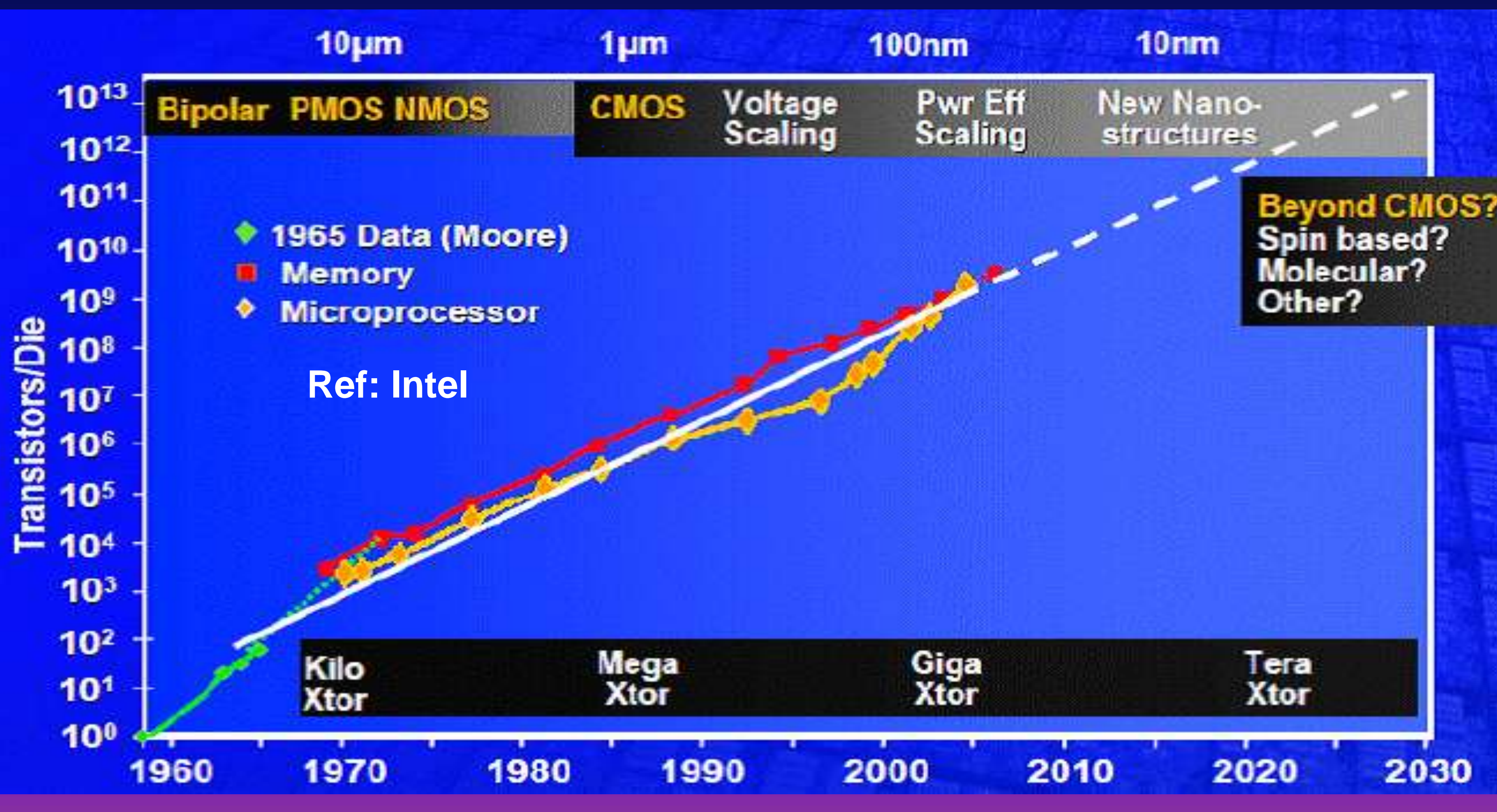
Conclusions:

The continued shrinking of CMOS type conventional devices will soon reach its end (10~15 years), when fundamental limits are approached.



Conclusions:

MOORE's Law is not dead, but the ways in which it continues to rule are changing.



Conclusions:

The most advanced Silicon MOSFETs, as they reach their miniaturization limits, will probably have:

- **Ultra Thin Bodies** (~ 5nm) without dopants
- **Si/SiGe** (“Strain Engineering”)
- **Multiple Gates** (3 Dimensional)
- **Very Short Channel Lengths ~ 10nm**
- **High“*k*” Multilayer Gate Oxides**
- **Metal Gates** (W, Mo, Ru,Ti, Ta, etc)
- **Low** effective “*k*” **insulator** (airgap, porous, etc)
- **Novel Interconnects** (graphene, CNTs, etc)

Conclusions:

Moore's Law general tendency regarding:

- ✓ Higher device density
- ✓ Higher speed
- ✓ Higher number of functions per chip
- ✓ Lower cost

will continue by means of other advances such as:

- Higher integration (3D devices + heterogeneous integration)
- "System-On-Chip" (SOC)
- "System-In-Pakage" (SIP)
- Parallel Processing, "multicore"
- New interconnets (graphene, CNTs)
- New materials (insulators, semiconductors, conductors)
- New devices (replace CMOS for 2020 ??)
- Avanzed Lithography (immersion, EUV, etc.)

Conclusions:

Continued development of a variety of other types of device concepts, such as:

- Heterogeneous Integration (InSb, InGaAs, etc, over Si)
- Printed devices and circuits (inkjet, stamp, etc)
- Organic, microcrystaline, amorphous, devices
- Flexible Displays
- Integrated Sensors
- MEMs, etc.

…but, please keep in mind:

Kroemer's Lemma of New Technology,

a.k.a.

The futility of predicting applications:

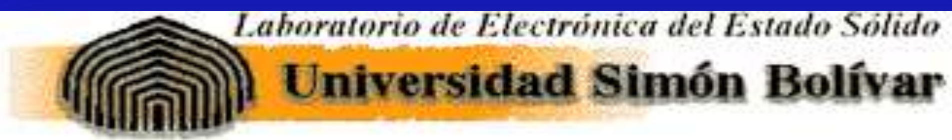
"The principal applications of any sufficiently new and innovative technology always have been – and will continue to be – applications created by that technology."

Ref: Herbert Kroemer (Nobel Laureate in Physics 2000), ECE Department and Materials Department, University of California, Santa Barbara, USA

UNIVERSITY OF CENTRAL FLORIDA

END of lecture

Thank you



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Some useful information sources:

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- "Molecular logic and computing," A. Ptasanna De Silva, S. Uchiyama, *Nature Nanotechnology*, vol. 2, pp. 399-410, July 2007.
- "Growth of nanotubes for electronics," John Robertson, *Materialstoday*, Vol. 10, pp. 36-43, January-February 2007.
- "Monolithic Concept and the Inventions of Integrated Circuits by Kilby and Noyce," Arjun N. Saxena, NSTI-Nanotech, vol. 3, pp. 460-473, 2007.
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- Semiconductor Manufacturing Technology association, http://www.sematech.org
- International Technology Roadmap for Semiconductors, http://www.itrs.net
- Moore's Law at Intel, http://www.intel.com/technology/mooreslaw/index.htm
- Nano Science and Technology Institute's Nanotech 2007 Workshop on Compact Modeling, http://www.nsti.org/Nanotech2007/WCM2007

The growing seed: