Processing and Defect Control in Advanced Ge Technologies

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Outline

- **Introduction/Motivation**
- **Ge Fabrication Techniques**
- **Processing Aspects**
    - ***Wet cleaning***
    - ***Surface passivation***
    - ***Shallow junction formation***
    - ***Germanidation***
- **Conclusions**

Introduction

- **Interest in defects due to their impact on:**
  - **physical processes (e.g. diffusion)**
  - **electrical device performance yield**
- **Interest since the early days of semiconductors, but now there is physical insight**

  No longer trial and error but ENGINEERING
- **Origin of defects can be**
  - **Grown-in (dislocations, vacancies, interstitials, swirls, COPs……)**
  - **Process-induced (dislocations, precipitates, metals, twinning,…)**
- **Scaling is putting stringent requirements on the resolution of the analytical techniques**

Introduction

- **Downscaling**

  Channel doping levels: UTSOI

  High-κ dielectrics

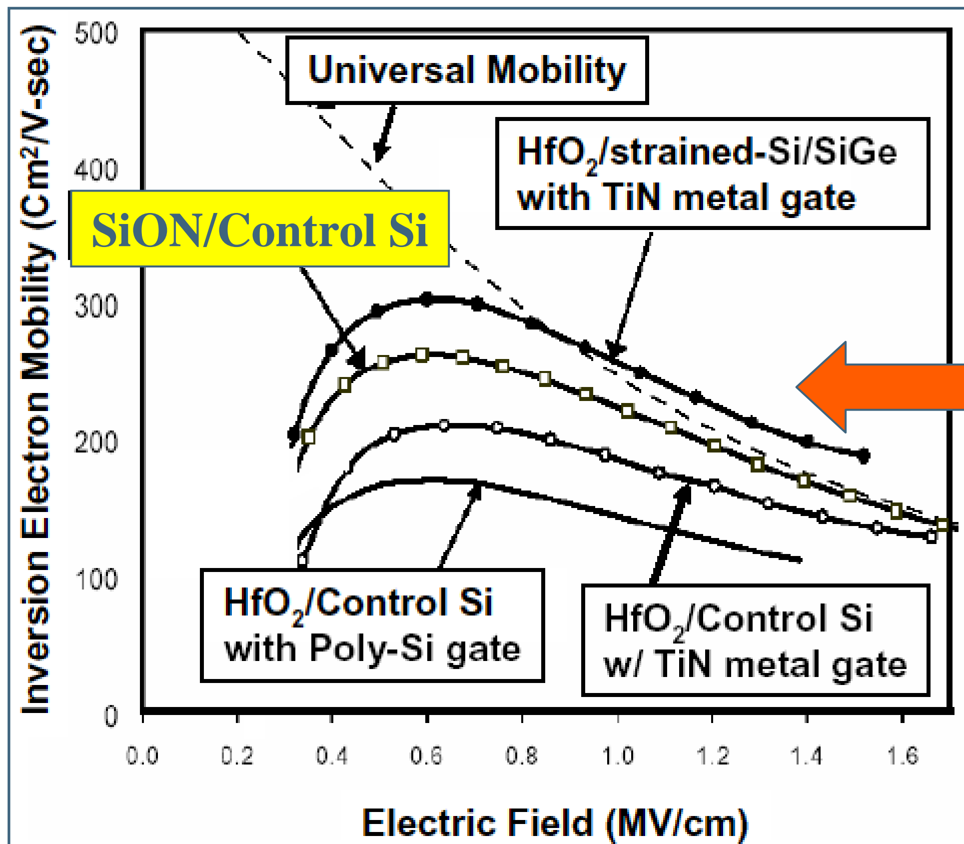
  FUSI/Metal gates

carrier mobility control

Scaling Aspects: Mobility Boosting

- **Use of high-κ dielectrics + metal gate + strained Si**

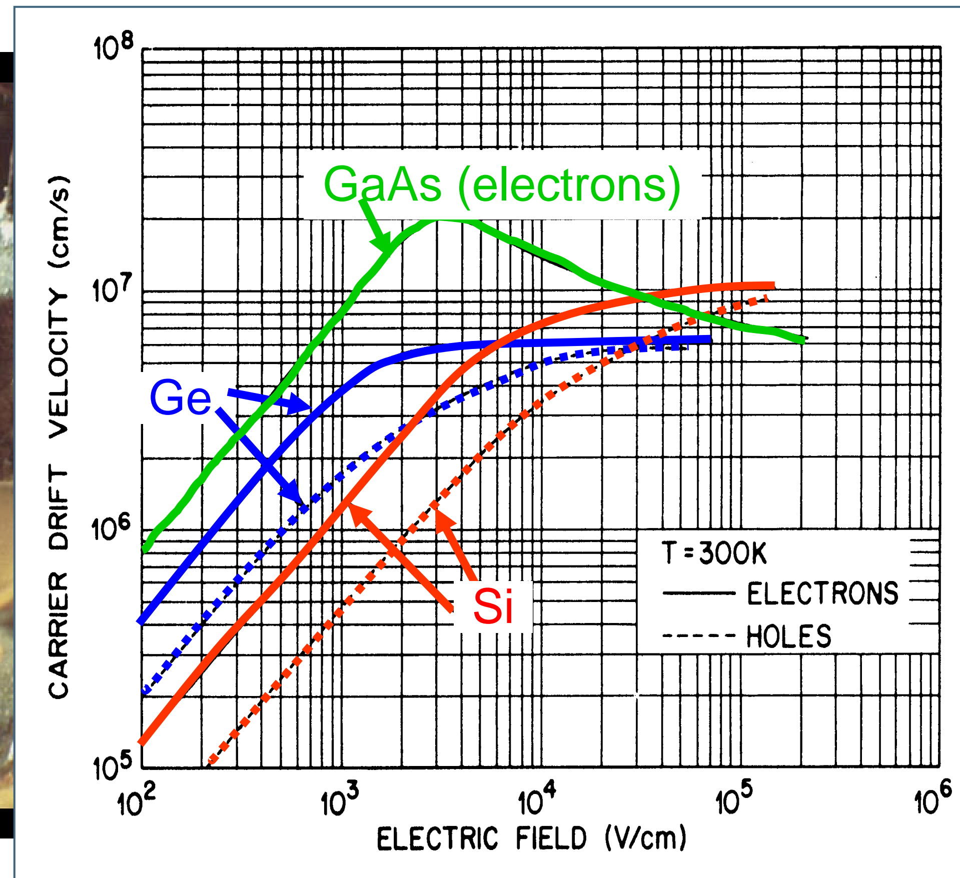
n-MOS



S. Datta et al, IEDM 2003, p. 653

35% increase for strained Si/SiGe

Why are we interested in Ge ?



- Ge has been shown to be a good material to make transistors….
  … and it has a high (low field) electron and hole mobility

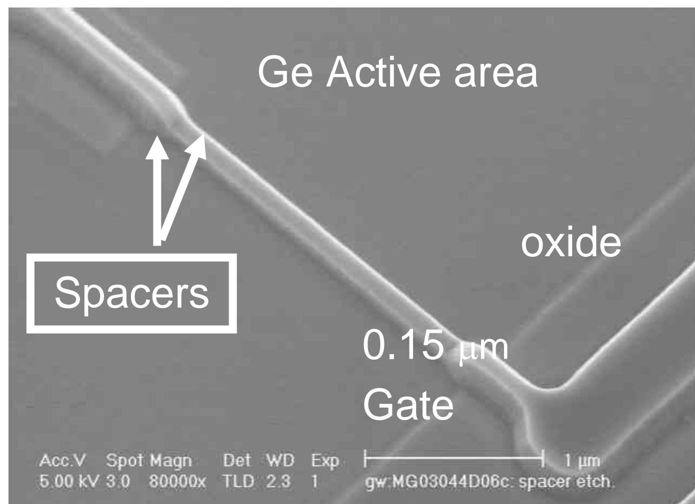
Ge used in first transistor radios

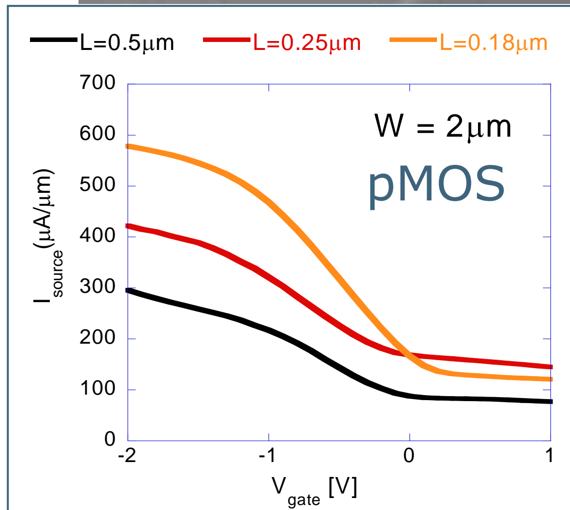
- On October 18, 1954, the U.S. company I.D.E.A. announced Regency TR1.
  - Used 4 germanium transistors.
- Sony's first radio, TR-55, in 1955
  - Used 5 germanium transistors.

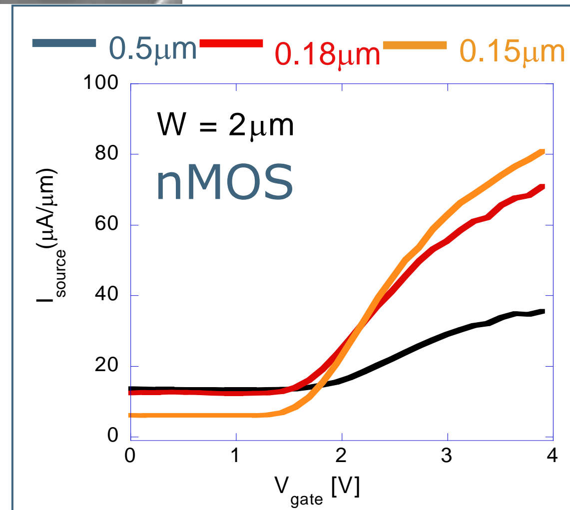
Regency TR1

Sony TR-55

Early results: pMOS and nMOS on 200mm GeOI







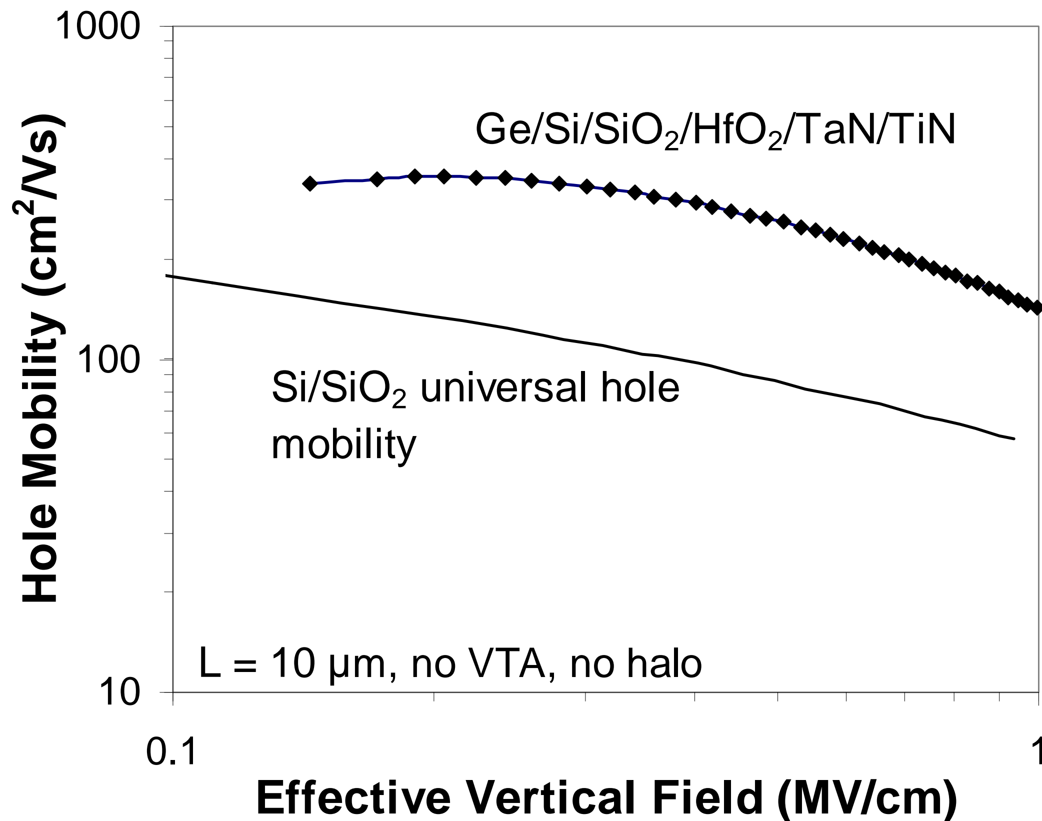
pMOS

- Good drive current>500mA/µm for L=0.18µm

nMOS

- Low drive current
- Ge/high-k interface quality is one of the main limiting factors

Experimental Results - Mobility



Best peak mobility achieved so far ~358 cm^2/Vs

Mobility as a function of vertical field for L = 10 µm Ge pMOSFETs following 350°C 20 min H_2 PMA

Yoshiki Kamata *Toshiba Corporation (2008)*

Materials Today, Jan/Feb 2008, vol. 11, no.1-2

Ge brought the microelectronics industry two Nobel prizes. The first transistor was based on Ge, as was the first integrated circuit. So why did we give it up?

Though semiconductor makers quickly switched to Si as the prime semiconducting material, Ge is now on the microelectronics research agenda again, and is being discussed as a possible replacement for Si.

It's back to the future.

Motivation/Objective

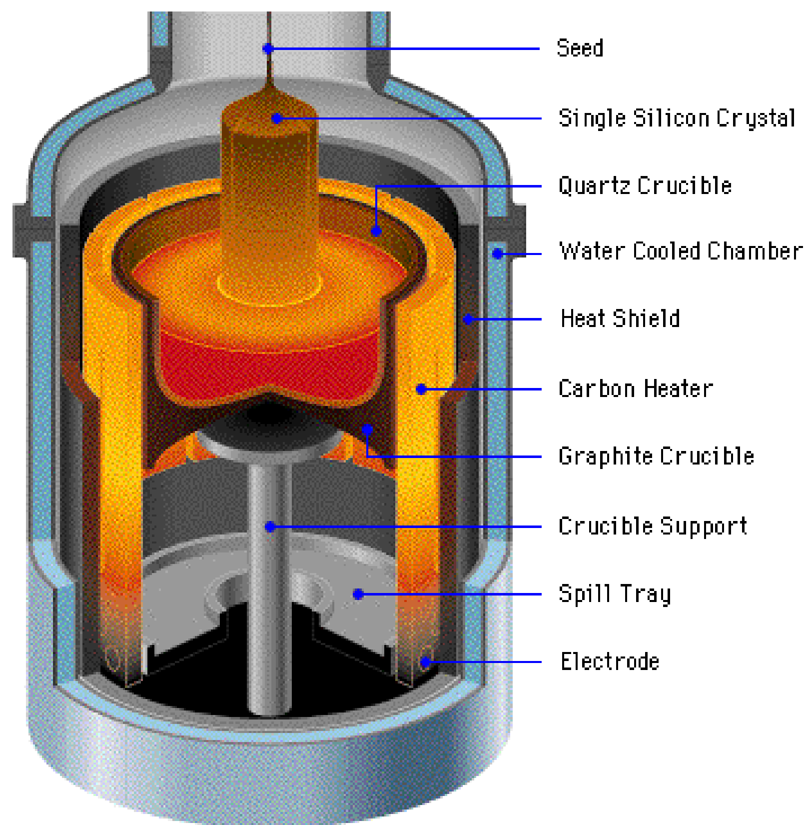
- **Diffusion limited leakage current for Si diodes: 1 nA/cm^2**
- **Ge diodes: 10^{-4} – 10^{-7} A/cm^2 theoretical limit at 298 K**

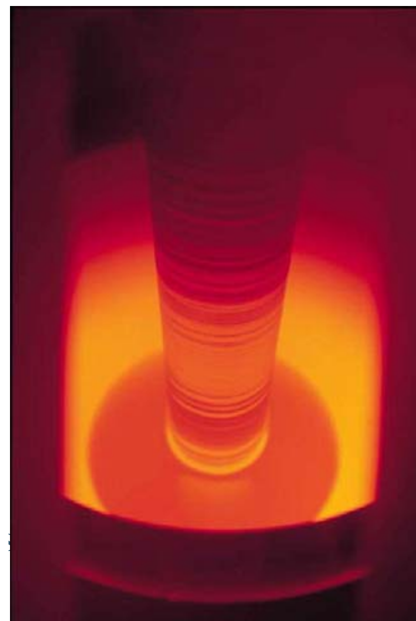
  n_i 10^3 times higher: 10^3 (generation) or 10^6 (diffusion) higher current
- **Leakage current depends on the presence of defects**
- **Impact defects on other parameters: lifetime, low frequency noise, reliability, …**

Systematic study of the origin of grown-in and processing-induced defects in Ge

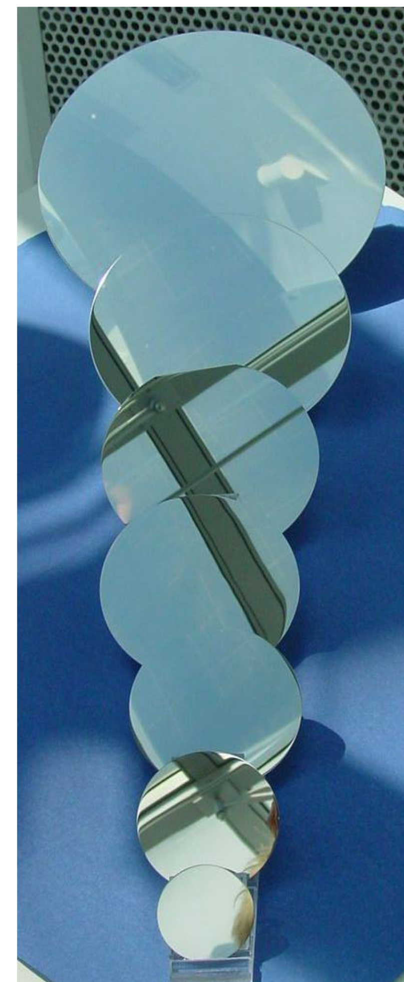
Defect Engineering

Czochralski Crystal Growth





Ge crystal



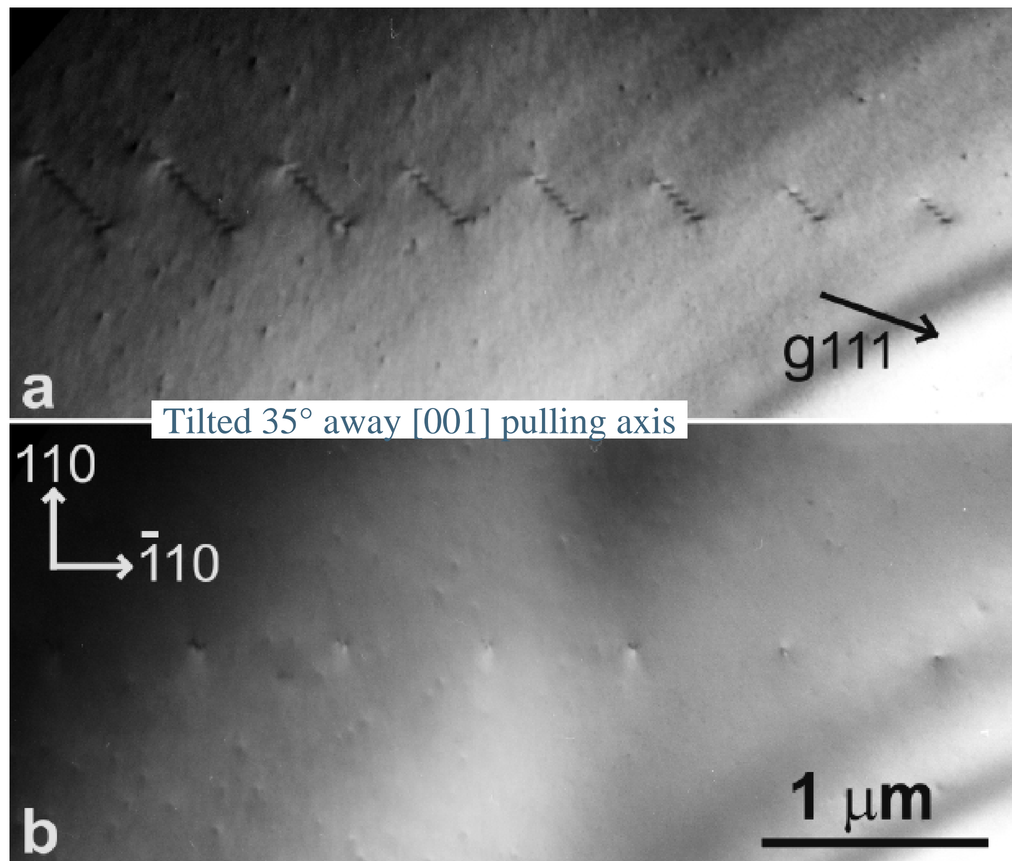
2 inch to 300 mm

Higher Ge material cost ($600/kg) vs Si ($54/kg)

Defects in Ge

Vanhellemont et al., in Defects and Diffusion in Semiconductors – An Annual Retrospective VII, Trans. Tech. Publ. Inc., 230, 149 (2004)

☞ *Defect in as-grown Ge (row of dislocations)*



- * **High-res. Ge, H-atm. crystal growth**
- * **30°, 60° and 90° disl.**
- * **Disl. sink for [V]**

No V_2-H complexes

Crystal Growth Aspects

⇒ 30°, 60° and 90° dislocations: sinks for [V]

Reduction of V_2-H complexes and COPs

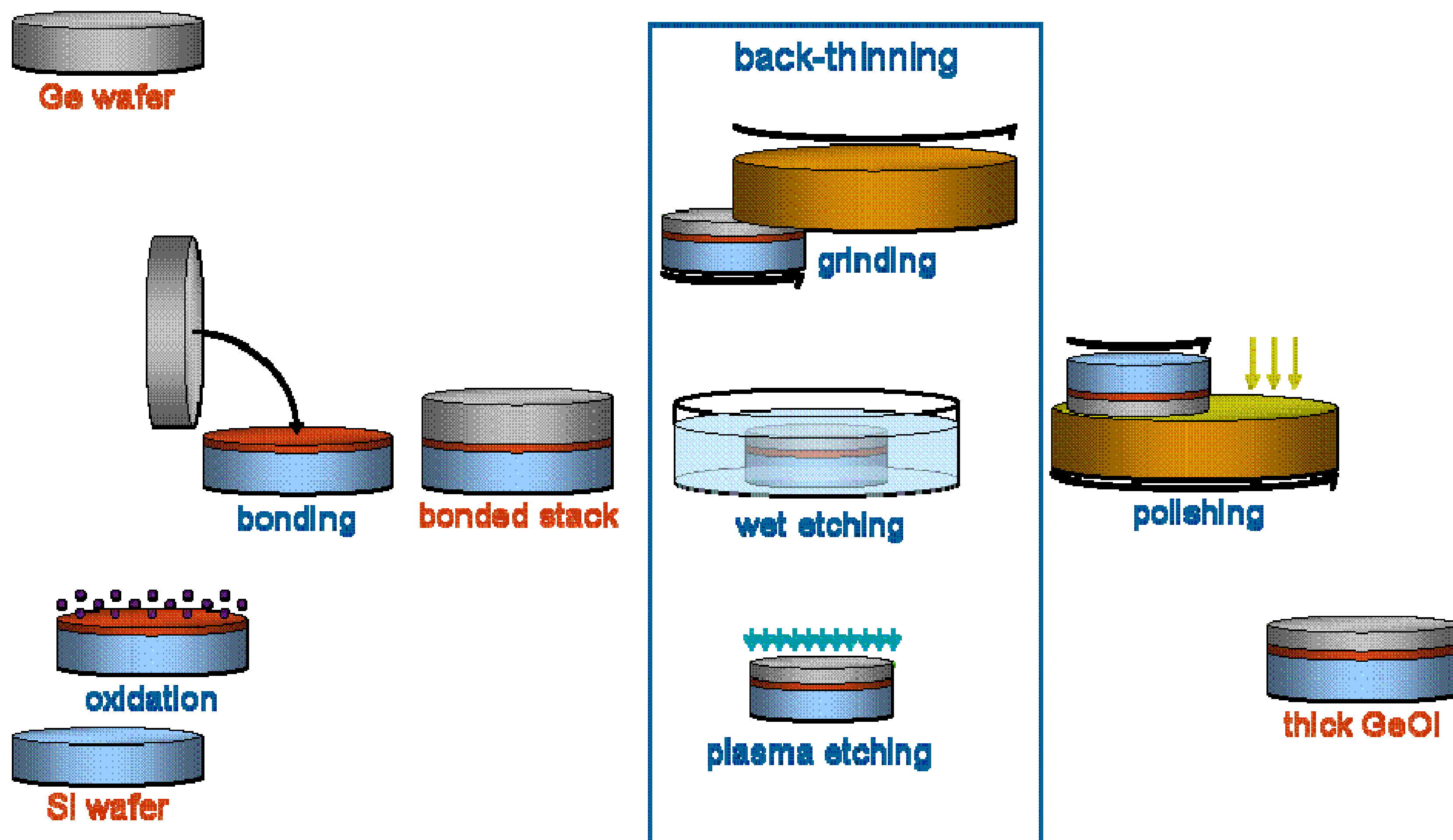
⇒ Dopant and self-diffusion controlled by [I]

⇒ Reduced O_i content (IR: Ge-856 cm^{-1} Si- 1107 cm^{-1})
Oxygen precipitation?

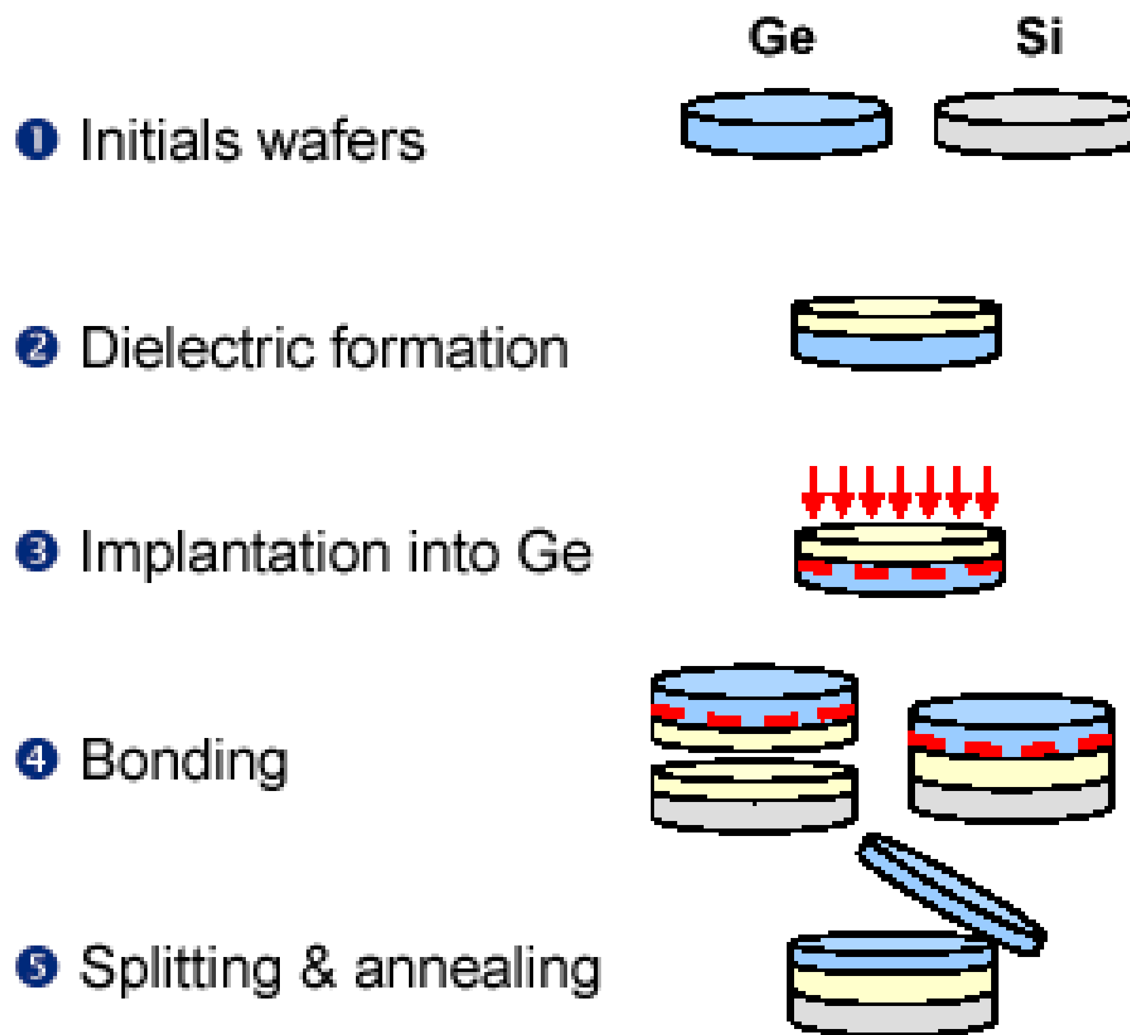
⇒ High quality Ge substrates for μE applications

GeOI, epitaxial Ge on Si, Ge condensation, …

Thick GeOI Process



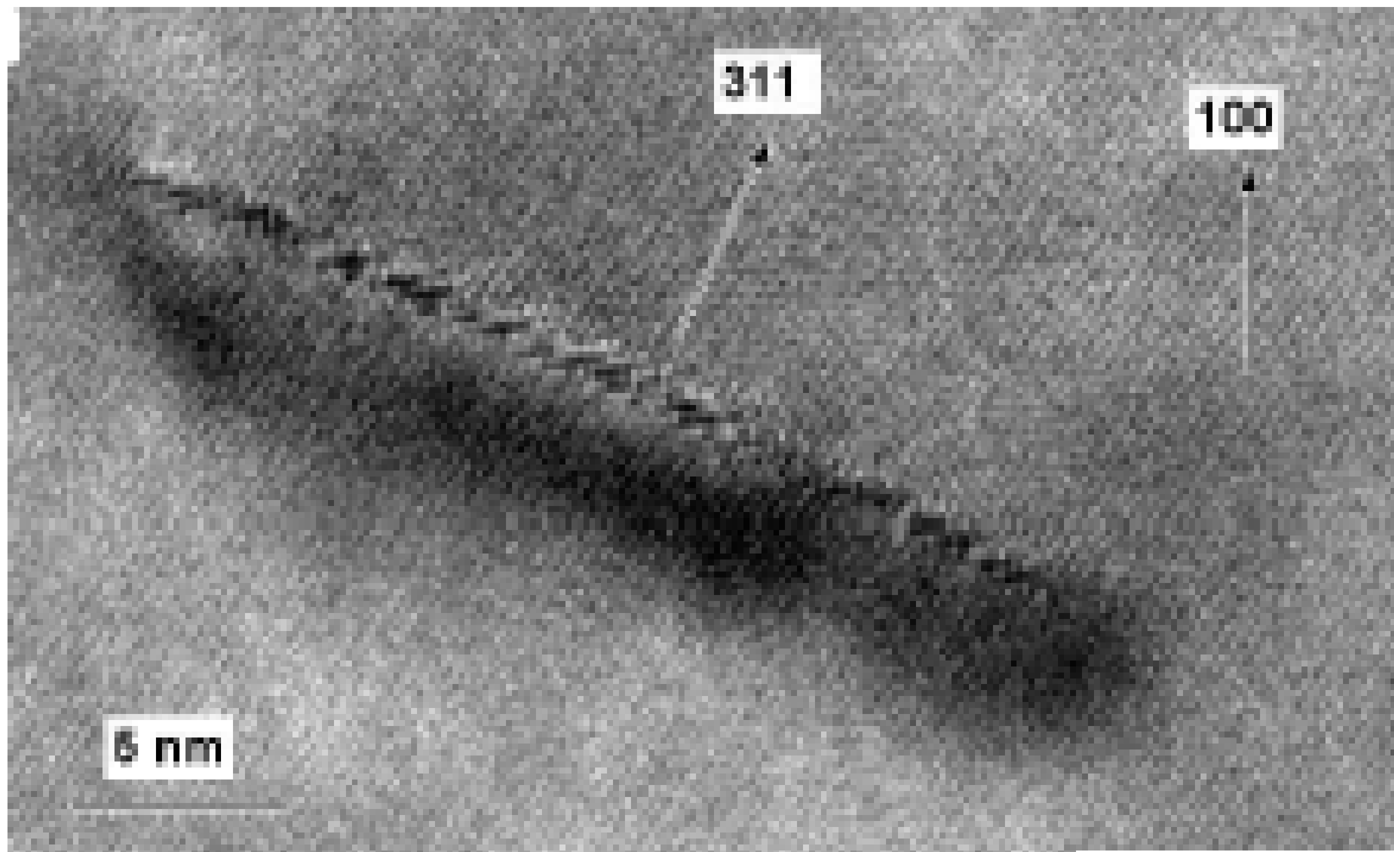
Smart Cut Process for Ge



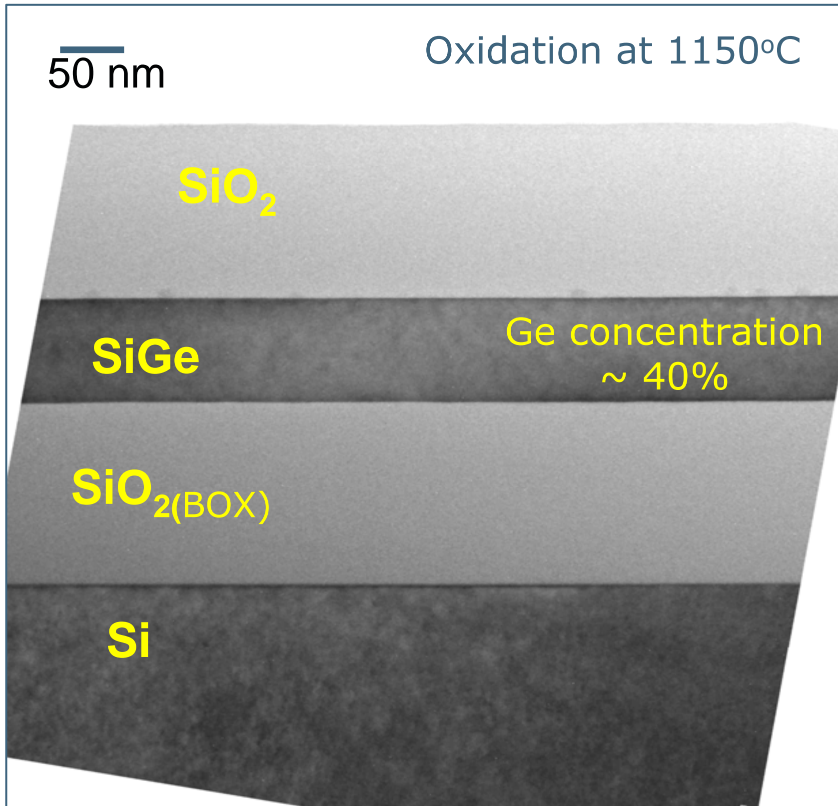
Defects in GeOI

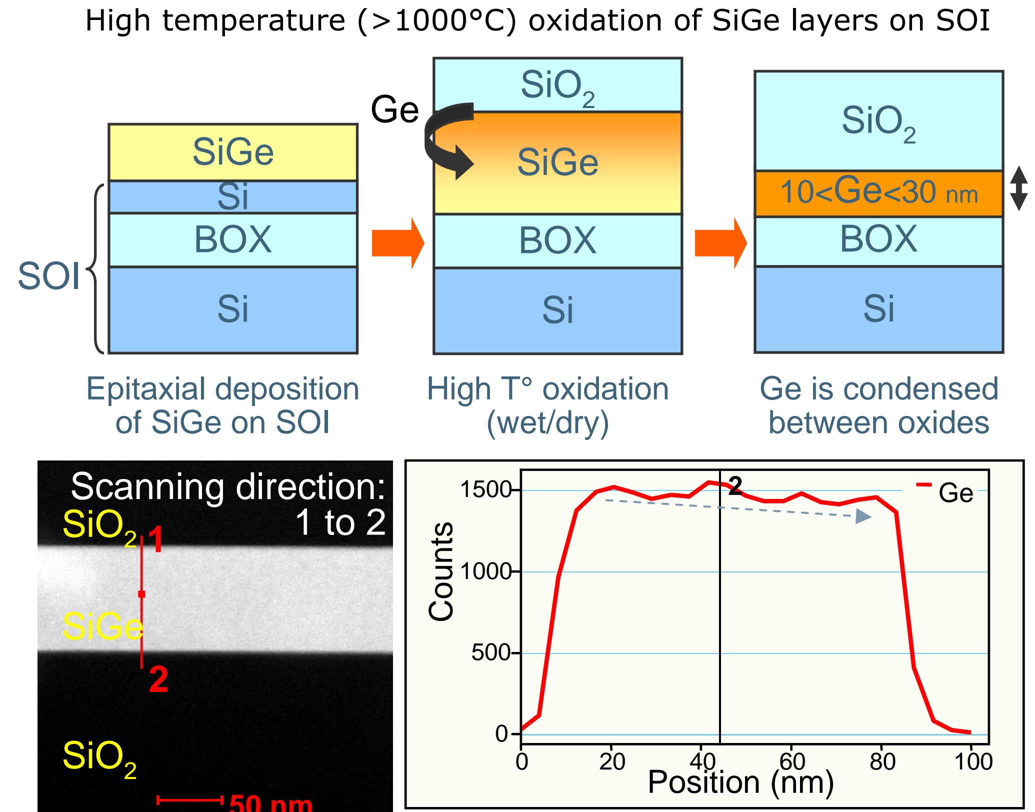
K.K. Bourdelle, APL, 86 (2005) 181910

{311} defect



(Si)GeOI formation by Ge condensation

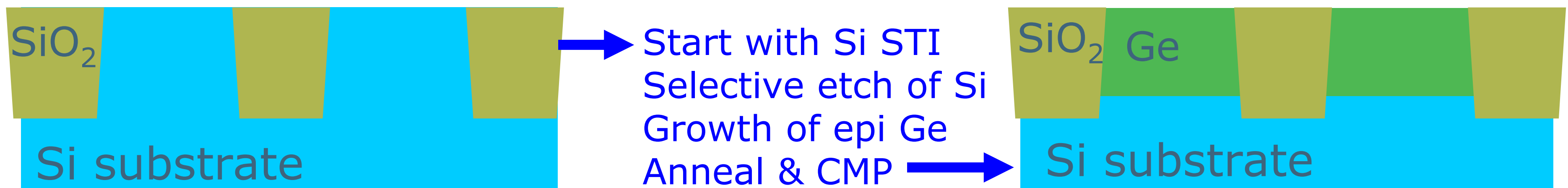




- Estimated defect density: < 1. 10^6 cm^{-2}
  - Needs further improvement
- Uniform Ge profile in SiGe
  - Could allow to make ultra-thin (Si)GeOI substrates for fully depleted devices

Substrates – Epi Ge in Si STI

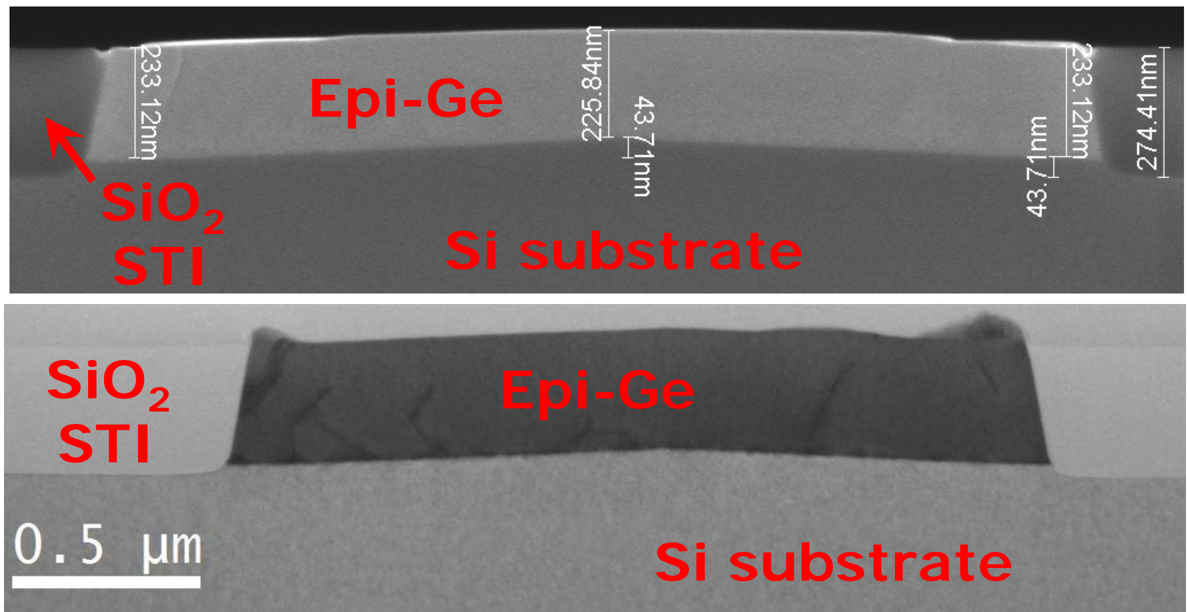
- Epi-Ge in Si STI
  - Utilizes Si STI module for device isolation.
  - Enables monolithic integration of Ge and Si devices



Proof of Concept

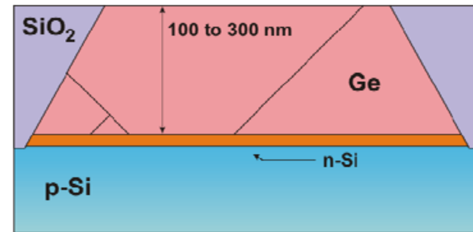
- 250 nm epi Ge
- 4×10^8 TD / cm^2

Note: TEM is without CMP.

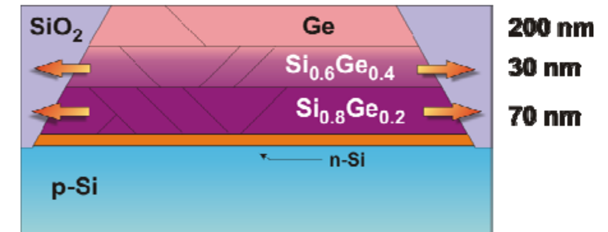


Selective growth of Ge on Si

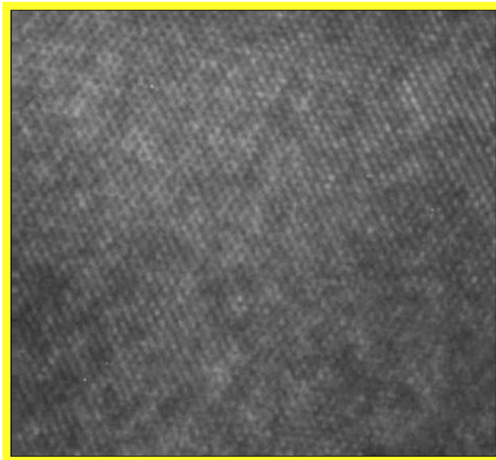
Selective growth of Ge after formation of STI could reduce the active area leakage

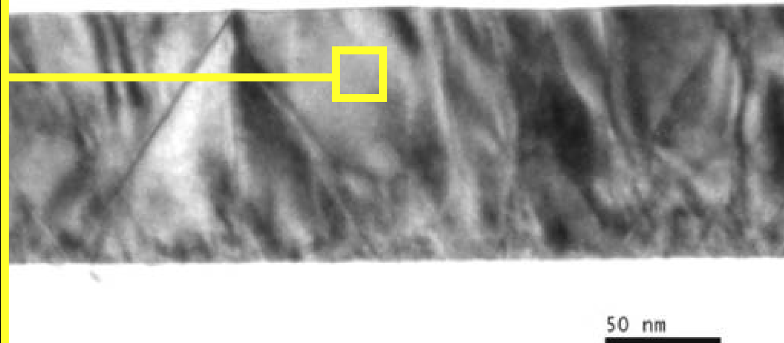


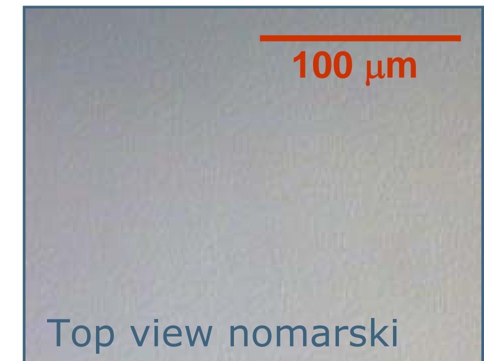
Pure Ge on Si



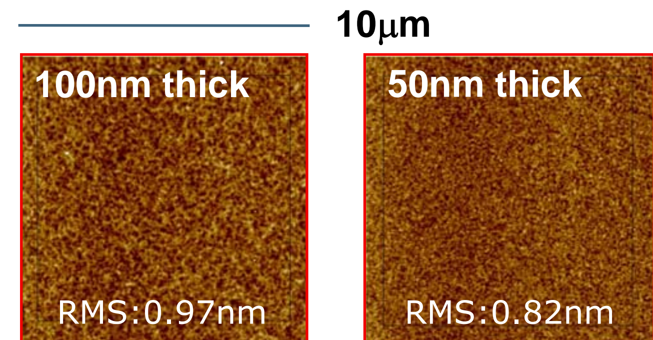
SiGe buffer layers







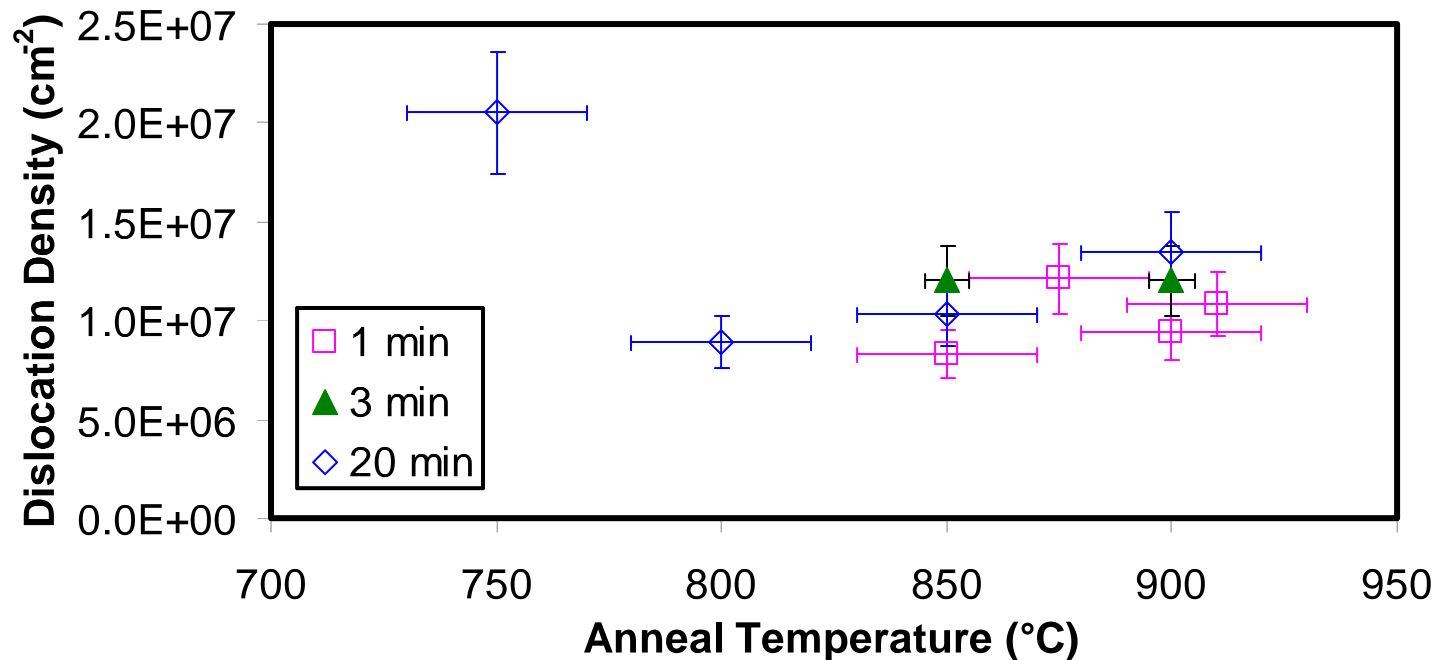
- Reduction in dislocations density needed
- Nomarski indicates uniform deposition and smooth surface
- AFM shows low RMS roughness for 50 and 100nm films



Substrates – Epi Ge on Si

- 200 mm of epi-Ge on Si used for most IMEC lots.
  - 2 µm thick, relaxed epi-Ge wafer from ASM
  - As-grown: ~1×10⁸ threading dislocations/cm²

  - Dislocation density reduced by ~10x with >800°C anneal.



Crystal Growth Aspects

⇒ Same bulk minority lifetime as in Si

Less Auger recombination for high doping

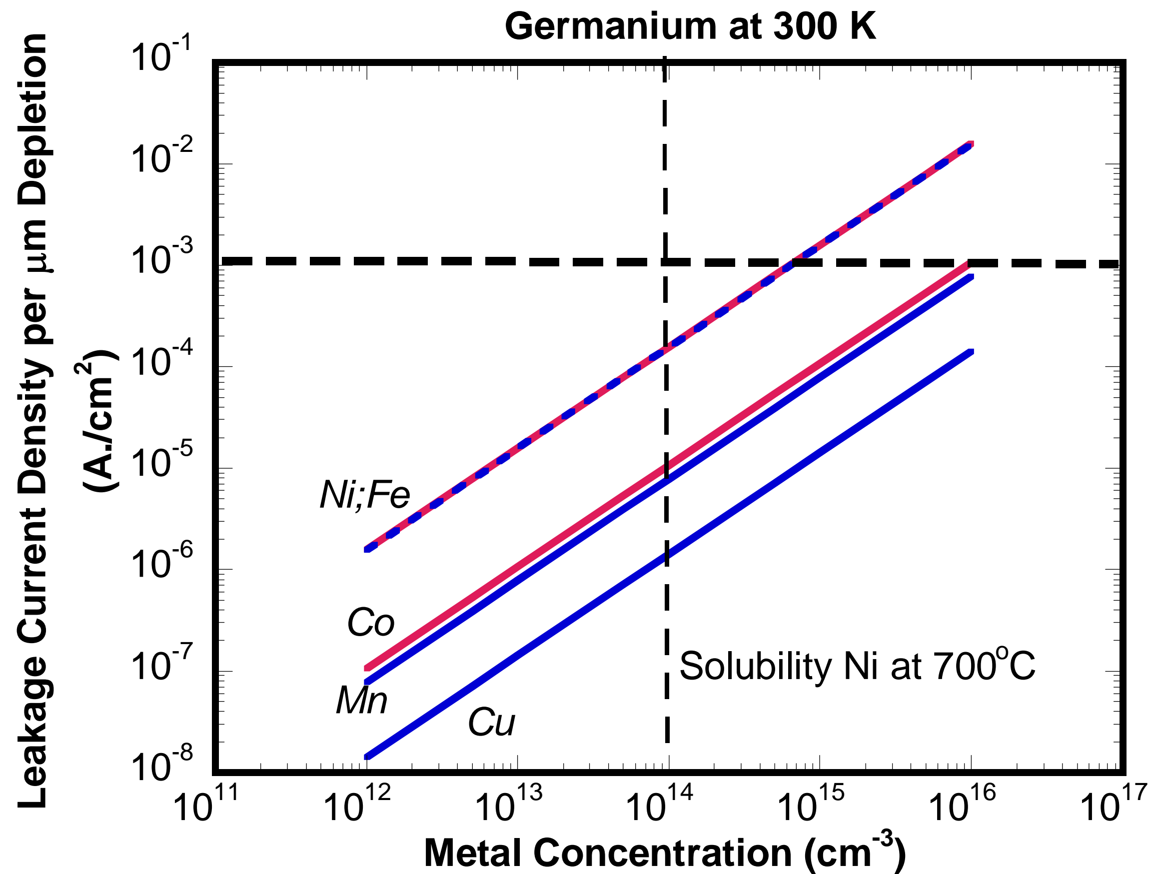
⇒ More prone to metallic contamination

Fe, Ni, Co dominant, less impact Cu
n-type lower lifetime than p-type

Mid gap acceptors increase the leakage current

⇒ Gettering is difficult in Ge

Metals in Ge



Leakage current per μm depletion width at 300 K for different transition metals in function of their concentration

Ge Processing Issues

- **Is Ge manufacturable in a Si processing line ?**
  - Same toolset can be used, but processes have to be modified
- **Ge surface and Ge/high-k interface quality**
  - Passivation of interface states
  - EOT scaling
  - Cleaning is critical (severe etching during wet processing)
- **Dopant activation and re-crystalization**
  - Especially n-type activation
  - Leakage current of junctions
- **Quality and availability of substrates**
  - Defect density of Ge layer ?
- **Main question: Ion(Ge transistor) > Ion(sSi transistor)?**
  - Ion/Ioff ratio

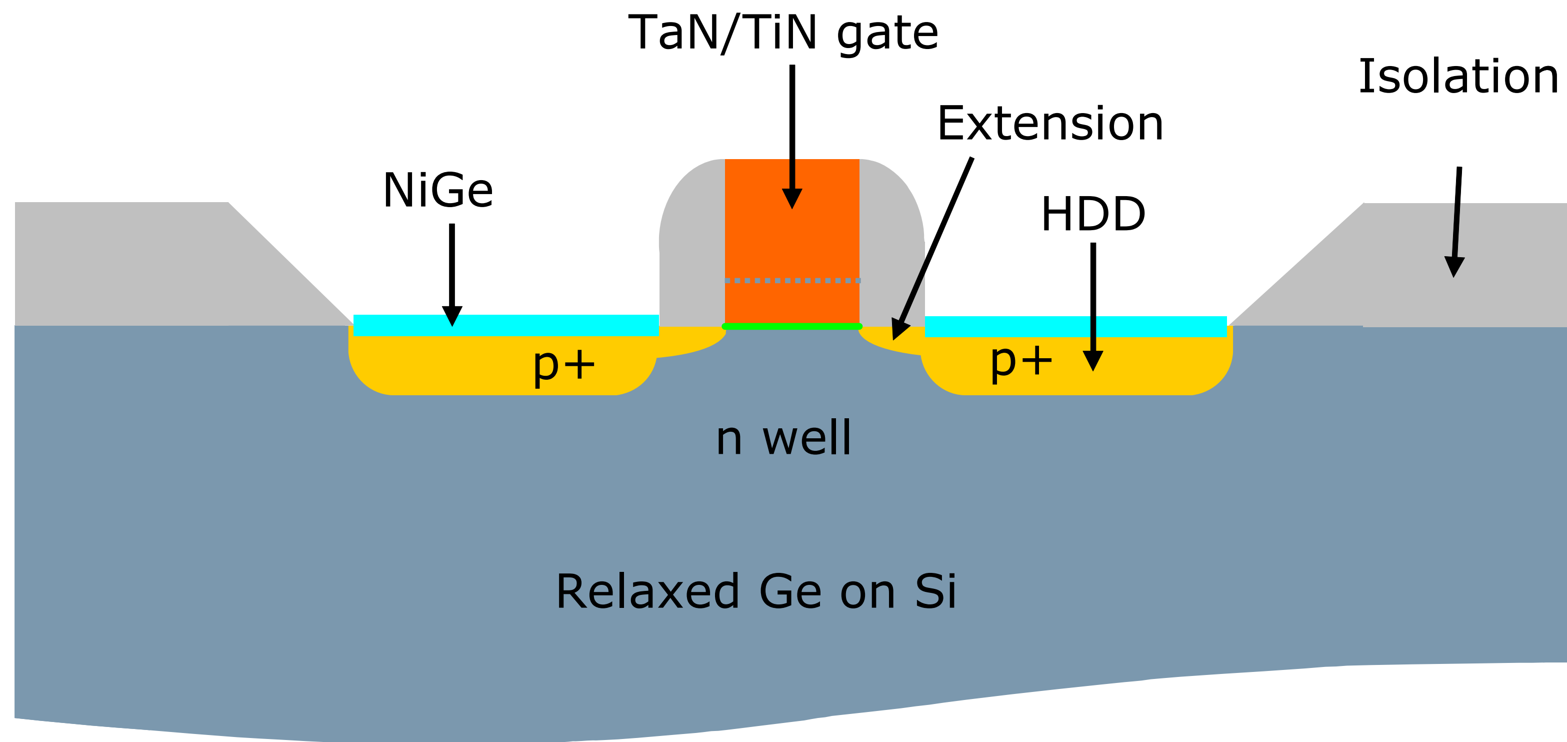
Etching of Ge during wet processing

Etch rate calculated from weight loss, all treatments at Room Temperature

Etch solution	etch rate (nm/min)
H_2O (dissolved oxygen)	0.005-0.006
10% HF	<0.001
BOE	<0.001
1M HCl	0.01
0.5%HF/1M HCl	0.006
1M NH_4OH	0.03
SC1(0.001/0.01/5)	17-27
SC1(1/1/7)	200-280

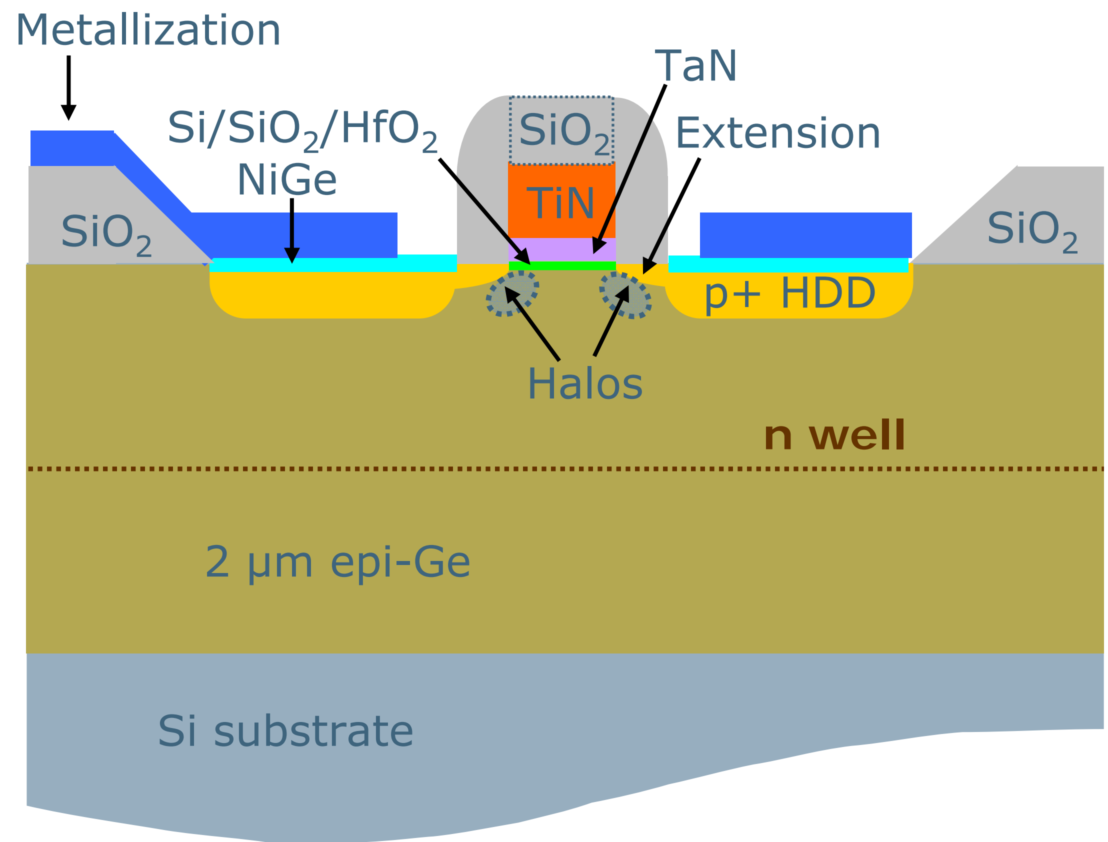
- **HF does not etch Ge**
- **all other solutions (incl. DI-water): measurable etch rate**

Transistor Structure

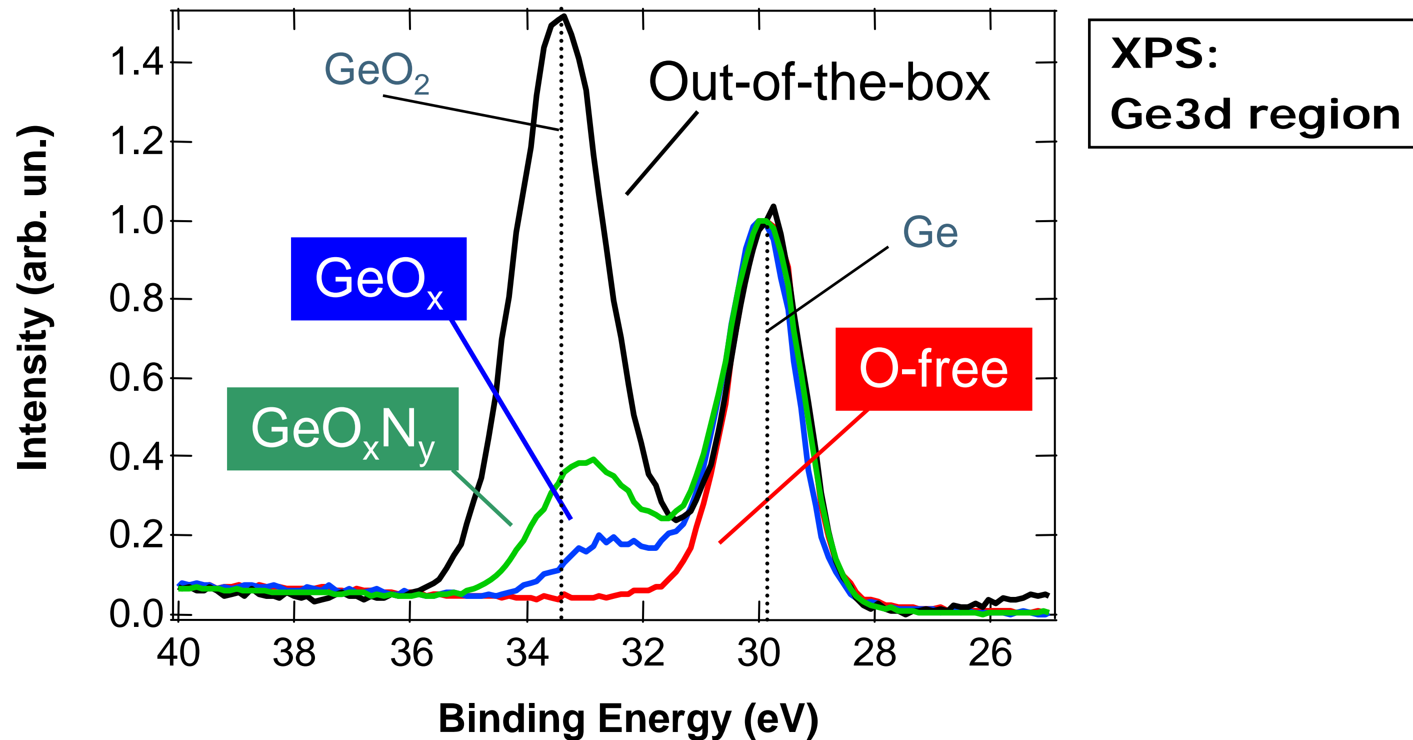


Typical 200 mm Ge pMOS Process Flow

Start:	2 µm epi Ge on Si
Wells:	P 90, 180, & 570 keV
Isolation:	~200 nm SiO2, 45°
Passivation:	~6 ML epi-Si / SiO_2
Dielectric:	4 nm HfO_2
Gate:	10 nm TaN / 100 nm TiN
Halo:	P 25°
Extension:	BF_2
Spacer:	90 nm width
HDD:	Ge PAI, B HDD
Anneal:	500°C 5 min
NiGe:	10 nm Ni, RTA, Etch, RTA
Metallization:	TiN / Ti / Al / TiN
Sinter:	350°C 20 min H_2



Ge surface preparation



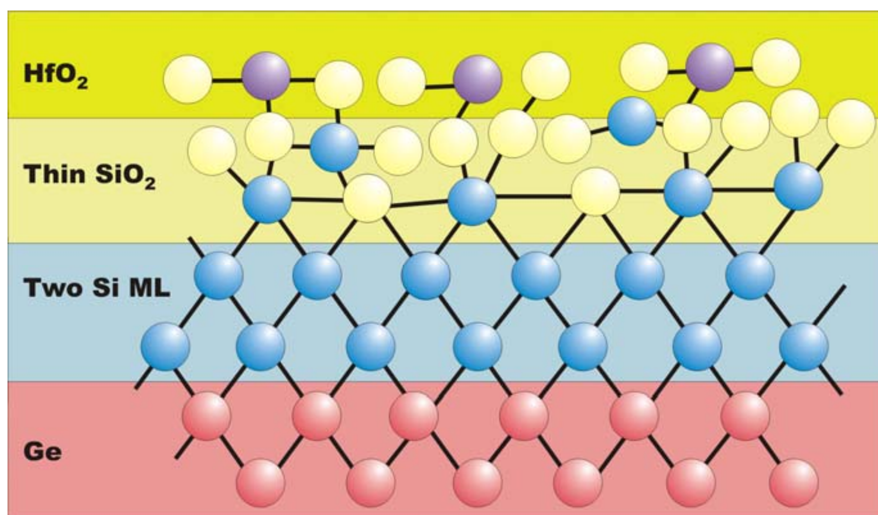
- Out of the box → 1.68 nm GeO_x
- HF-dip → 0.3 nm GeO_x
- HF-dip + NH_3 anneal → 0.6 nm GeO_xN_y
- HBr-dip → O-free

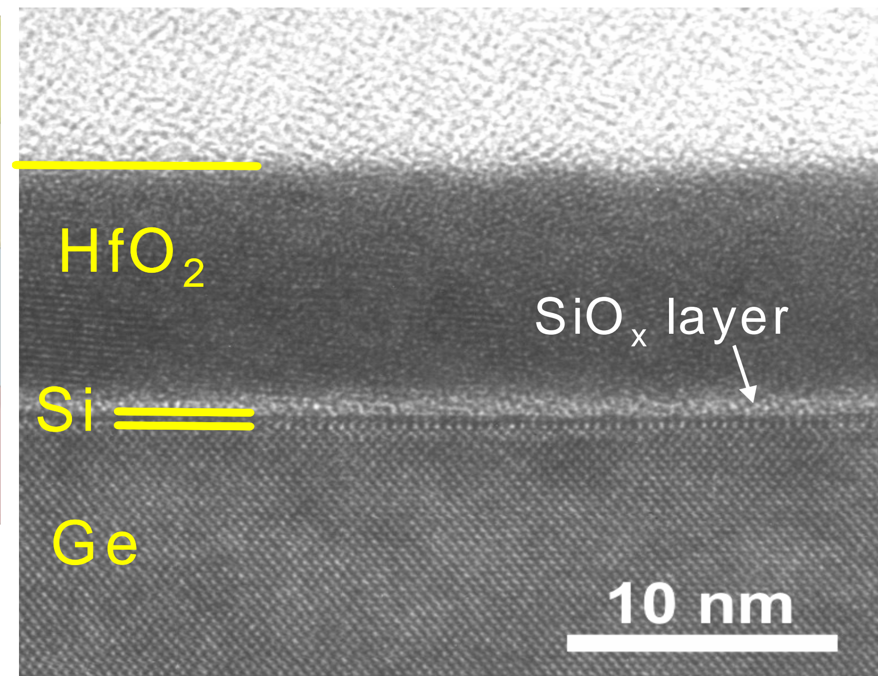
Surface Passivation

CeO_2 good passivation : N_{it} $1x10^{12}$ (p) $6x10^{11}$(n) $eV^{-1}cm^{-2}$

S under investigation

Good results with Si

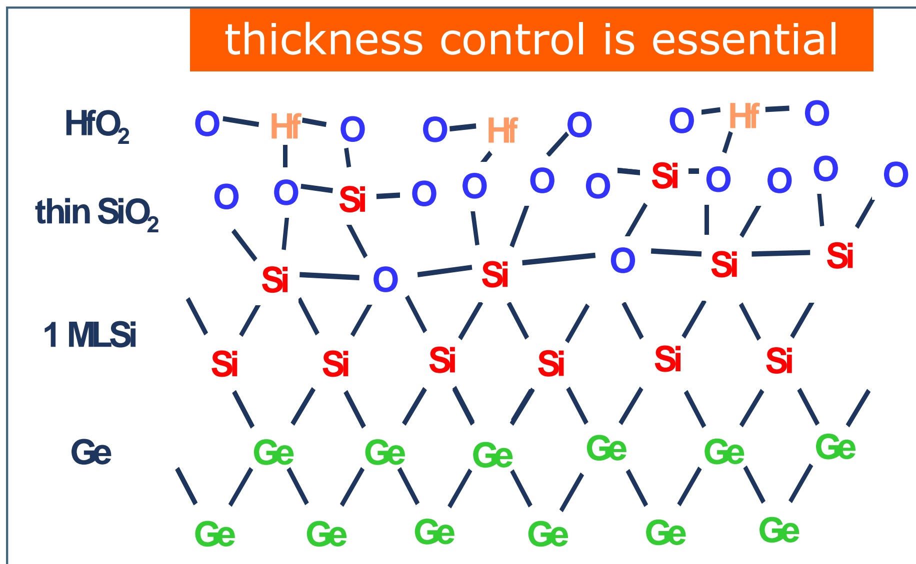


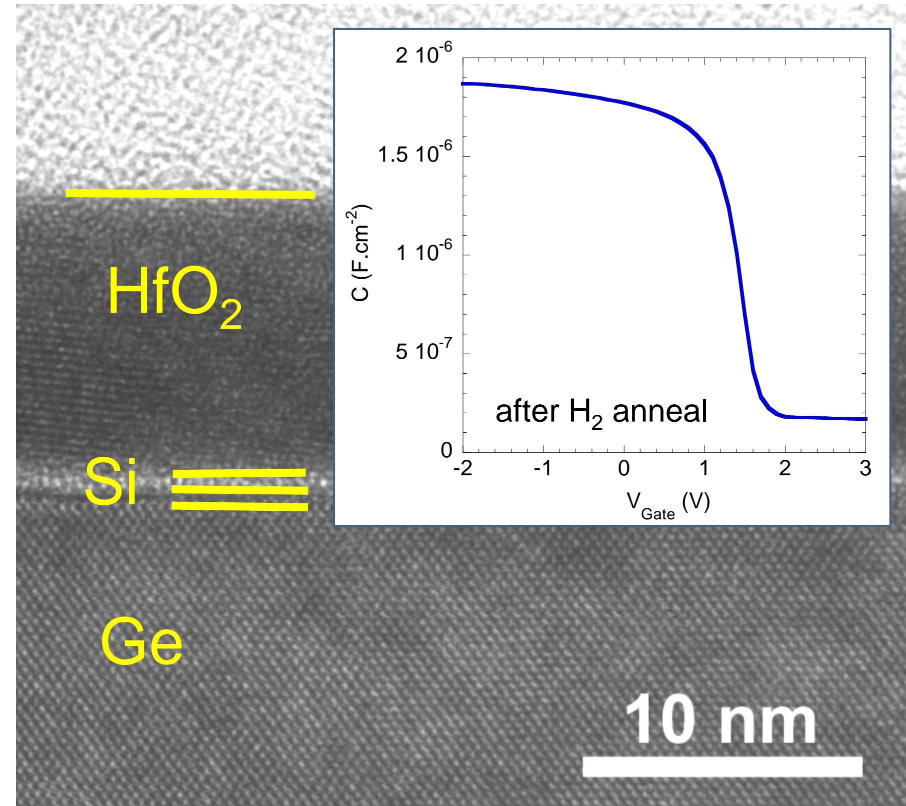


Si passivation of Ge surface

- **Si layer too thick**
  - stress-induced interface defects
  - C-V curve shows high D_{it}
- **Si layer too thin**
  - Ge will oxidize and defective layer with poor interface is formed

CV curve shows a passivated surface and a reduced N_{it}





- **CV curve on Si passivated Ge surface has low N_{it}**
  - H_2 post treatment further improves C-V curves
    - effect is similar to the passivation of silicon with H_2

Shallow Junction Formation

Ge: lower anneal temperatures for activation (400-600°C)

Higher I/I damage in Ge, but anneal at lower temperatures

Sheet resistivity: max solubility, dopant out-diffusion activation degree

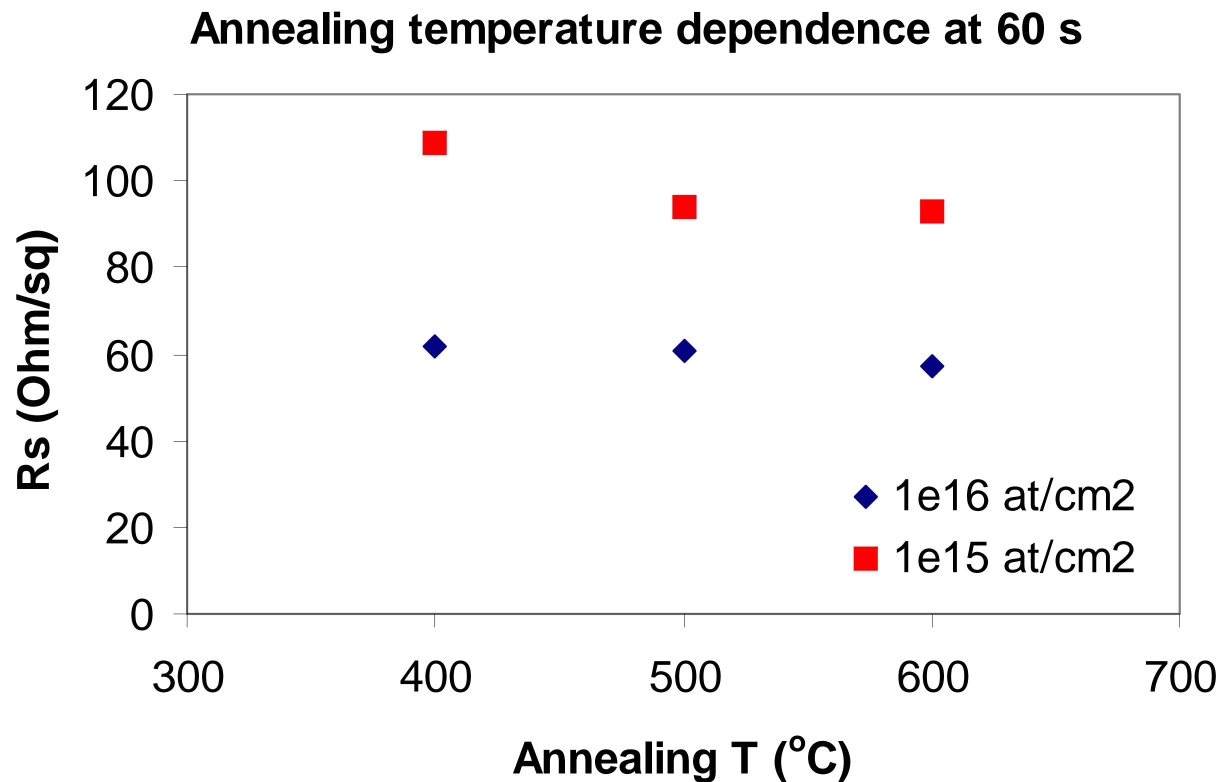
Thermal budget: balance between dopant activation, defect annealing and junction depth

Boron shallow junction can be obtained by Ge pre-amorphization and RTA

More difficult to control n-type dopants like P, As an Sb

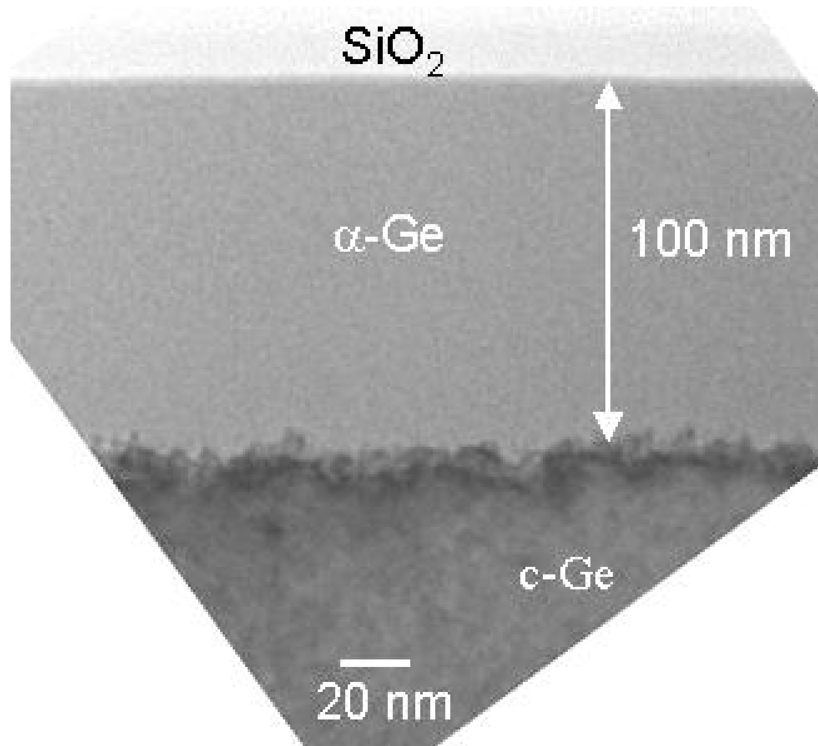
Co-implantation with non-doping impurities like N and C gives promising results for P – less dose loss and lower P in-diffusion

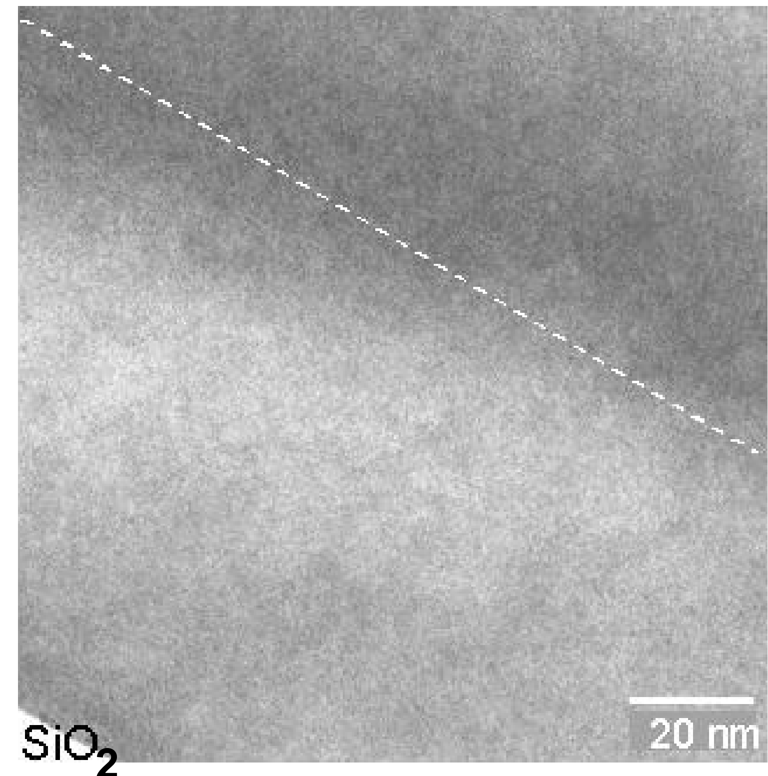
Boron Doping – Sheet Resistivity



Sheet resistance versus RTA temperature (60 s), corresponding with a 4.5 keV B 10^{15} or 10^{16} at/cm^2. A Ge pre-amorphization implantation was done at 120 keV & 10^{15} at/cm^2. A junction depth at a carrier concentration of 10^{18} cm^{-3} of ~70 nm

Re-crystallization of pre-amorphized, B-doped Ge





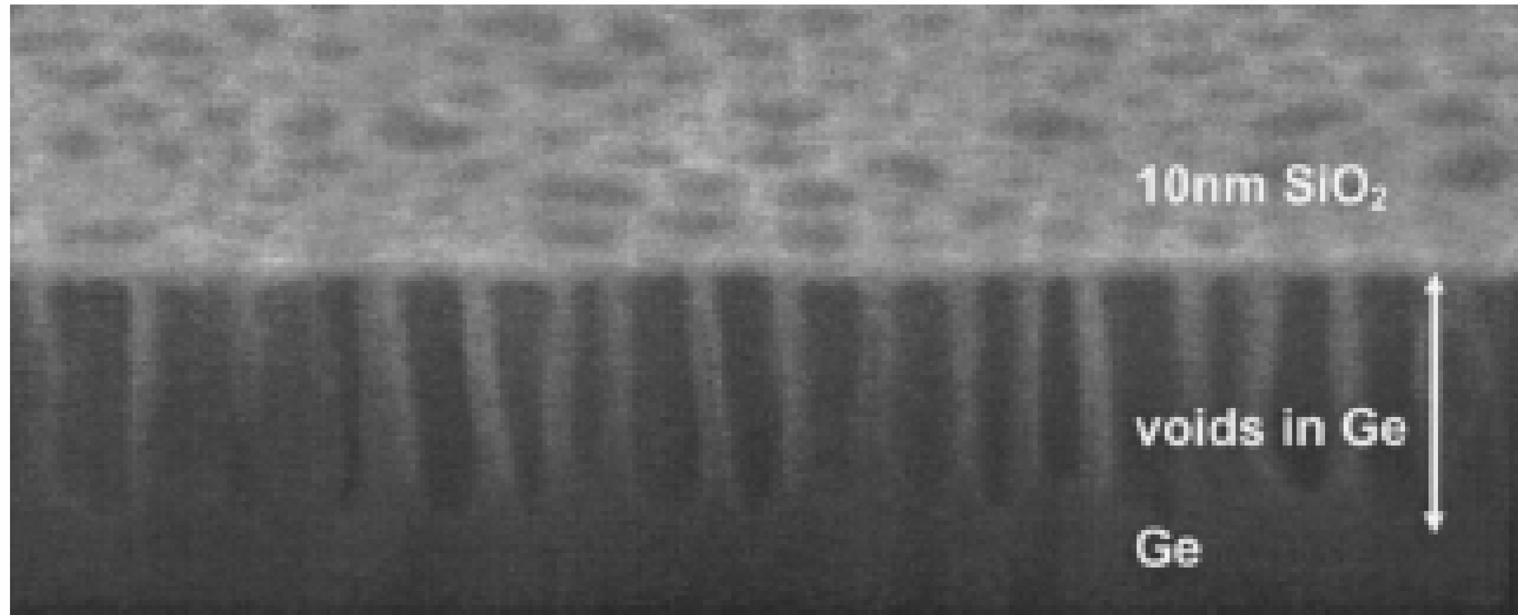
As-implanted

Depth of amorphous layer: 100 nm

Annealed at 400C, 60s, N_2

- Fully re-grown
- No visible residual defects at the EOR

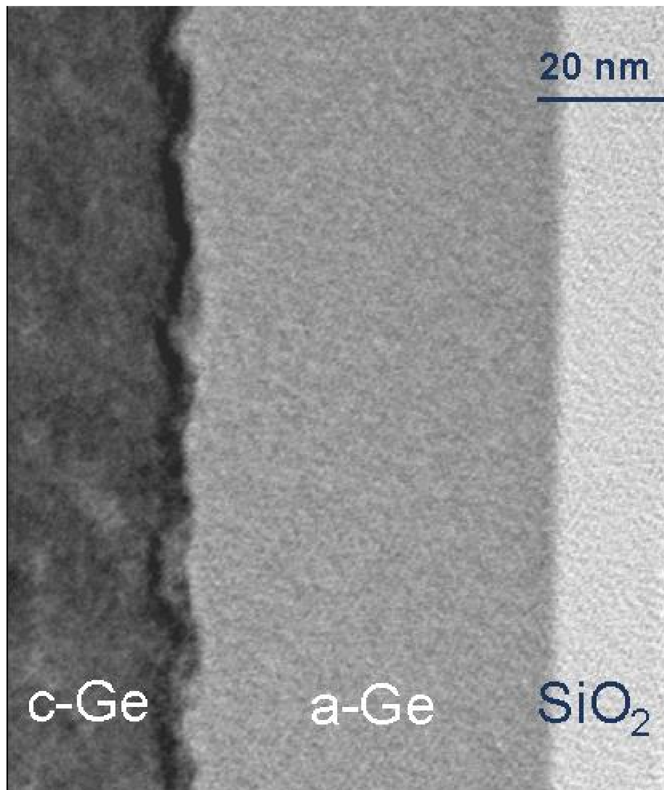
Sb Doping – Void Formation



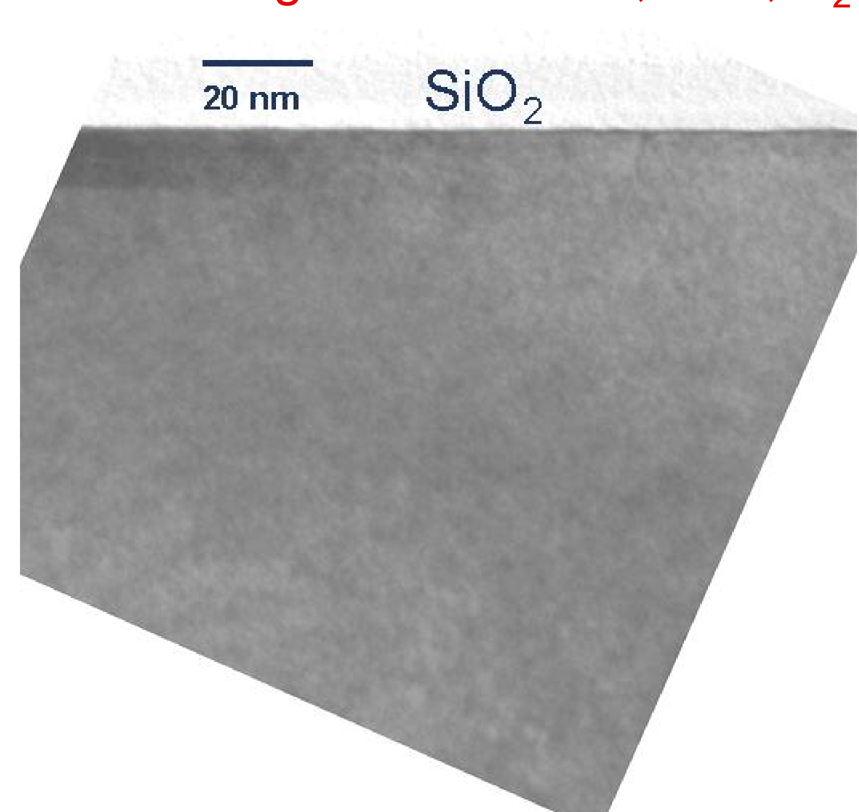
SEM image (x150 000) of a 10 nm SiO_2/Ge sample implanted with 10^{15} at/cm^2 Sb at 70 keV, showing voids extending up to 100 nm below the surface

P (as-)implanted and re-grown Ge: microstructure

as-implanted P 25 keV 3e15 at/cm^2



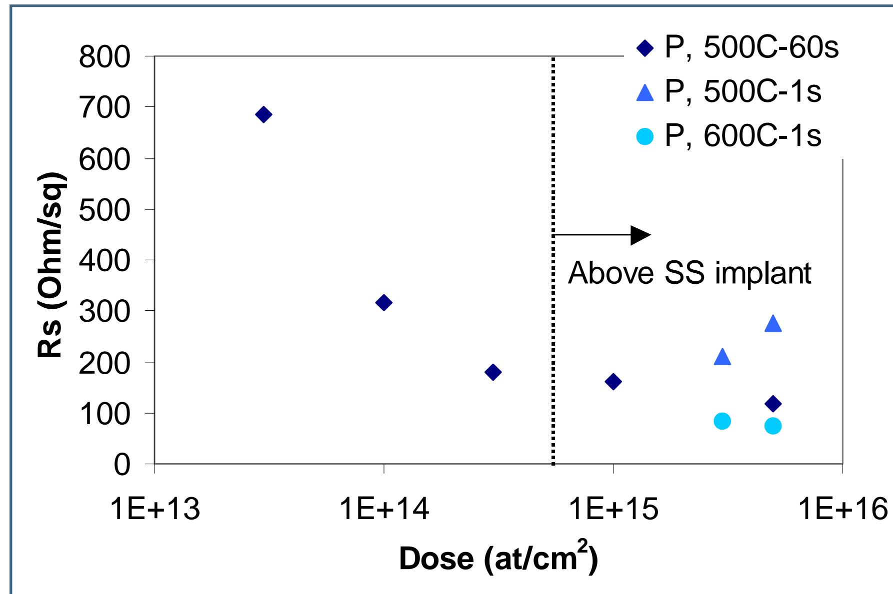
After re-growth at 400C, 60 s, N_2

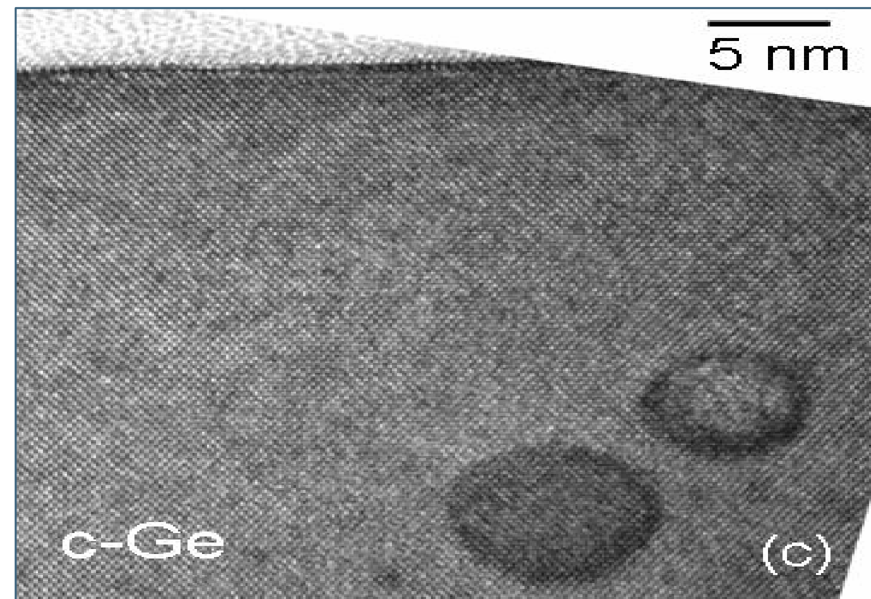


- P-doped Ge fully re-grows at 400C (60 s)
- No evidence of P clusters or residual damage after re-growth at low T
- Inactive P may be in small P-V clusters or interstitials

Control P doping in Ge - Precipitation

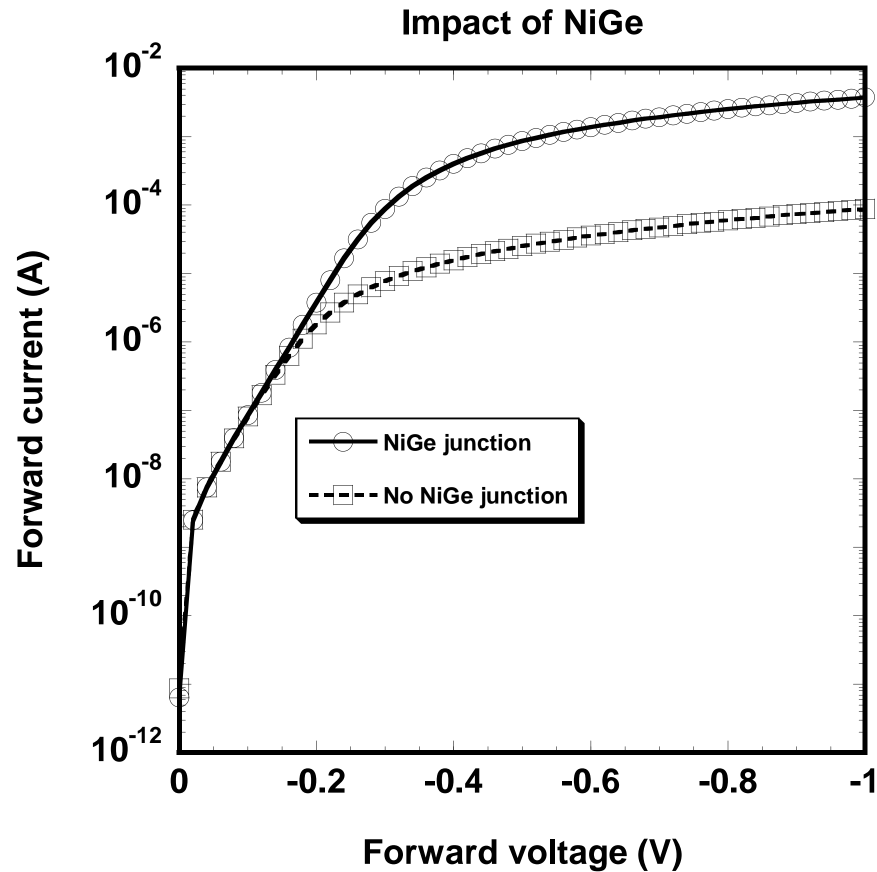
15 keV P in Ge; no SiO_2 cap



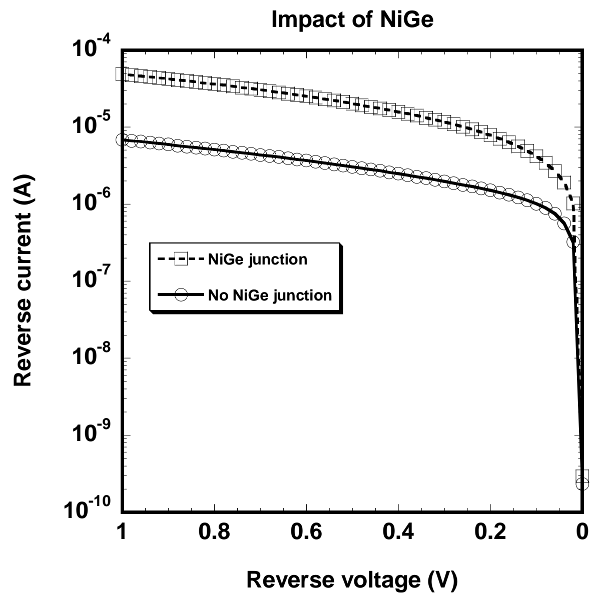


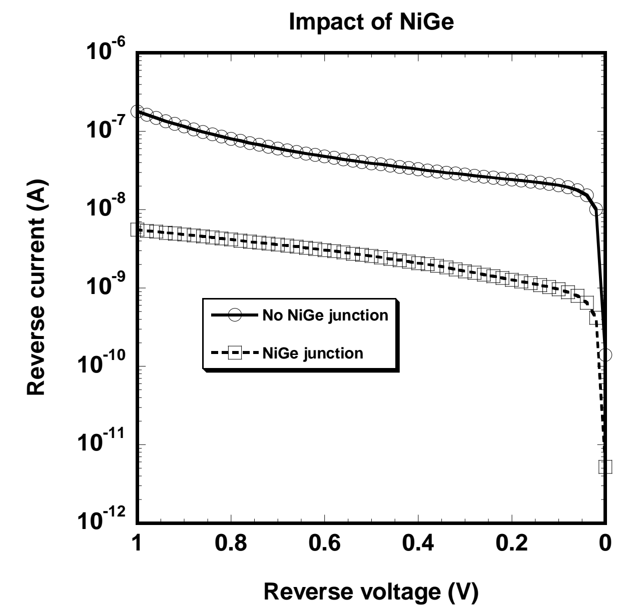
15 keV $5x10^{15}$ cm^{-2} P, 60 s at 500°C

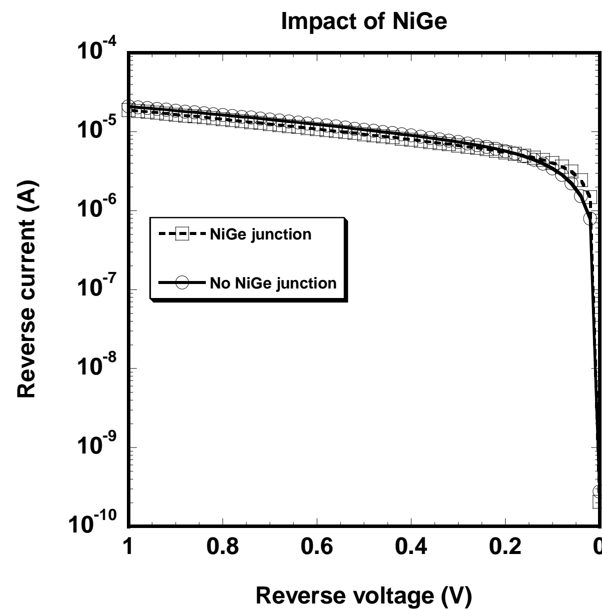
Impact NiGe on I_D



Impact NiGe on I_R







Junction Diode: Theoretical Analysis

Geometrical components

bulk – surface – corner

$$I_R = AJ_A + PJ_P + N_C J_C + I_{par}$$

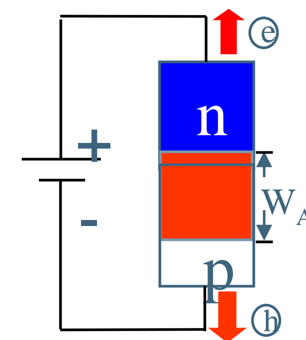
→ 3 diodes structures with different P/A ratios should be measured

Physical components

diffusion - generation

$$J_{dA} = qn_i^2\left(\frac{D_n}{L_n N_A} + \frac{D_p}{L_p N_D}\right)$$

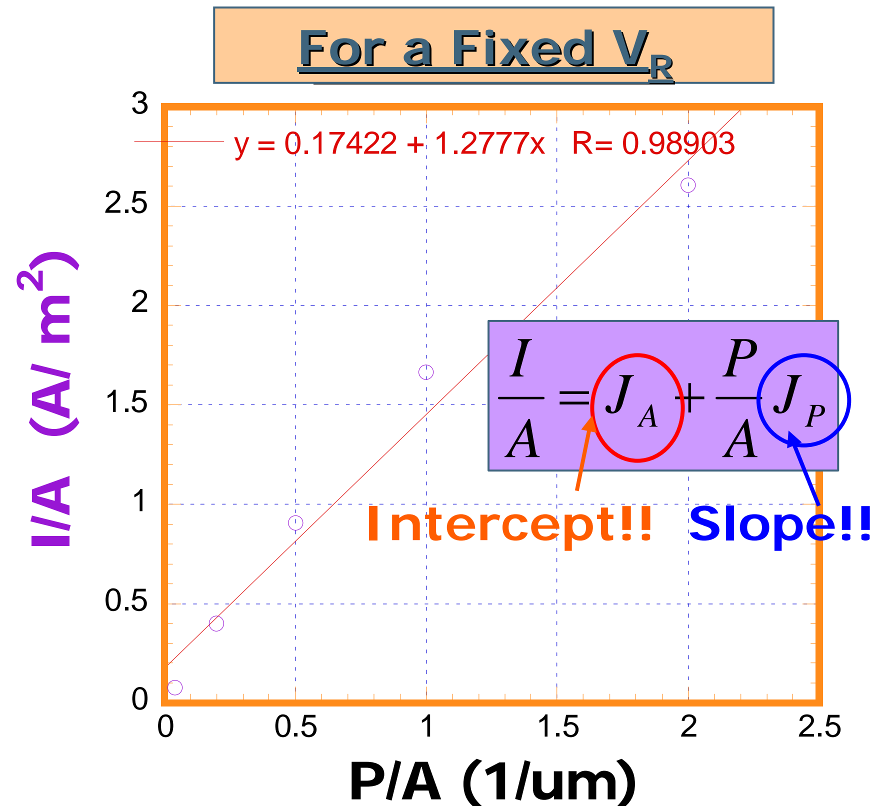
$$J_{gA} = \frac{qn_i W_A}{\tau_{geff}}$$



Junction Diode: Graphical Technique

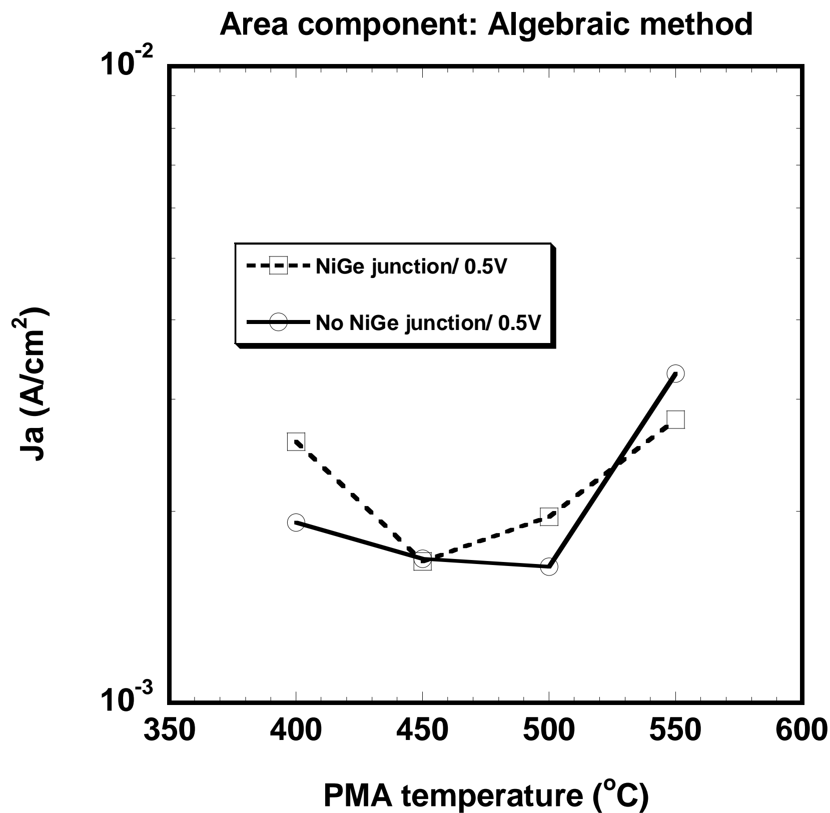
$$\frac{I_R}{A} = J_A + \frac{P}{A} J_P + \frac{N_C}{A} J_C + \frac{I_{par}}{A} \approx J_A + \frac{P}{A} J_P$$

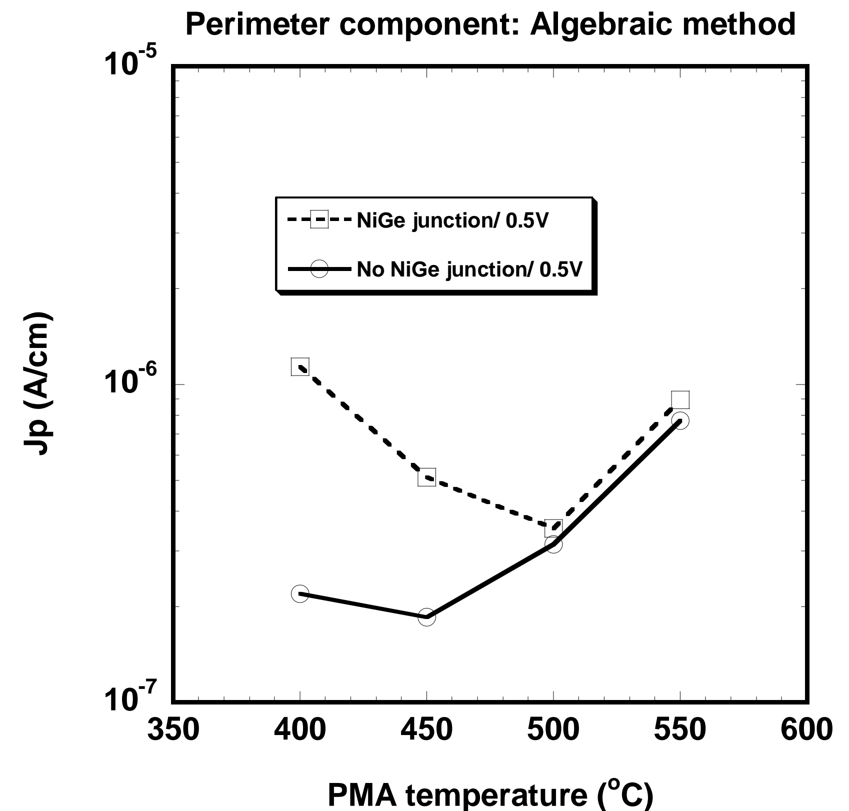
If there isn't corner generation component



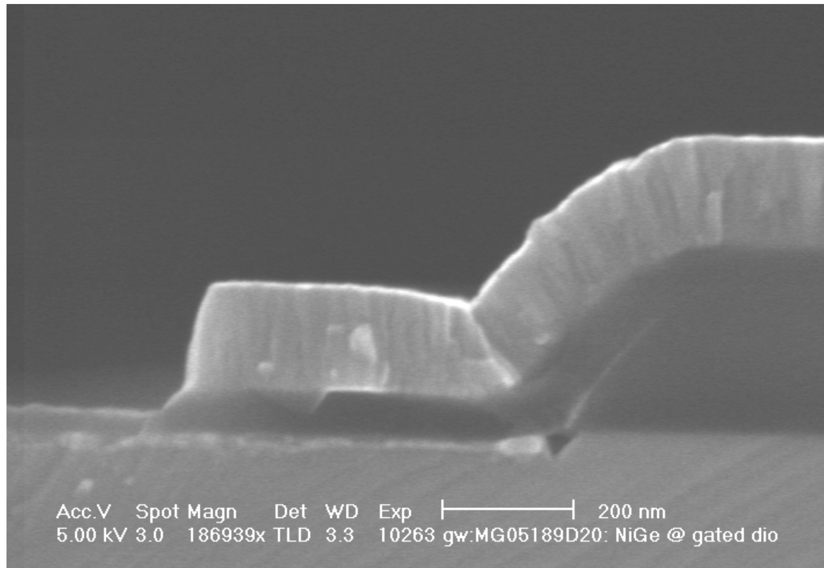
Impact NiGe and PMA

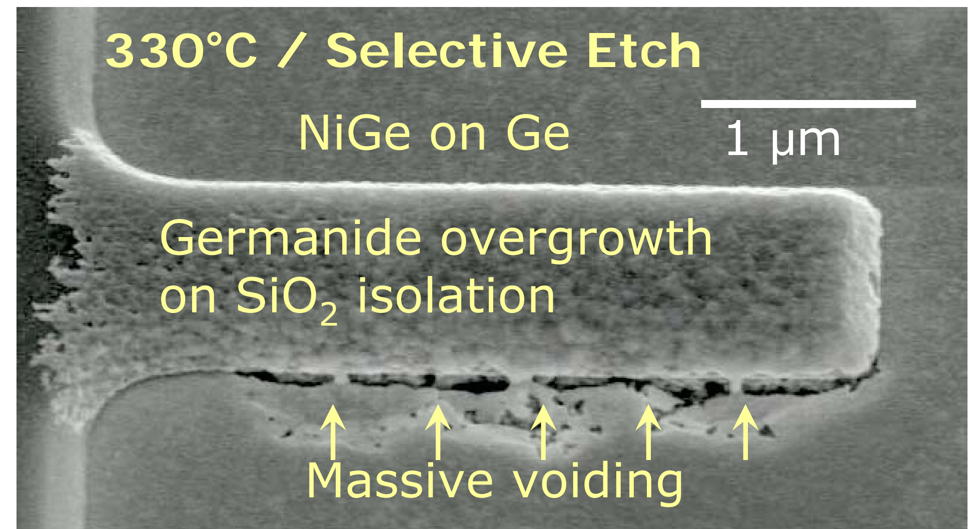
S. Sonde, E. Simoen, C. Claeys, A. Satta, B. De Jaeger, G. Nicholas and M. Meuris, in Avanced Gate Stack, Source/Drain and Channel Engineering for Si-Based CMOS 3: New Materials, Processes and Equipment, Electrochem. Soc. Trans., vol. 6, no. 1, 2007, pp. 31-39

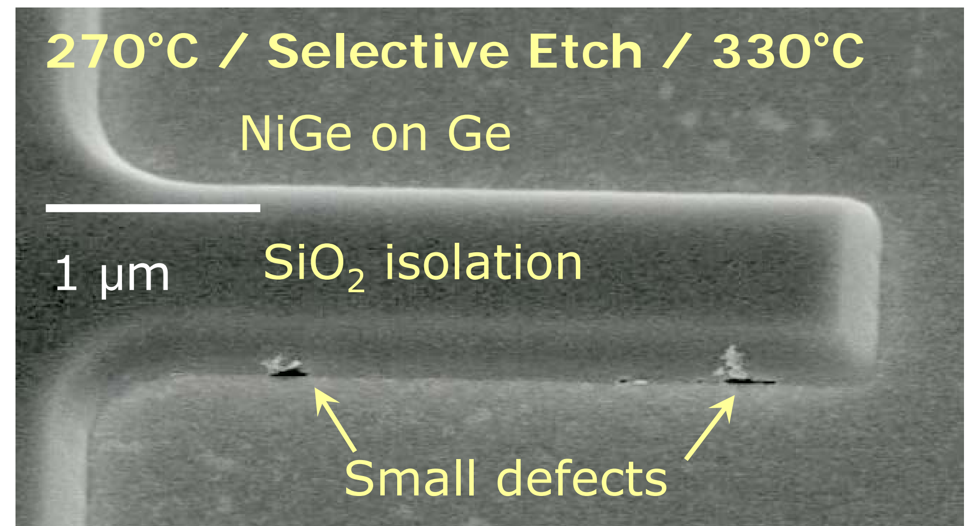




Experimental : Impact NiGe







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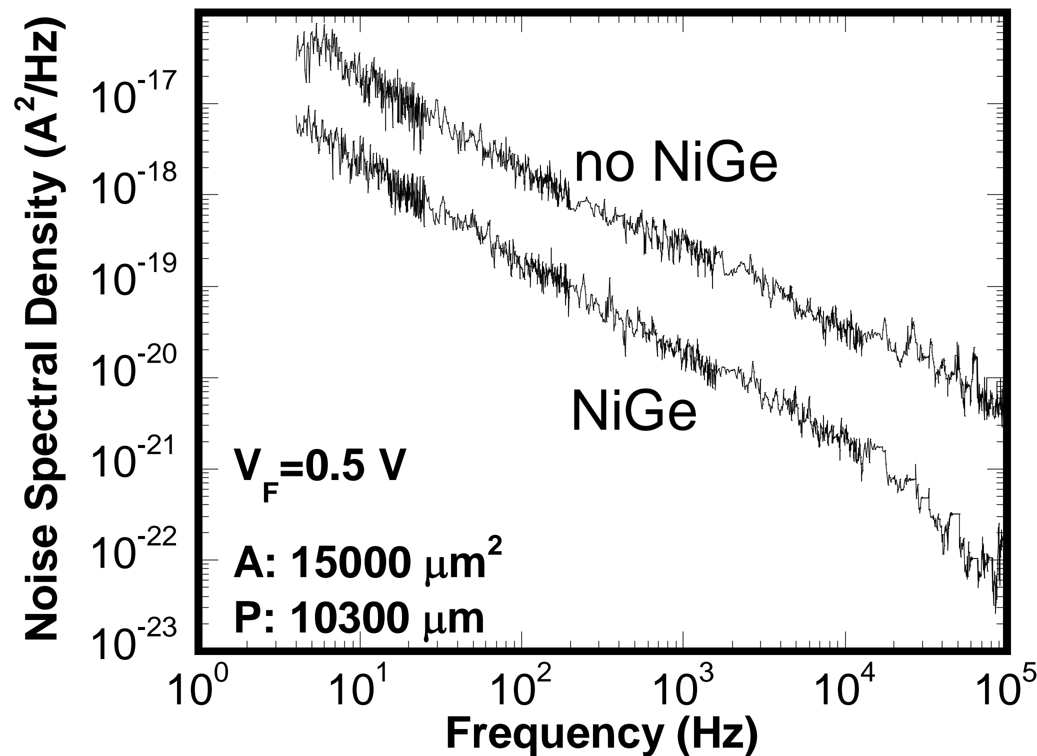
Impact NiGe on LF noise in p^+n Ge junctions

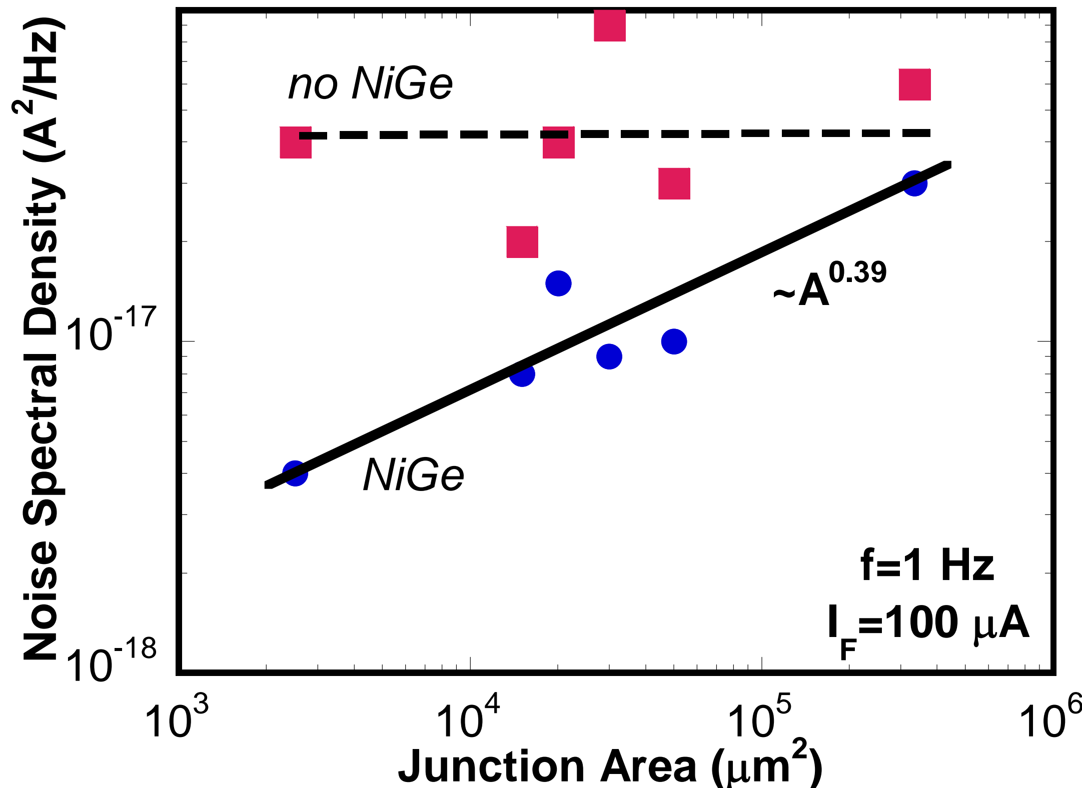
R.M. Todi, S. Sonde, E. Simoen, C. Claeys and K.B. Sundaram, Appl. Phys. Lett., vol. 90, no. 4, pp. 043501-1/3, 2007.



Low-frequency noise spectra for a germanided and a non-germanided p+-n junction at a forward bias of 0.5 V. The area is 15000 mm^2 and the perimeter P=10300 mm.

Germanidation: Impact on LF Noise

R.M. Todi, S. Sonde, E. Simoen, C. Claeys and K.B. Sundaram, Appl. Phys. Lett., vol. 90, no. 4, pp. 043501-1/3, 2007

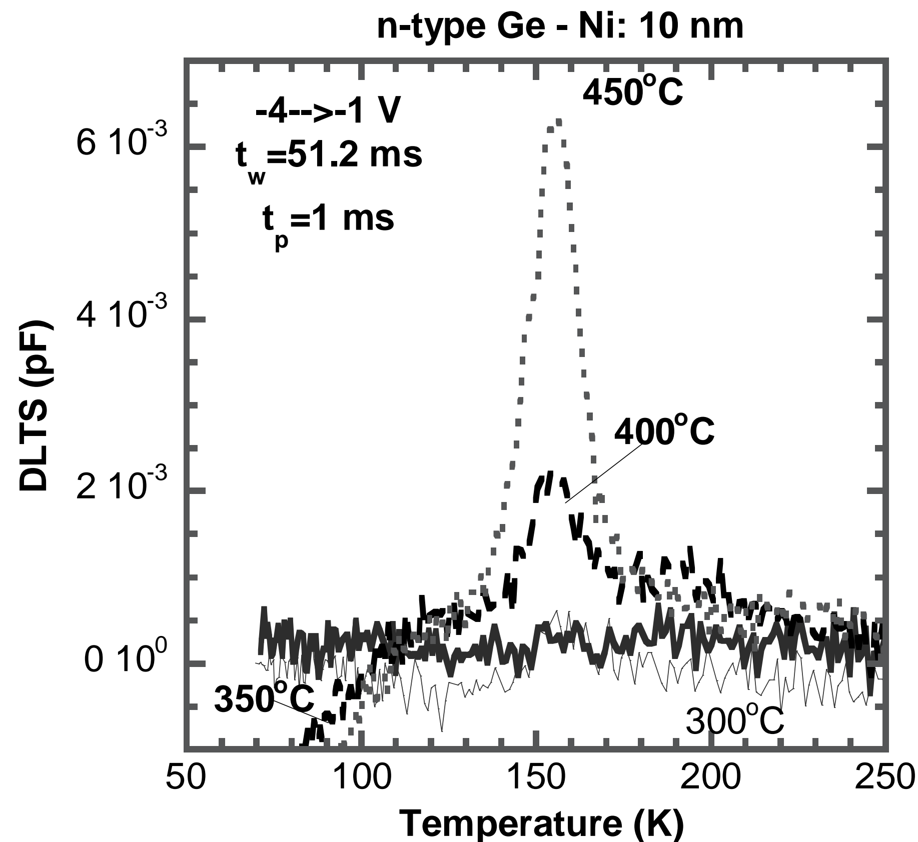


S_I is proportional with $A^{0.39}$

Defect-assisted GR noise origin

S_I at 1 Hz and 100 mA for NiGe germanided and non-germanided p^+-n junctions versus area.

Germanidation : Ni



Low temperatures used

Phase = f(T)

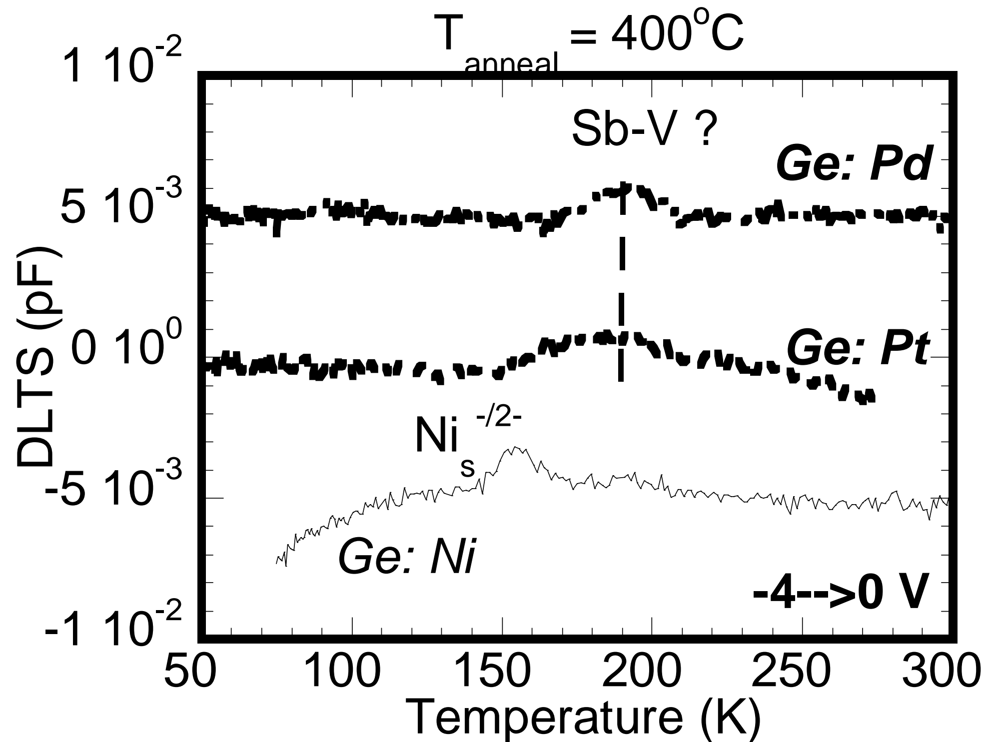
300-350°C: no deep electron traps

400-450°C: double acceptor at E_c-03 eV – substitutional Ni

Low defect concentration

DLT-spectra at t_w=51.2 ms, t_p=1 ms and a pulse from -4 to -1 V for a 4 mm diameter NiGe Schottky barrier on n-type Ge and corresponding with different RTA temperatures: 300, 350, 400 and 450°C

Germanidation : Pd and Pt



30 nm metal deposited by Ar sputtering

400°C: V-related traps

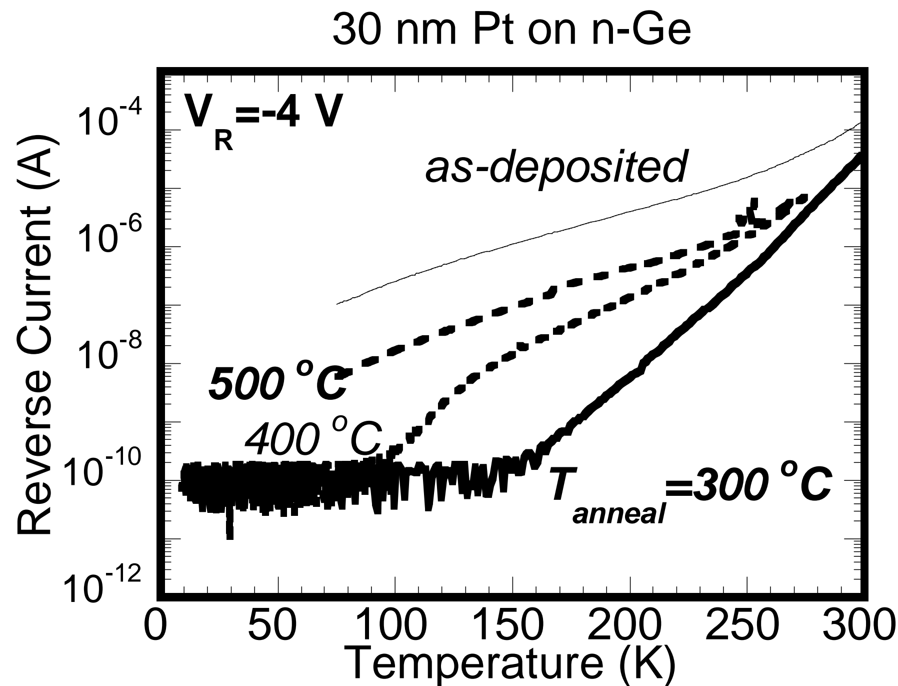
Sputter damage

Low defect concentration

DLT-spectra corresponding with a Ni-, Pt- and Pd-germanided n-type Ge Schottky barrier for an anneal temperature of 400°C. A bias pulse from -4→-1 V was applied for 1 ms, with a repetition time constant t_w=51.2 ms. The Ge: Ni and Ge: Pd spectra are offset in the y direction for reasons of clarity

Germanidation : Pd and Pt

E. Simoen, K. Opsomer, C. Claeys, K. Maex, C. Detavernier, R.L. Van Meirhaeghe and P. Clauws, J. Electrochem. Soc. Vol. 154, no. 10, 2007, pp. H857-H861



300°C –Pt_2Ge

400°C: PtGe

450°C: $PtGe_2$

200°C: Sputter damage reduces

I-T curves for the Pt-germanided n-type Ge Schottky barriers and for the pure Pt Schottky barrier indicated by as-deposited

Conclusions

- Good performing p-channel transistors have been fabricated

  mobility up to 350 cm^2/Vs for L =0.12 μm

- NiGe reduces the series resistance but increases the perimeter leakage current and lowers the LF noise

  voids in the silicon substrate

- PMA reduces the leakage current

  Optimum 450-500°C

Good understanding Ge processing

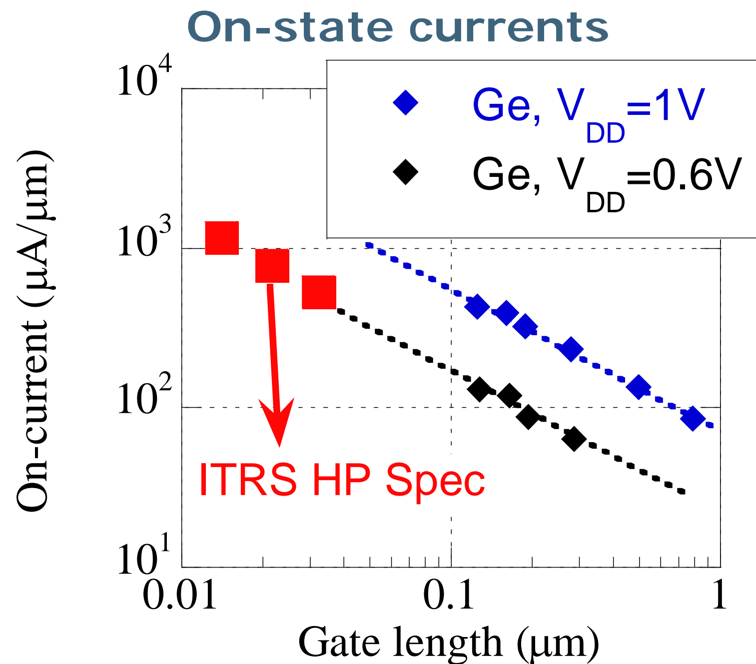
Ge pMOS vs. ITRS roadmap

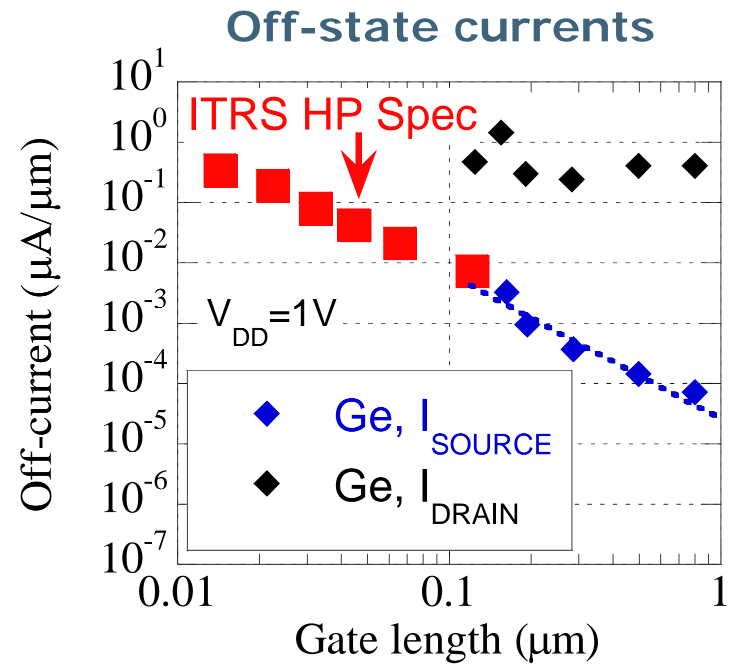
- I_{on} and I_{off} vs. gate length for (unstrained) Ge pMOS

  ITRS specifications for Si pMOS are used

  → I_{on}: High Performance ITRS spec seems obtainable with Ge pMOS

  → I_{off}: High Performance ITRS spec seems obtainable with GeOI technology





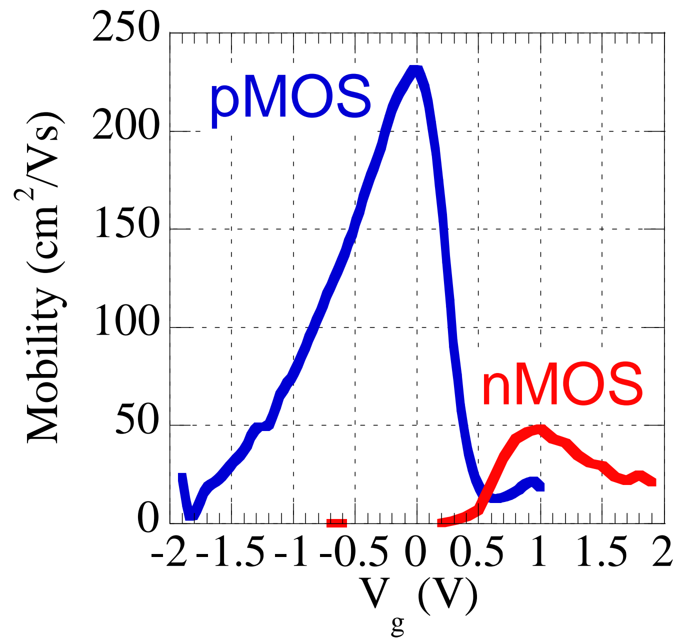
G. Eneman *et al.*

→ Ge pMOS could fulfill ITRS specs, for GeOI substrates

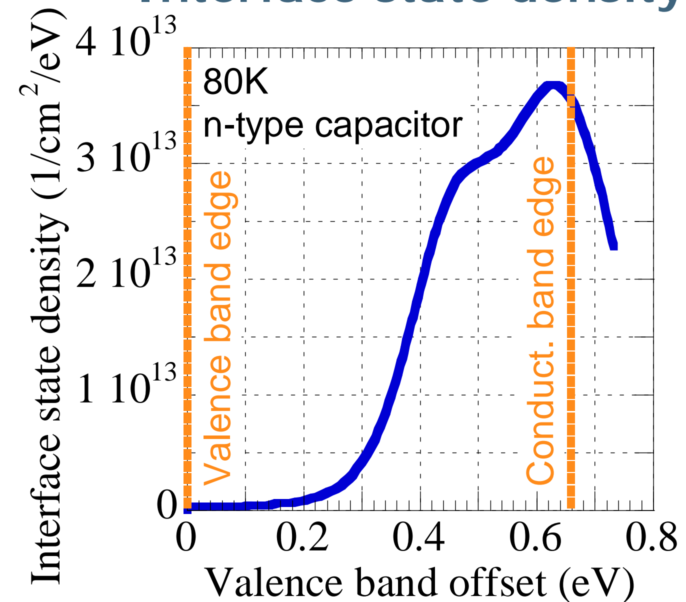
What about Ge nMOS?

- Low mobility/drive current measured for n-type MOSFETs (also in literature)
  - Si IL cannot passivate Ge nMOS. Accurate D_{it} analysis only at 80K [1]
  - Other potential problem: poor dopant activation for n-type dopants (activation limit for P ~ 6×10^{19} cm^{-3})

Ge nMOS and pMOS mobility



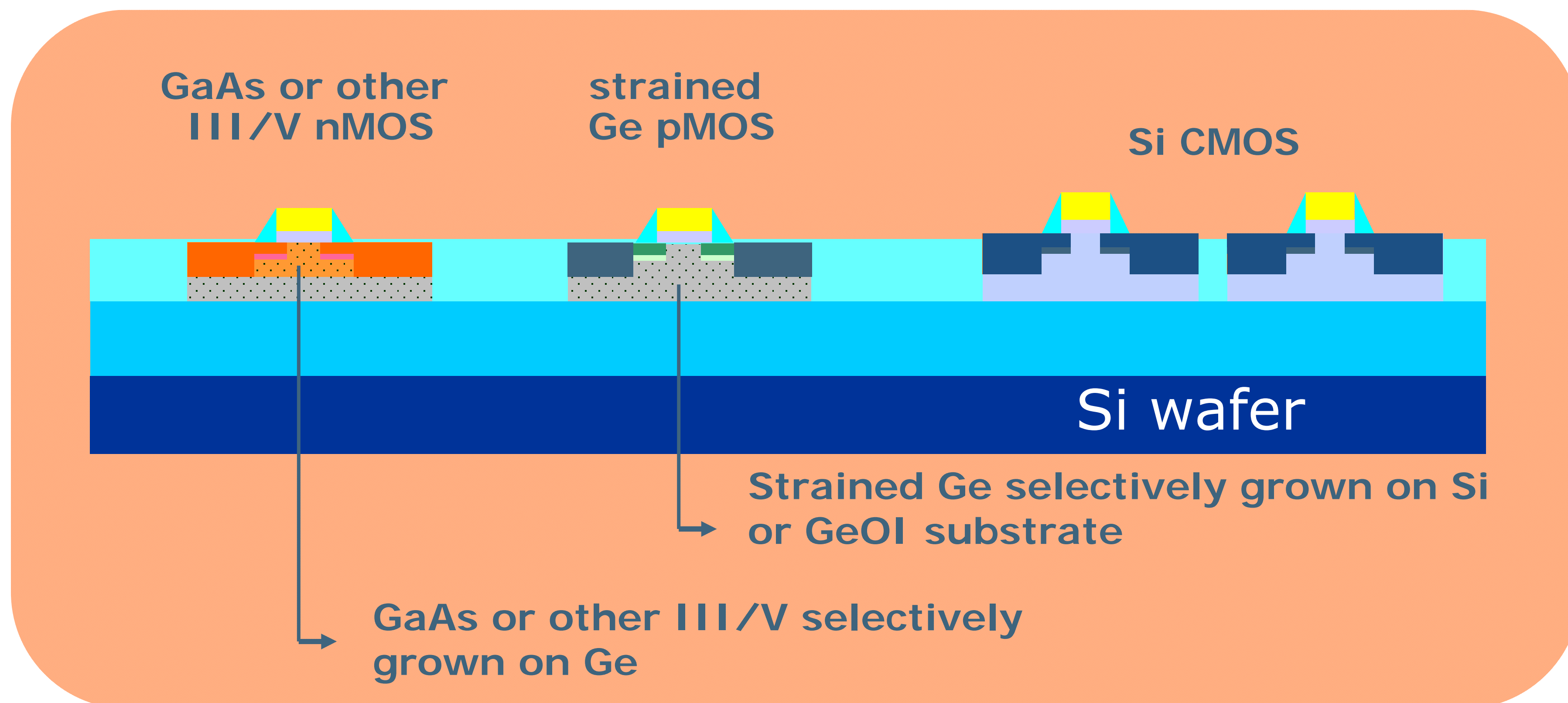
Interface state density



*[1] K. Martens et al., EDL **27**(5), 405 (2006)*

→ Consider other options for nMOS. nFET with GaAs?

Ge and III/V transistors



CMOS: Work towards combination of Si, Ge and GaAs or other III/V materials on one substrate

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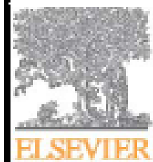
Conclusions



Germanium-Based Technologies

From Materials to Devices

Edited by Cor Claeys and Eddy Simoen

IMEC, Kapeldreef 75, B-3001 Leuven, Belgium

The aim of this book is to give an overview of today's Ge substrates – their grown-in and process-induced defects and how this impacts on the electrical performance of state-of-the-art CMOS processing and devices (junctions, capacitors, MOSFETs). At the same time, an insight into the basic Ge device and defect physics and modelling is provided.

Additional chapters describe CMOS (silicon compatible) processing, with special emphasis on the key issues: high-quality gate dielectric deposition on Ge and low-leakage shallow junction formation. Finally, an overview of alternative Ge devices that could be co-integrated on a silicon wafer (sensors, MEMS, optoelectronics, III-V epitaxy) is provided. In conclusion, an outlook and future trends are given.

Key features:
- First complete book on Ge, covering all fields from material growth to state-of-the-art processing
- Chapters written by key international experts in both academia and industry
- Broad coverage from fundamental aspects to industrial applications

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Chapter 2: Grown-in Defects in Ge
Chapter 3: Diffusion and Solubility of Dopants in Germanium
Chapter 4: Oxygen in Germanium
Chapter 5: Metals in Germanium
Chapter 6: *Ab-initio* Modeling of Defects in Germanium
Chapter 7: Radiation Performance of Ge Technologies
Chapter 8: Electrical Performance of Ge Devices
Chapter 9: Device Modeling
Chapter 10: Nanoscale Germanium MOS Dielectrics and Junctions
Chapter 11: Advanced Germanium MOS Devices
Chapter 12: Alternative Ge Applications
Chapter 13: Trends and Outlook