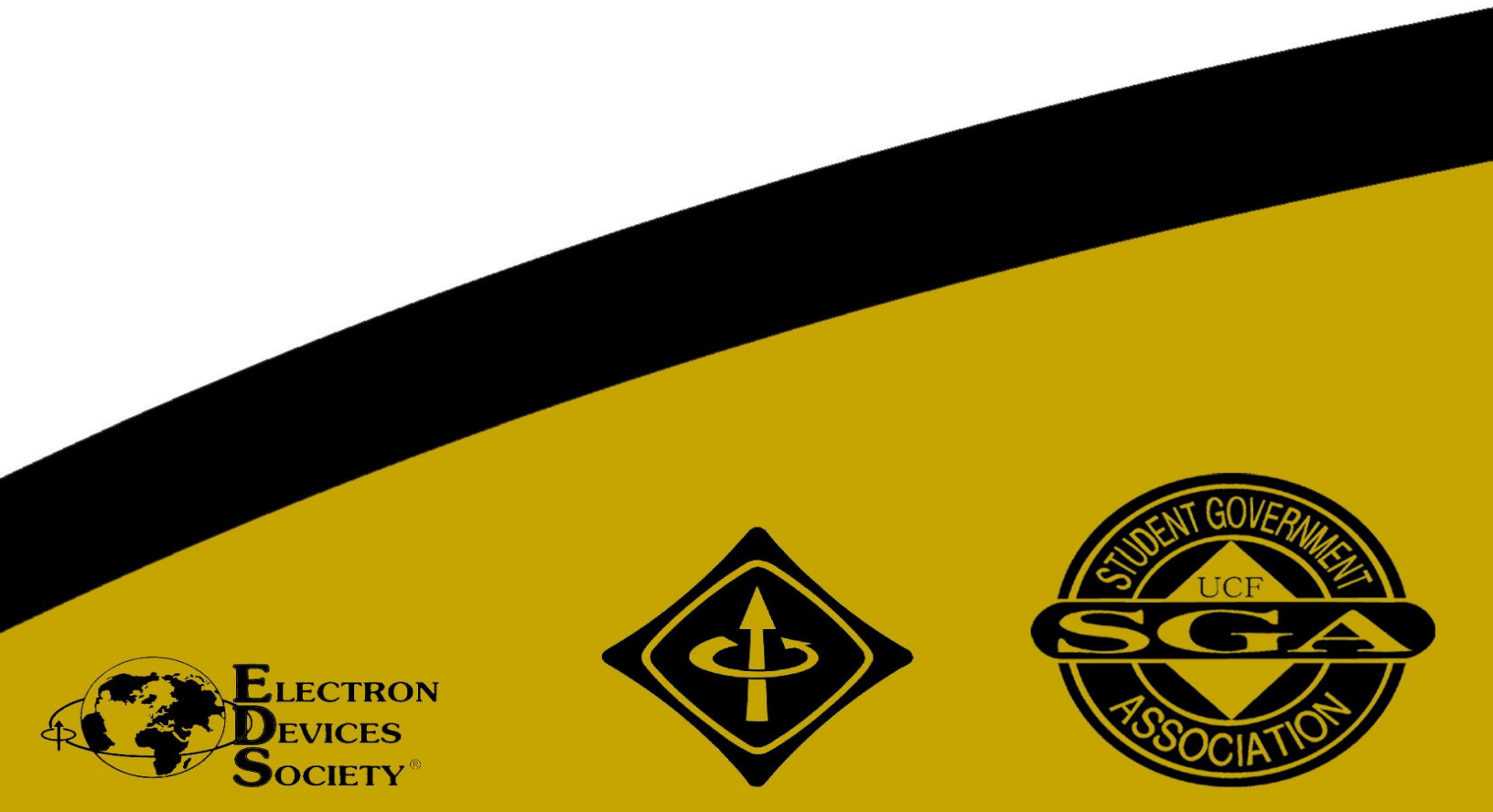
University of Central Florida

IEEE Electron Device Colloquium

Feb 21-22 2008



ELECTRON DEVICES SOCIETY®

Welcome

On behalf of the IEEE Electron Device Society (EDS) Orlando Chapter, I would like to welcome you to the IEEE EDS Mini-Colloquium. The technical program consists of nine talks given by internationally recognized lecturers in the field of electron devices. The topics include electron device evolution, new memory technologies, electrostatic discharge protection, nano-particles in semiconductor processes, high-frequency field-effect transistors, advanced germanium technologies, and optical modulators for analog fiber links.

This colloquium will provide an excellent opportunity for UCF graduate and undergraduate students to learn about the state of the art in micro/nanoelectronics, to interact and exchange ideas with the speakers, and to discuss research activities. Furthermore, it provides a great networking opportunity for all the IEEE members in the Central Florida region.

At this time, I would like to thank all the sponsors of this event: Student Government Association of UCF, IEEE Electron Devices Society, UCF School of Electrical Engineering and Computer Science, IEEE Orlando Section, and AVS and IEEE Student Chapters of UCF. I would also like to thank Dr. Juin J. Liou, EDS Vice-President of Regions/Chapters for his guidance, Dr. K. B. Sundaram ,the UCF student chapter adviser, Mr. Vinit Todi, President of IEEE Student Branch at UCF for his participation, and Ms. Blerina Aliaj, Ms. Lifang Lou and Mr. David Ellis for their logistic support. Last, but not the least, I thank all the lecturers for taking the time off their work to come to Orlando and participate in this event.

It is again my great honor and pleasure to extend a warm welcome to everyone. It is my hope that this colloquium is an intellectually enriching experience for all who attend.

Slavica Malobabić
Chair

Program

Thursday, Feb. 21st, 2008 (Harris Corporation Engineering Center (ENG 3) HEC 101)

8:00 - 8:30	Breakfast on site
8:30 - 8:50	Director's Message– Dr. Issa Batarseh (Director School of Electrical Engineering and Computer Science)
8:50 - 9:00	Opening Speech– Dr. Juin J. Liou (Professor School of Electrical Engineering and Computer Science)
9:00 - 9:15	Welcome Note– Miss Slavica Malobabic (Chair: IEEE Electron Device Society, Orlando Section)
9:15 - 10:15	Dr. Cor Claeys- Processing and Defect Control of Advanced Ge Technologies
10:25 - 11:25	Dr. James Vinson- Designing Electrical Overstress Robust Integrated Circuits
11:35 - 12:35	Dr. Subramanian Iyer- Beyond Scaling – Teaching the Old Dog some New Tricks!
12:45 - 2:30	Lunch
2:30 - 3:30	Dr. Eric Kay- Synthesis, Properties and Applications of Granular Composite Thin Film Systems
3:40 - 4:40	Dr. Frank Schwierz- Physics and Performance of Ultra-High-Frequency Field-Effect Transistors
4:50 - 5:50	Dr. Francisco Garcia Sanchez– A Succinct Overview of Electron Device Evolution
7:00 - 10:00	Banquet Dinner (By Invitation Only)

Program

Friday, Feb. 22st, 2008 (Harris Corporation Engineering Center (ENG 3) HEC 101)

8:30 - 9:00	Breakfast on site
9:00 - 10:00	Dr. Paul Yu - Optical Modulators for Transparent Analog Fiber Link
10:10 - 11:10	Dr. Jean-Jacques Hajjar- Predicting Circuit ESD Performance Through SPICE-type Simulation
11:20 - 12:20	Dr. Steven Voldman - Latch-up in Semiconductor Technology
12:30 - 1:30	Buffet Luncheon
1:30 - 7:30	Kennedy Space Center Tour
7:30- 10:00	Banquet Dinner (By Invitation Only)

Dr. Cor Claeys

Cor Claeys received the electrical-mechanical engineering degree in 1974 and the Ph.D. degree in 1979, both from the Katholieke Universiteit Leuven (KU Leuven), Belgium.

From 1974 to 1984 he was a Research Assistant and Staff Member, respectively, of the ESAT Laboratory of the KU Leuven and since 1990, a Professor. In 1984, he joined IMEC as Head of Silicon Processing Group. Since 1990 he was Head of the research group on Radiation Effects, Cryogenic Electronics and Noise Studies. Recently, he became as Director Advanced Semiconductor Technologies responsible for Strategic Relations. He is also member of the European Expert Group on Nanosciences. His main interests are in general silicon technology for ULSI, device physics, including low-temperature operation, low frequency noise phenomena and radiation effects, and defect engineering and material characterization. He coedited a book "*Low Temperature Electronics*" and on *"Germanium-Based Technologies: From Materials to Devices"* and wrote a monograph on "*Radiation Effects in Advanced Semiconductor Materials and Devices*". He also authored and co-authored eight book chapters and more than 750 technical papers and conference contributions related to the above fields. He has been involved in the organisation of a large number of international conferences and edited more than 35 Proceedings Volumes. He is an associated Editor for the *Journal of the Electrochemical Society*. He had short stays as Visiting Professor at the Queens University in Belfast, Ireland, and the University of Calabria, Italy.

Prof. Claeys is a Senior Member of IEEE and a Fellow of the Electrochemical Society. He was the founder of the IEEE Electron Devices Benelux Chapter, was Chair of the IEEE Benelux Section, was in the period 1999-2005 elected AdCom member of the Electron Devices Society (EDS), and was EDS Vice-President for Chapters and Regions during 2000-2006. Since 2000 he is an EDS Distinguished Lecture. In 2006, he has been elected as EDS President-Elect. and became EDS President in 2008. He also received the IEEE Third Millennium Medal. Within the Electrochemical Society he has been serving in different committees and was Chair of the Electronics Division (2001-2003). In 1999 he was elected as Academician and Professor of the International Information Academy. In 2004 he received the Electronics Division Award of the Electrochemical Society.

“Processing and Defect Control of Advanced Ge Technologies”

The boost up the device performance, strain engineering is gaining much interest and has already been successfully implemented for 65 and 45 nm technology nodes. However, for sub 32 nm another interesting approach is based on using again Ge as a substrate. Worldwide there has been much interest in investigating the potential of Ge processing.

This presentation will review the advantages and challenges of advanced Ge processing for future logic applications. Attention will be given to the processing challenges such as ion implantation, shallow junctions, passivation, gemanidation, contact technology, etc. For all the steps a good control of both the grown-in and the process-induced defects is crucial. Although very good electrical performances have been achieved for p-channel devices processed on Ge and GeOI high-mobility substrates, this is not the case for the n-channel ones. The future outlook will be briefly addressed.

Dr. James Vinson

James E. Vinson received the B.E.E. degree from Auburn University, Auburn, in 1982, the M.S. degree in Electrical Engineering from North Carolina State University, Raleigh, in 1984, and the Ph.D. degree in electrical engineering from the University of Central Florida, Orlando, in 1998. In the summer of 1984, he joined the Reliability and Failure Analysis Group at Intersil Corporation, Palm Bay, FL (formally called Harris Semiconductor). He is currently the Senior Manager of the Corporate Process Reliability Group at Intersil. His group is responsible for all wearout reliability evaluation of internal and foundry process for Intersil. He also is the ESD/EOS expert within Intersil and manages the ESD development team for all of Intersil processes. He has four patents and has published a book and numerous journal/ conference papers in the areas of reliability, ESD, and EOS.

“Designing Electrical Overstress Robust Integrated Circuits”

Electrical overstress (EOS) is the major cause of integrated circuit failure throughout its lifetime. This includes the semiconductor manufacture as well as in the equipment builder and end users. EOS is a classification of any electrical stimulus (voltage or current) which is applied to a part outside of its normal operating conditions. Examples of EOS range from the simple act of plugging a part in the socket backwards to the extreme of a lightning discharge. The cost of protecting against all forms of EOS may be prohibitive so it is important to understand the operating environment a circuit is expected to see during its life and the most likely forms of EOS in that environment. Establishing this criteria forms the first stage of designing a circuit for EOS robustness.

Battery operated hand held devices could be exposed to EOS in the form of a consumer putting the battery in backwards so the circuit would need to be designed to accommodate reverse battery voltage without damage. Telecommunication equipment is subjected to lightning strikes. These lines have lightning protection on them but some energy may still reach the integrated circuit. Understanding the peak voltage and current waveform of this residual lightning helps to design the output so it will survive a lightning strike. In the automotive industry, circuits are powered from the battery in the car. This bus must be able to handle a load dump which is an inductive voltage spike on the system power bus. Each electronic circuit on the power bus must be made robust to this voltage spike. This talk will present an overview of EOS and look at some common forms of EOS in power management, industrial and consumer electronics as well as providing options that could be employed to make circuits more EOS robust.

Dr. Subramanian Iyer

Subramanian S. Iyer is Distinguished Engineer and Chief Technologist for the Semiconductor Research and Development Center, IBM Systems & technology Group, and is responsible for setting semiconductor technology direction. Till recently he was Director of 45nm CMOS Development. He obtained his B.Tech in Electrical Engineering at the Indian Institute of Technology, Bombay, and his M.S. and Ph.D. in Electrical Engineering at the University of California at Los Angeles. He joined the IBM T. J. Watson Research Center in 1981 and was manager of the Exploratory Structures and Devices Group till 1994, when he founded SiBond LLC to develop and manufacture Silicon-on-insulator materials. He has been with the IBM Microelectronics Division since 1997. Dr. Iyer has received two Corporate awards and four Outstanding Technical Achievement awards at IBM for the development of the Titanium Salicide process, the fabrication of the first SiGe Heterojunction Bipolar Transistor and the development of embedded DRAM technology and the development of eFUSE technology. His current technical interests and work lie in the area of 3-dimensional integration for memory sub-systems and the semiconductor roadmap at 22nm and beyond. He holds over 40 patents and has received 19 Invention Plateau awards at IBM. He received the Distingushed Aluminus award from the Indian Institute of Technology, Bombay in 2004. Dr. Iyer has authored over 150 articles in technical journals and several book chapters and co-edited a book on bonded SOI . He has served as an Adjunct Professor of Electrical Engineering at Columbia University, NY. Dr. Iyer is a Fellow of IEEE and a Distinguished Lecturer of the IEEE.

"Beyond Scaling – Teaching the Old Dog some New Tricks!"

While the semiconductor industry has been focused on the challenges of scaling, it has become quite apparent that one must take a broader view of delivering productivity and performance gains in this new regime of non-classical scaling. While transistor level and interconnect performance will continue to make strides through the innovative use of stress engineering, novel materials such as high k dielectrics in the front end and low k dielectrics and high conductivity interconnects in the backend, there is much more to be gained by addressing the issues of memory integration including three dimensional integration, , on-chip decoupling and autonomic chip functions.

The scaling of memory poses a very significant challenge as it is quickly becoming a dominant part of the chip real estate and easily exceeds 70% of the chip area and contributes immensely to processor performance. Till recently most of this memory was SRAM. But SRAMs have not scaled gracefully for several reasons and we have begun to use embedded DRAMs for fast dense memory. We will examine the tradeoffs and technological and design advances that have made this possible to use embedded DRAMs to replace large blocks of SRAM memory and are being used extensively in network switches and high performance computing such as the BlueGene® chip as the onboard cache. More recently, we have been able to integrate trench based eDRAM in high performance processor technology as well and show a significant improvement in DRAM performance through a combination of process technology, DRAM architecture and circuit design. However, even wit these innovations, on-chip memory is necessarily limited and it will be necessary to explore the third dimension

Trench base DRAM technology, also lends itself to some very novel decoupling solutions. Typically modern logic chips switch at rates of several GHz and at these frequencies there are significant transient voltage droops called voltage compression. The local collapse of the power grid on a chip can lead to unpredictable results including functional breakdown, and memory failure. We look at the ways in which trench based on-chip decoupling alleviates these problems. This allows a 25X increase in decoupling capacitance for the same area and this can result in an almost 5-8 % decrease in power or equivalently a corresponding improvement in performance. The innovative use of a simple passive element gives us half a generation advantage.

Finally, we have developed the concept of an electrical fuse based on electromigration that can be combined with on-chip built in test and repair system. This can be used for chip repair at wafer level, in the package and in the field, power management, Bill of Materials, Yield management and a host of autonomic functions as well as onetime programmable memory. We will explore these applications.

While scaling and innovative new materials will continue to provide density and performance improvements to CMOS technology, a judicious use of memory technologies, the innovative use of on chip structures such as trenches for decoupling and the innovative use of phenomena such as electromigration and three dimensional integration will continue to provide huge benefits in altogether new dimensions.

Dr. Eric Kay

Dr. Eric Kay got his PhD in High Temperature Thermodynamics.
He spent 35 years with the IBM Research in San Jose, California, heading up the Surface, Thin Film, and Plasma Science Research Groups. From 1991 to 1998 he was on the Faculty at Stanford University in the Material Science and Engineering Department. His personal research throughout his career has included many aspects of plasma science in the context of thin film science and technology. His most recent personal research has centered around two distinct areas.

1.) Granular composite thin film science and
2.) Low Dimensional and Interfacial Magmetism.

He is a Fellow of the American Physical Society as well as the American Vacuum Society and was the first recipient of the John Thornton Memorial AVS Award as well as the recipient of US Senior Scientist von Humboldt Award. He received an honorary doctorate from the University ofKarlsruhe. He has served in numerous capacities in the AVS and is presently the Editor of JVST, Critical Reviews and also serves as one of the AVS Distinguished Lecturers. He is the author of 8 book chapters and 175 refereed papers in thin film science. He also holds 12 patents.

"Synthesis, Properties and Applications of Granular Composite Thin Film Systems"

Metal nano particles can be readily dispersed in an inert polymer thin film matrix in order to study a variety of physical and chemical properties as a function of size, shape and especially volume fraction of such nano particle composites. Among a number of possible synthetic approaches, plasma enhanced chemical vapor deposition of polymer and simultaneous sputtering of any metal is especially well suited to making a large variety of such composite thin film systems using low temperature processing throughout. Optical, electrical, magnetic and mechanical properties reflect dramatic changes as a function of particle size and volume fraction of these nano particle composites, especially when reaching the onset of percolation. Post deposition annealing above the glass/rubber transition temperature of the dielectric polymer matrix leads to metal nano particle migration and coalescence. Irradiating such composite films with spatially confined, scanning heat sources can lead to a variety of applications such as circuit writing or single domain ferromagnetic arrays. Noble metal and transition metal dispersions in hydrocarbon and fluorocarbon thin film matrices will be described as prototype systems for this approach.

Dr. Frank Schwierz

Frank Schwierz received the Diploma, Dr.-Ing., and Dr. habil. degrees from Technische Universität (TU) Ilmenau, Germany, in 1982, 1986, and 2003, respectively. Since 1985, he was responsible for the GaAs research at TU Ilmenau. Together with partners from German universities and industry he was involved in the development of the fastest Si-based transistors worldwide in the late 1990s. Presently he serves as Privatdozent at TU Ilmenau and is the Head of the RF & Nano Device Research Group. His research interests include semiconductor device simulation and modeling, very high-speed transistors, and novel material and device concepts for future ULSI and RF transistor generations. He is conducting research projects funded by the European Community, German government agencies, and the industry. He has published 130 journal and conference papers including more than 15 invited papers, and is authors of the book *Modern Microwave Transistors – Theory, Design, and Performance* (J. Wiley & Sons 2003). Another book entitled *Nanometer CMOS* will be published in 2008.
Dr. Schwierz is a Senior Member of the IEEE.

“Physics and Performance of Ultra-High-Frequency Field-Effect Transistors”

In this talk, the present understanding of the physics and design of high-frequency field-effect transistors (FET) is reviewed. Based on rather general (and simple) considerations, important design guidelines for fast FETs are discussed. Furthermore, an overview of the state-of-the-art performance of high-frequency FETs is presented and future trends in this field are highlighted. Special emphasis is given to the recent improvements of the high-frequency performance of Si MOSFETs and to the competition among Si MOSFET and III-V HEMTs. It is shown that the MOSFET concept, when compared to HEMTs, offers some inherent advantages with respect to the high-frequency performance. Finally, the prospects of novel materials, such as narrow bandgap semiconductors and carbon, for high-speed devices are discussed.

Dr. Francisco Garcia Sanchez

Francisco. J. García Sánchez was born in 1947 in Madrid, Spain. He received the B.E.E., M.E.E. and Ph.D. degrees in Electrical Engineering from the Catholic University of America, Washington, DC, USA, in 1970, 1972 and 1976, respectively.

In 1977, Prof. García Sánchez joined the faculty of the Electronics Department at Universidad Simón Bolívar (USB), Caracas, Venezuela, where he was promoted to the Full Professor rank in 1987. He has held several directive positions within USB academic administration, such as Coordinator of Undergraduate and Graduate Studies in Electronics Engineering, Coordinator of Applied Sciences Research, and elected faculty member to USB's Academic and Superior Councils. He has been actively involved, both locally and internationally, in the promotion, planning, direction, management and evaluation of many R&D endeavors. He was National Coordinator for Electronics in Venezuela's New Technologies Program. He has been the President of the Engineering Commission in Venezuela's System for the Promotion of Research, and a member of its Appeals Committee. He was for several years a member of the External Evaluation Commission of Mexico's National Institute of Astrophysics, Optics, and Electronics. He presently holds a Research Professorship chair at USB, is a Level IV Researcher (highest rank) in Venezuela's Scientific Research System, and is an EDS Distinguished Lecturer since 2003. He has been the recipient of several awards for excellence in research. In February 2007 he received the honorary title of "Professor Emeritus of Simón Bolívar University."

Prof. García Sánchez was in charge of the creation in 1979 of USB's Solid State Electronics Laboratory (LEES). Its functions are teaching and research and serves the Masters and Doctorate Solid State programs in electronics engineering at USB. It maintains academic cooperation with other research groups in Latin America, the European Union, and the U.S.A.

Prof. García Sánchez early research experience was in the areas of polycrystalline compound semiconductor thin- and thick-film deposition techniques for photovoltaic solar cells and sensors, and the electrical characterization and modeling of biological tissues, ceramics and other composite materials. His group's present research interests lay mainly in the area of semiconductor device modeling, especially field effect devices. He has published over 120 technical articles in refereed technical journals and specialized conferences, including numerous invited and plenary talks. He is the co-author of a book on MOSFET modeling, and has been the editor of several specialized collective works. He serves as reviewer for specialized technical journals and has been active in editorial work as well as in numerous conference organization activities. Since 1994 he has shared the responsibility for steering the organization of the CAS and EDS co-sponsored "International Caribbean Conference on Devices, Circuits and Systems (ICCDCS)," whose seventh edition is due to be held on April 2008, in Mexico.

Prof. García Sánchez is a member of the Venezuelan Association for the Advancement of Science, a founding member and past Vice-President of the Galilean Society, and a Senior Member of the IEEE. He is past Chair of IEEE´s CAS/ED/PEL Societies Venezuela Joint Chapter, and past member of the IEEE Leon K. Kirchmayer Graduate Teaching Award and Undergraduate Teaching Award Committee. He is presently a member of EDS Master and PhD Student Fellowships Subcommittee, Vice-Chair of EDS Subcommittee for Regions & Chapters for Latin America (SRC-LA), and an elected member of EDS Administrative Committee (AdCom).

"A Succinct Overview of Electron Device Evolution"

The integrated circuit, as the fundamental technological basis of the present post-industrial information society, represents Engineering's highest achievement. It constitutes the most complex apparatus that human beings have ever fabricated. Since 1965 when Gordon Moore published the first projection about IC density growth, the number transistors per chip has been doubling approximately every 2 two years, as a result of the continuous shrinking of transistor size. A historic retrospective of the impact of microelectronics's evolution indicates that miniaturization has enabled the spectacular growth of function density and speed of ICs. Not less important has been the role of miniaturization in cost reduction and in the explosive development of the world-wide semiconductors market. However, nowadays miniaturization seems to be reaching a stage where it is becoming increasingly difficult to continue shrinking much more the size of conventional, CMOS type, transistors. The difficulty stems mainly from physical barriers, but also from technological complications. Fundamental physical limitations show up when the transistors feature sizes approach interatomic dimensions. New manufacturability challenges also arise for such minuscule structures. Additionally there are several economic issues that must also be resolved. Consequently today, and for the first time since 1965, it has become very difficult, or even impossible, to continue predicting the future of the semiconductor industry much further than the next decade, because everything seems to indicate that the miniaturization of conventional transistors will reach its limit approximately in that period. In spite of that, we will sketch a view of the likely future evolution, offering some insight on tentative projections and tendencies. We will consider the short term (10 to 15 years) and will try to visualize several possibilities of what might come afterwards, projecting three fundamental directions: Miniaturization (More Moore), functional diversification (More than Moore), and heterogeneous integration (Beyond CMOS). Among other aspects, we will present some emerging nanosize MOSFETs, potential new materials and devices, such as graphene, carbonanotubes, nanowires, nanodots, spintronics, as well as the progress of other nonconventional devices which do not relay on massive flow of electrons. Finally we will come to conclude that Moore's Law has not really died, but only has changed the way in which it continues to rule electronics.

Dr. Paul Yu

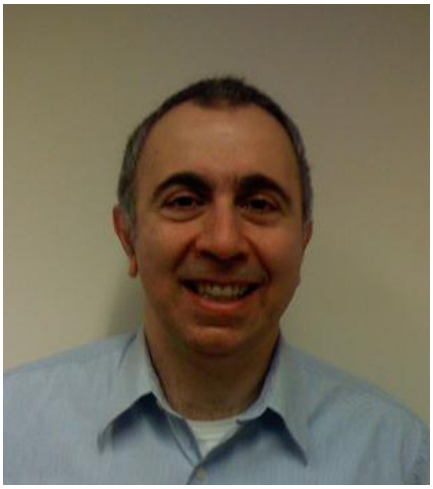
Dr. Yu is a professor at the Department of Electrical and Computer Engineering at the University of California at San Diego (UCSD). At UCSD he offers courses in solid state electronics and optoelectronics as well as conducts research on semiconductor materials and devices for various photonics and microwave applications. His research interests include: lasers in the near infrared wavelength region for optical communication and optical interconnection; optical/RF schemes for narrow-band, high center frequency microwave transmission; high speed, high power optical detectors and high speed waveguide modulator devices for both digital and analog modulation; high power semiconductor optical switches for microwave generation; and electronic analog-to-digital conversion using high speed optical switches. He is a founding member of the IEEE AP/ED/MTT Chapter of San Diego, and is presently the Vice-President of Education Activities at the IEEE Electron Devices Society. He is a Fellow of IEEE, Optical Society of America and SPIE.

“Optical Modulators for Transparent Analog Fiber Link”

This presentation gives an overview of the requirements of the photonic components in their insertion in applications such as CATV, antenna remoting and base station connections in wireless communication systems. The fiber-optic links are commonly used in these systems. For analog transmission, the gain and linearity properties are critical in the overall performance of the transmission system. Among the components of a fiber-optic link, the performance of optical modulator is of primary importance and has been broadly studied for advancing the analog fiber link. The presentation reviews the advances in the state-of-the-art optical modulators for analog fiber links with some discussion of the possible use of nanowires for modulator application. Much of the emphasis will be given to semiconductor electroabsorption modulator (EAM).

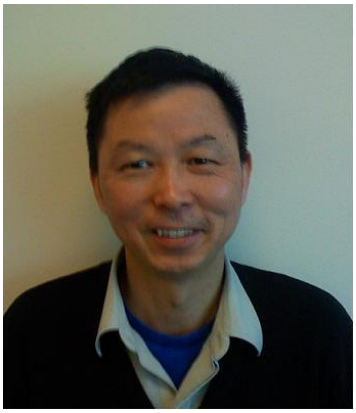
Semiconductor electroabsorption modulator (EAM) with high gain is very attractive due to the small size of the transmitter. EAMs using multiple-quantum-well (MQW) active layers have been popular as they typically have a large absorption-coefficient change with applied electric field. The peripheral coupled waveguide (PCW) MQW EAM was designed for low optical loss and high analog gain operation. In PCW EAM, the active region is placed at the peripheral, evanescent field region of the optical waveguide mode such that a large portion of the optical mode is inside the low loss region; the corresponding analog link gain approaches a limit close to transparency as the optical power is raised. The negative feedback in the EAM attributed to the photocurrent generation improves the modulator linearity but causes the transmission to saturate at high optical power. The implications for high link gain, low noise figure analog link will be presented.

Dr. Jean-Jacques Hajjar



Jean-Jacques Hajjar received the B.S, M.S and PhD degrees from the Massachusetts Institute of Technology, Cambridge, MA, in 1983, 1985 and 1989 respectively.
He is currently the manager of the Corporate ESD Department at Analog Devices, Wilmington, MA. Dr. Hajjar is focused on improving ESD and latchup robustness for all Analog Devices products. Prior to his current role, Dr. Hajjar was involved, also at Analog Devices, in fully-isolated bipolar IC process development and SPICE device modeling for predictive circuit simulations. Dr. Hajjar was also a leading team member at Polaroid Corporation (Waltham, MA) for the characterization of thin film material for low-cost high efficiency solar-cell development.

Dr. Yuanzhong (Paul) Zhou



Yuanzhong (Paul) Zhou received a BS degree in 1982 and a MS degree in 1988 from Huazhong University of Science and Technology (HUST), Wuhan, China, both in physics. He received a MSEE degree in 1997 and a Ph.D. degree in electrical engineering in 1998 from Northeastern University, Boston, MA.

From 1988 to 1992, he was a lecturer at HUST, where he taught physics courses and was involved in research in the fields of solid state physics and applications of electrostatics. After worked at Fairchild Semiconductor for 7 years as a modeling engineer, he joined Analog Devices Inc. (ADI) in 2005, where he is a senior ESD engineer working on ESD technology development in the Corporate ESD Department in Wilmington, Massachusetts.

Thorsten Weyl

Thorsten Weyl received the Dipl. Ing. in European Electrical Studies from the University of Applied Sience Osnabrueck in 1998 and the M. Eng. in Electrical Engineering from the University of Limerick in 2003. He works in the Mixed-Signal CAD group of Analog Devices in Limerick Ireland since 1998. His primary responsibilities are in the area of ESD simulation and layout automation.

“Predicting Circuit ESD Performance Through SPICE-type Simulation”

Predicting the electro-static discharge performance of a circuit design prior to manufacturing is very appealing. Circuit level simulation using accurate models is critical in ensuring that ESD protection works properly. This allows circuit designers to evaluate the ESD robustness of their design, optimize it and most importantly reduce the number of design iterations in order to meet the product's minimum protection specifications.

A practical macro-modeling approach composed of industry standard BJT and MOS compact models is presented. The approach has advantages of simple implementation, high simulation speed, wide accessibility and fewer simulation convergence issues. Moreover, the said models include most key physical device effects resulting from and ESD event. SPICE-type circuit level simulation that uses these models is demonstrated. These include examples at both the I/O cell as well as full-chip levels.

Steven Voldman

Dr. Steven H. Voldman is an IEEE Fellow for "Contributions in ESD protection in CMOS, Silicon On Insulator and Silicon Germanium Technology." He was the recipient of the ESD Association Outstanding Contribution Award in 2007.

He received his B.S. in Eng. Science from Univ. of Buffalo (1979); a first M.S. EE (1981) from Massachusetts Institute of Technology (MIT); a second degree EE Degree (Engineer Degree) from MIT; a MS Eng. Physics (1986) and a Ph.D EE (1991) from Univ. of Vermont under IBM's Resident Study Fellow program.

Dr. Voldman was a member of the semiconductor development of IBM for 25 years. He was a member of the IBM's Bipolar SRAM development, CMOS DRAM development, CMOS logic, Silicon on Insulator (SOI), BiCMOS and Silicon Germanium developmnt. More recently, he was a member of the RF Silicon Germanium (SiGe), RF CMOS development, RF SOI, smart power technology development and image processing technology teams. He is presently a member of the Qimonda DRAM development team, and reporting to Qimonda Europe working on 70, 58 and 48 nm technology.

Dr. Voldman was chairman of the SEMATECH ESD Working Group, to establish a national strategy for ESD in the United States; this group initiated ESD technology benchmarking strategy, test structures and commercial test system strategy. He is a member of the ESD Association Board of Directors, ESDA Education Committee, as well ESD Standards Chairman for Transmission Line Pulse testing. Dr. Voldman was also the first chairman of the ESDA ESD Technology Roadmap committee and co-established the ESD Technology Roadmap in 2005. In 2005, he was the Subcommittee Chairman for both the Latchup Sub-committee for the International Reliability Physics (IRPS) and the EOS/ESD Symposium, the ESD Chairman for the International Physical and Failure Analysis (IPFA) Symposium, and presently serving on the technical program committees for the Taiwan ESD Symposium, International Conference on Electromagnetic Compatibility (ICEMAC, Taipei, Taiwan), Bipolar Circuit Technology Meeting (BCTM), IRPS, and EOS/ESD Symposium; Steve has provided tutorials on ESD, latchup, failure mechanisms, and RF ESD devices to the IRPS, EOS/ESD, BCTM, and IPFA.

Dr. Voldman has written over 150 technical papers between 1982 and 2007. He is a recipient of over 164 issued US patents and 91 US patents pending, in the area of ESD and CMOS latchup. Dr. Voldman also has written an article for *Scientific American* in October 2002. Dr. Voldman is an author of the book *ESD: Physics and Devices*, and the second book in the series *ESD:Circuits and Devices*, a third book, *ESD: Radio Frequency (RF) Technology and Circuits,* and fourth text, *Latchup,* as well as a contributor to the book *Silicon Germanium: Technology, Modeling and Design*.

In the ESD Association, Voldman initiated the "ESD on Campus" program which was established to bring ESD lectures and interaction to university faculty and students internationally; the ESD on Campus program has reached over 24 universities in the United States, Singapore, Taiwan, Malaysia, Philippines, Thailand, and China.

"LATCH-UP IN SEMICONDUCTOR TECHNOLOGY"

CMOS latch-up continues to be of interest today in advanced CMOS, BiCMOS to automotive, smart power and space applications. With technology scaling, non-native voltages and mixed signal applications, latchup is still a design and integration today. In the design of ASICs, with high level integration for system on chip (SOC) and network on chip (NOC) applications, new latchup issues are beginning to occur. In space applications, the threat of Single Event Latchup (SEL) is still a concern today.

The lecture will address latchup theory, physical bipolar device models, simulation, design criteria, latch-up test structures, test methods, latch-up measurement techniques, semiconductor process issues, circuit design techniques, latchup ground rules, and computer aided design methodologies.

The lecture will focus on the internal and external latchup problems today, and on new developments in failure analysis techniques and tools, and CAD methods being proposed today and for the future.

Notes

Notes

Colloquium Committee

Slavica Malobabić
Vinit Todi
Blerina Aliaj
David Ellis

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