On the Modeling of Undoped Double-Gate MOSFET

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ABSTRACT

We review classical physics based compact models of undoped double-gate SOI MOSFETs. The use of multiple-gate has emerged as a new technology to possibly replace the conventional planar MOSFET when its feature size is scaled to the sub-50 nm regime. MOSFET technology has been the choice for mainstream digital circuits for VLSI as well as for other high frequency applications in the low-GHz range. But the continuing scaling of MOSFET presents many challenges, and multiple-gate, particularly double-gate, SOI devices seem to be attractive alternatives as they can effectively reduce the short-channel effects and yield higher current drive.

The existing double-gate SOI MOSFET core compact models under review, which are in general developed based on the Pao-Sah formulation for the bulk MOSFET, define the drain current in terms of one of the following three different variables: surface potential, inversion charge, and auxiliary variables. Numerical simulations are included in order to assess the validity of the models reviewed.