An Overview of STT-RAM Technology – From Device Modeling to Applications

Date: Nov 16, 2011 (Wednesday)

Time: 6.00 -6.30 pm - Networking/ Refreshments
6.30 - 7.30 pm -Talk
7.30 - 8.00 pm - Q&A

Place: CoRE 503
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SPEAKER: PROF. HAI (HELEN) LI, NYU POLY

Abstract:

The introduction of heterogeneous multiprocessor system-on-chips (MPSoC) into embedded system designs, e.g. cellular phones, generates explosive demands on cache memories. The reliance on the conventional memory technologies in on-chip cache designs, however, raises the concerns about the costly auxiliary circuitry, the huge power consumption, and the significantly degraded reliability at nanoscale technology nodes. A new memory technology, spin-transfer torque random access memory (STT-RAM), combines the major advantages of all mainstream memories, including the fast access time of SRAM, the high integration density of DRAM, and the nonvolatility of Flash, and offers a better scalability. However, many technical obstacles need to be overcome when integrating STT-RAM technology into embedded system designs.

In this lecture, we will give a comprehensive overview on our research work on STT-RAM, from device, circuit design, architecture, and system applications perspectives. The critical issues (such as the impact of process variations, slow write speed, stochastic switching process, etc.) and the corresponding solutions will be presented. The goal of our work is to design a high-density, low-power, high performance STT-RAM based memory with high yield and simple architecture, and to utilize it in the next-generation SoC systems effectively.

Speaker Bio:

Dr. Hai (Helen) Li is an Assistant Professor of ECE Department of New York University. She received her B. S. and M. S. degrees from Tsinghua University, China and her Ph.D. degree in 2004 from Purdue University. Before joining NYU-Poly, Dr. Li worked for Qualcomm Inc., Intel Corp., and Seagate Technology. Her research interests include architecture/circuit/device co-optimization for green computing systems, emerging embedded memory design, and 3D integration technology and design. Dr. Li has published more than 50 technical papers in refereed journals and conferences, filed 51 U.S. patents (29 granted) and one Seagate Trade Secret. Her new book "**Nonvolatile Memory Design: Magnetic, Resistive, and Phase Changing**" will be published with CRC Press in 2011.

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