On-Chip Voltage and Timing Diagnostic Circuits

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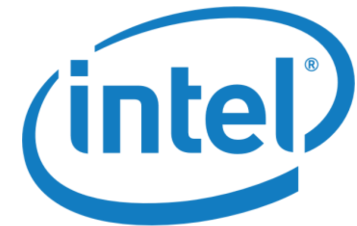
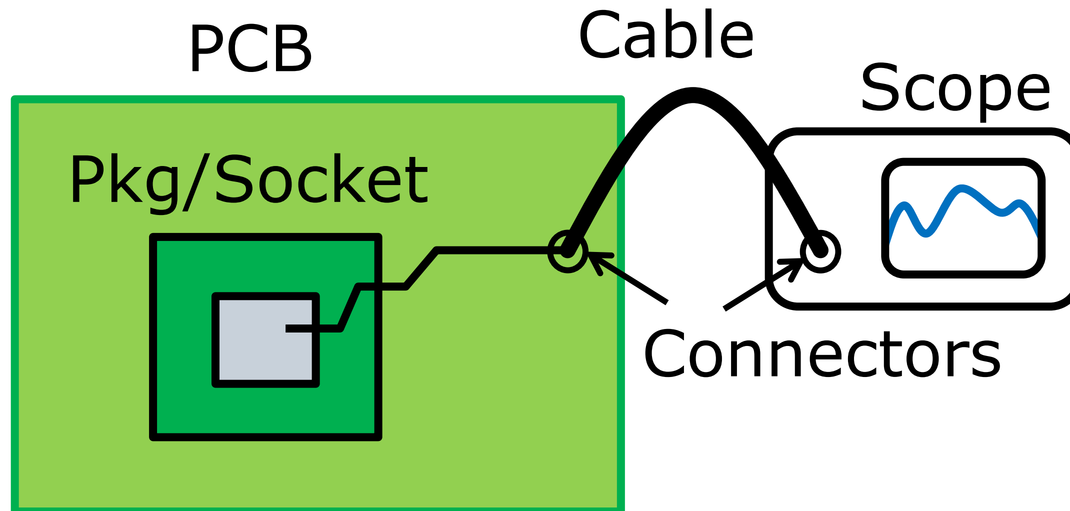
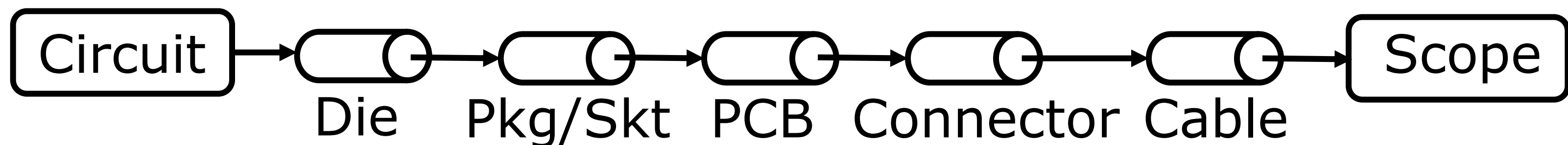


October 2014

Why Measure Time/Voltage On-Chip?

1. Routing signals to equipment can filter and corrupt measurement
   - Loss, delay, discontinuities, loading, noise





Why Measure Time/Voltage On-Chip?

2. Some measurements must be done w/o external equipment

Wafer Sort

Ref: www.besi.com

In-Situ Test

Ref: www.intel.com

Presentation Flow

- We'll discuss key metrics and the limitations of off-chip measurements
- Then we'll see how to solve these with on-die measurement circuits
- My objective is that you will leave today with a set of simple but very useful techniques that you can apply to your own designs

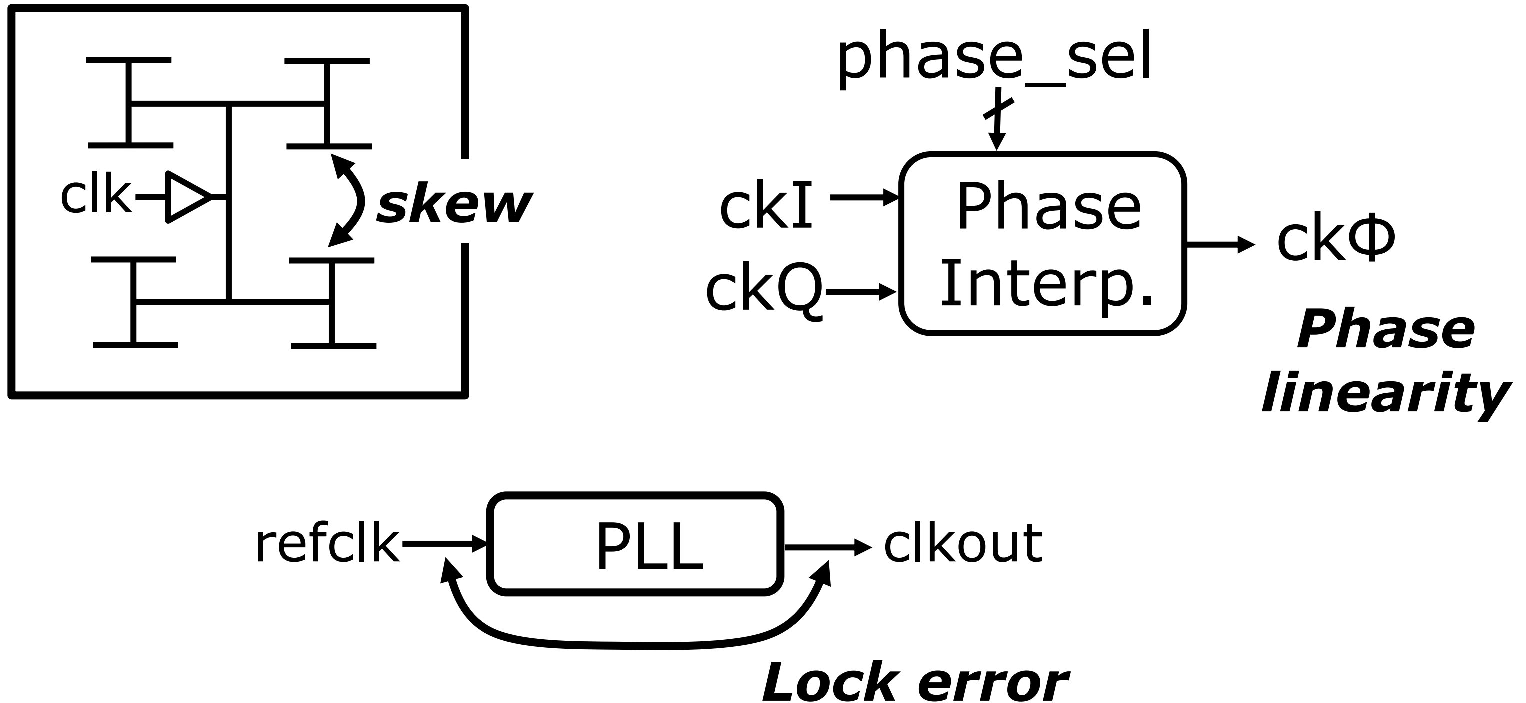
Outline

- Delay Measurement
- Power Supply Characterization
- I/O System Characterization

Outline

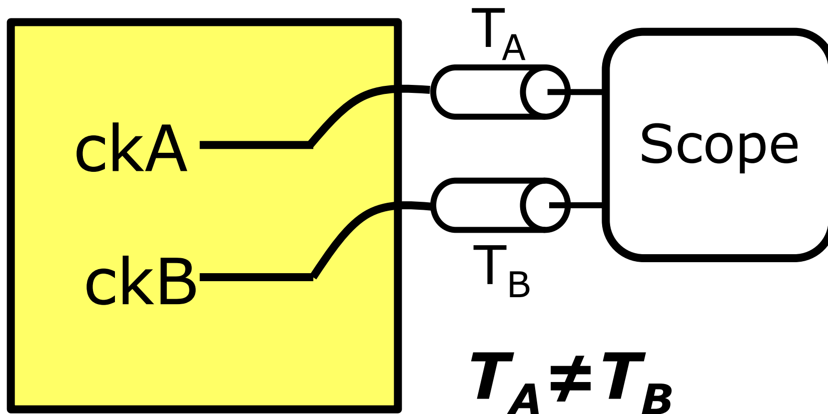
- **Delay Measurement**
  - Delay Metrics
  - Off-chip measurement limitations
  - On-Chip Phase Detector
  - Code Density Test (CDT)
- Power Supply Characterization
- I/O System Characterization

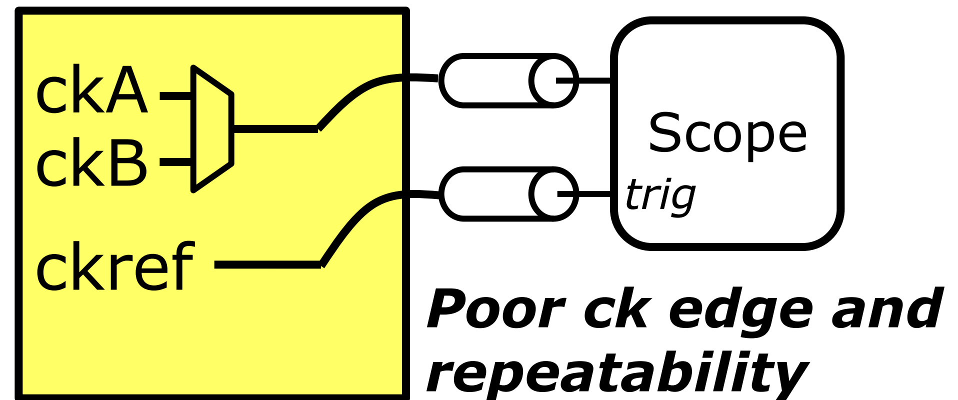
Delay/Skew Measurements



- Measuring the delay between two or more signals (often clocks) can be critical for circuit debug and characterization

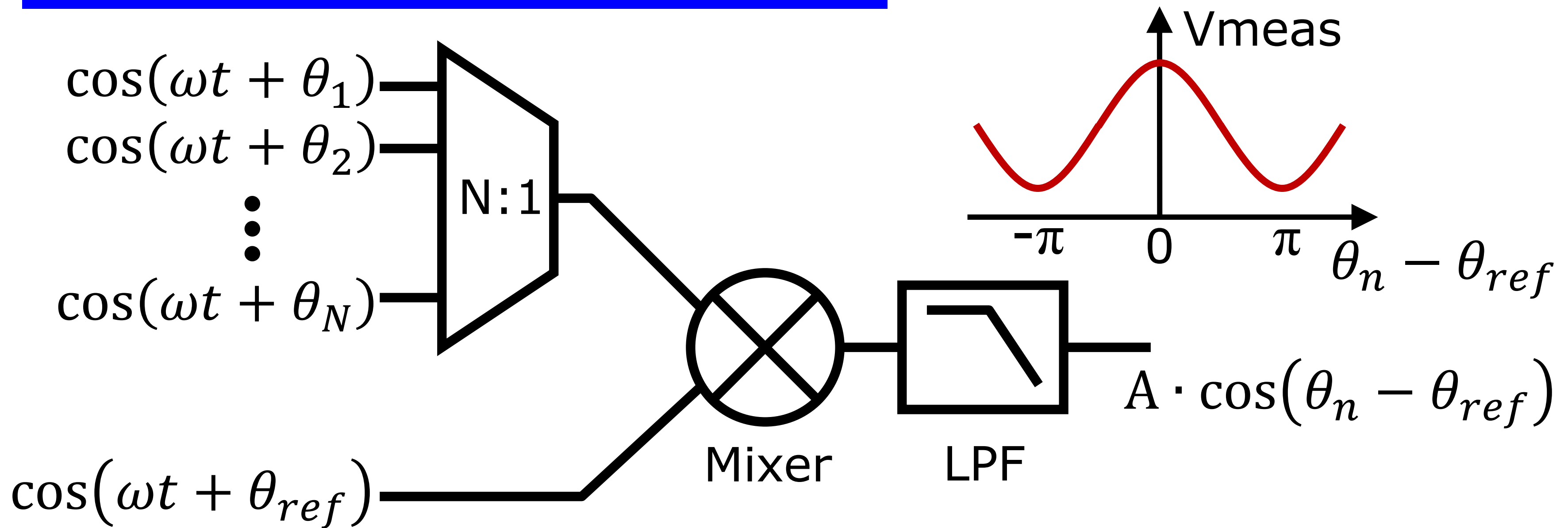
Off-Chip Clock Skew Measurement





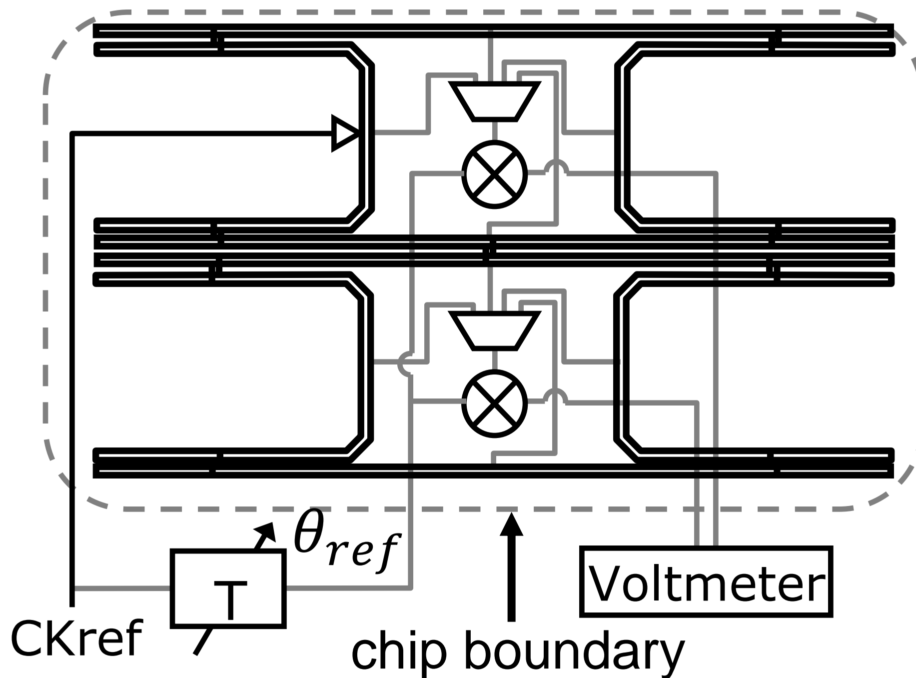
- External measurement limitations
  - Delay matching to equipment → delay error
  - Filtering for high-speed signals → delay error
    - V_{CM} and edge rate differences cause error
  - Delay stability → poor repeatability

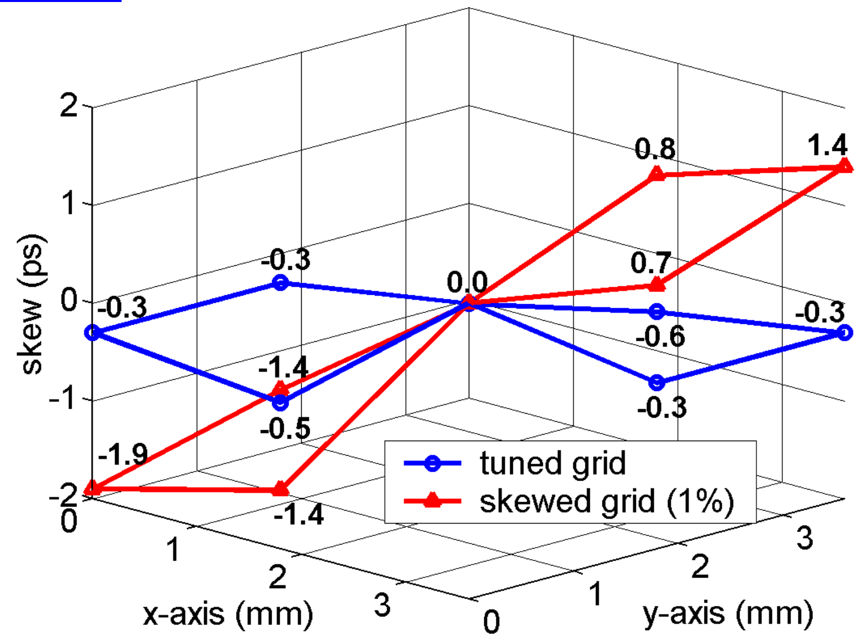
On-Chip Phase Detector



- Mix phase difference down to DC on chip
  - Other types of phase detectors can also work
- Measure DC component off- or on-chip
- Shared Mixer reduces mismatch. Still has MUX mismatch.
- Requires calibration for Voltage-to-Time constant (*A*)

Example: 10GHz Clock Skew Measurements

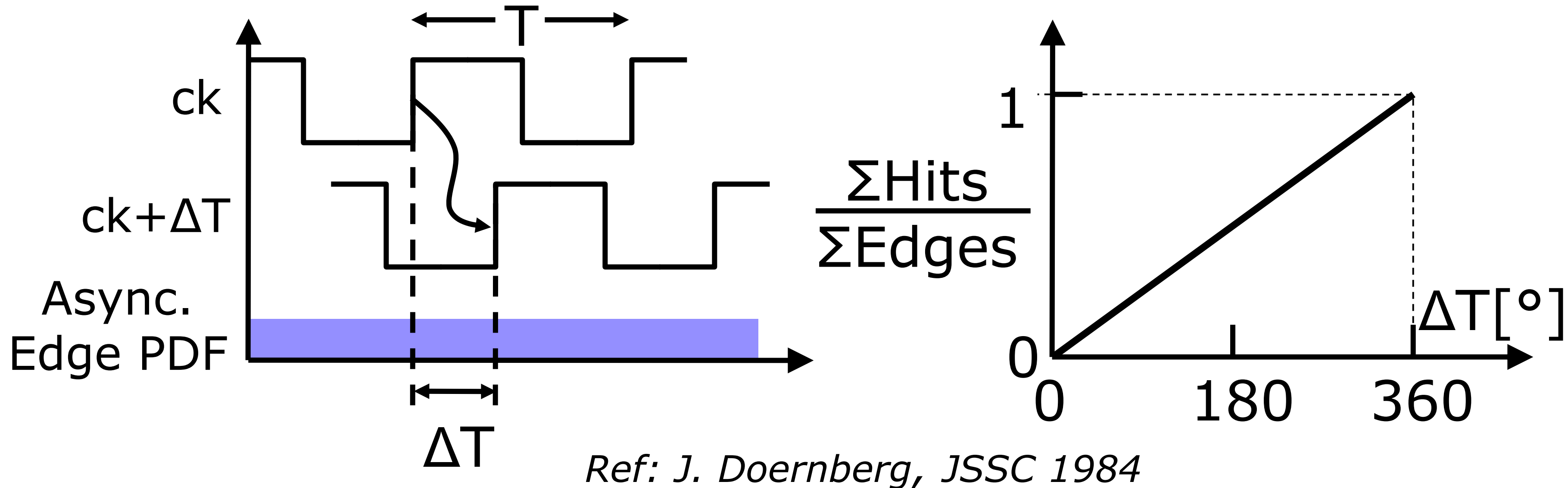




Ref: F. O'Mahony, ISSCC 2003

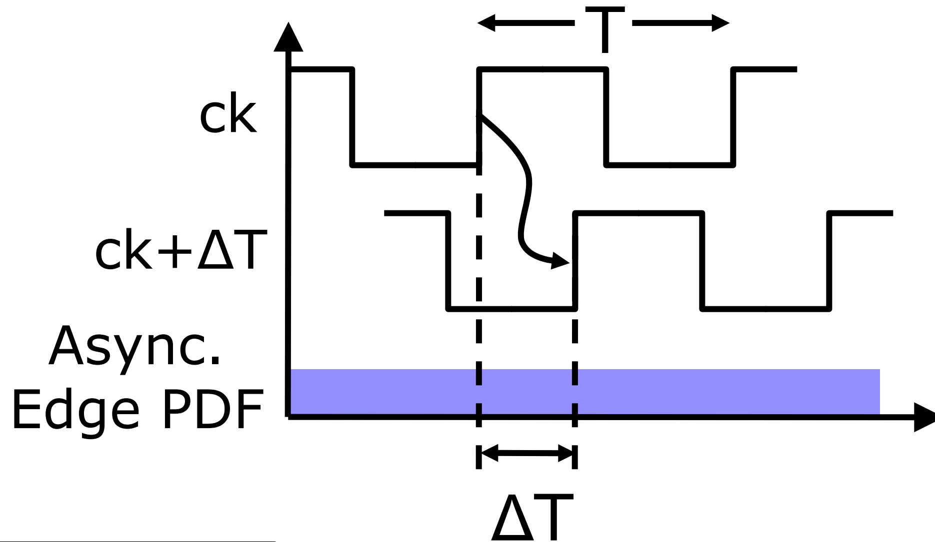
- Meas. resonant clock grid skew w/ sub-ps accuracy
- Minimize/match routing to phase detectors
- Measure externally with voltmeter
- Calibrate externally using adjustable delay line

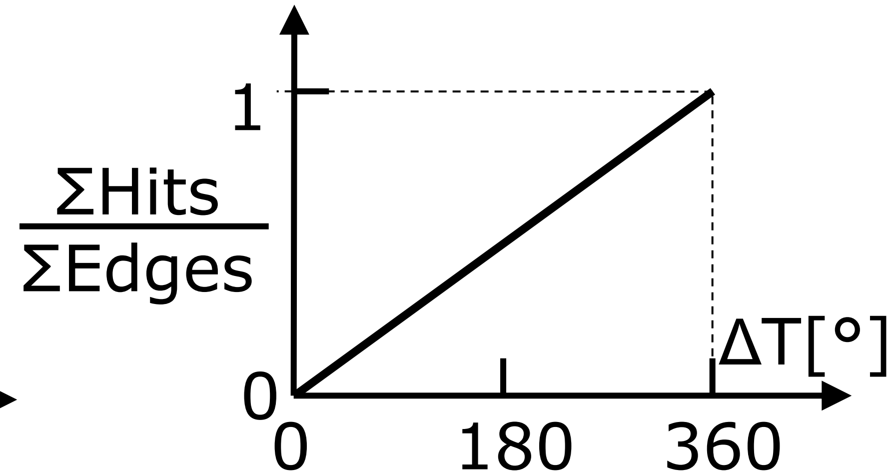
Code Density Test (CDT) Method

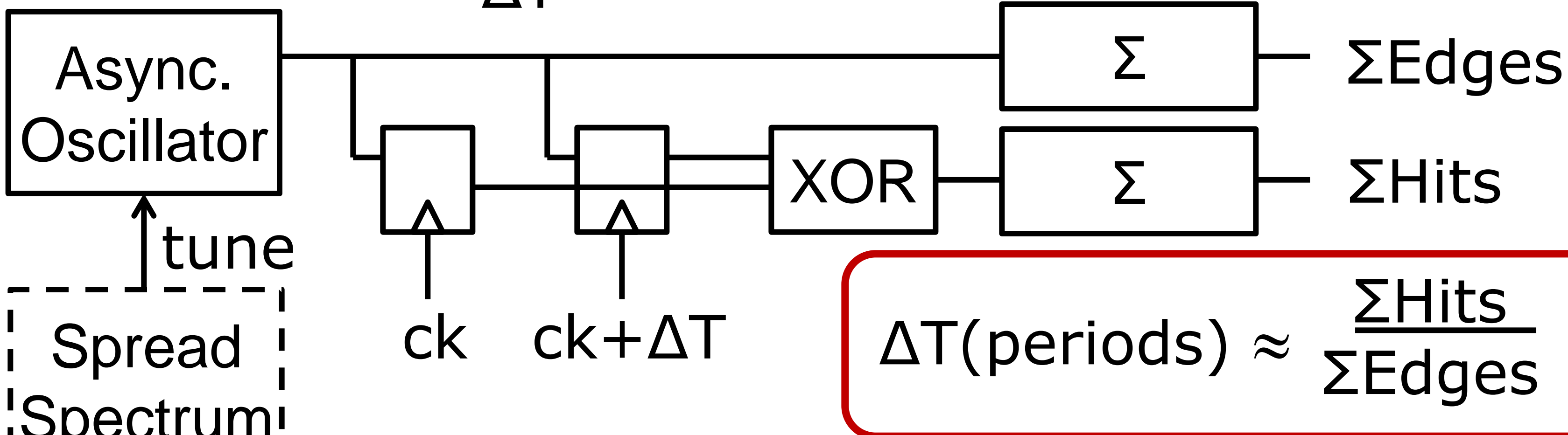


- Basic Idea: Count the # of Reference Edges that occur between two clock edges
- Likelihood of "Hit" is ΔT/T
- Asynchronous ring VCO provides uniform Edge PDF
  - Jitter and spread-spectrum improve the distribution

Code Density Test (CDT) Method



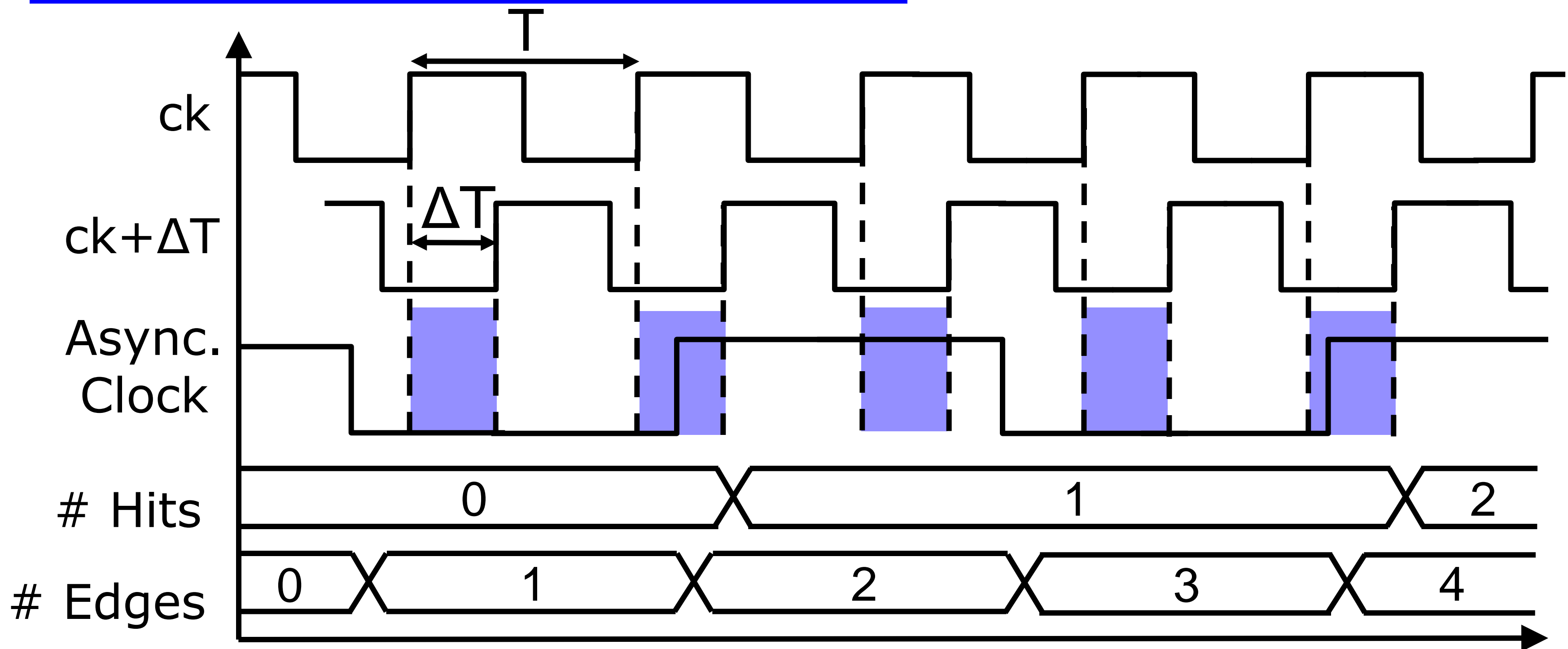




$$\Delta T(\text{periods}) \approx \frac{\Sigma \text{Hits}}{\Sigma \text{Edges}}$$

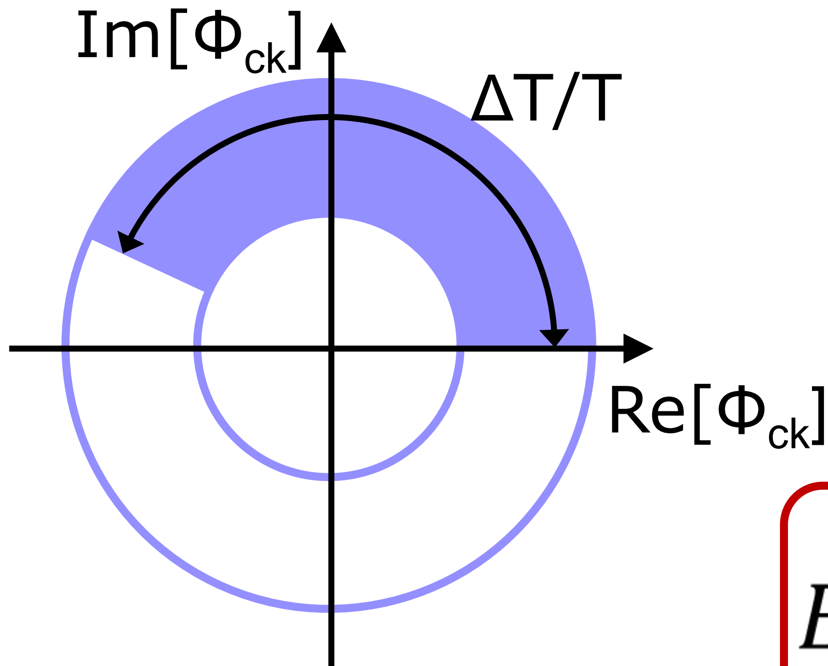
Ref: M. Mansuri, VLSIC, 2012

Time-Domain Circuit Operation



- Likelihood of "Hit" is ΔT/T
- Async. clock period must be >2·ΔT_{max}
  - A simple VCO frequency calibration ensures this
- Jitter helps by randomizing edge location

Delay Measurement Accuracy



$$\mu = np,\ \sigma^2 = np(1-p)$$

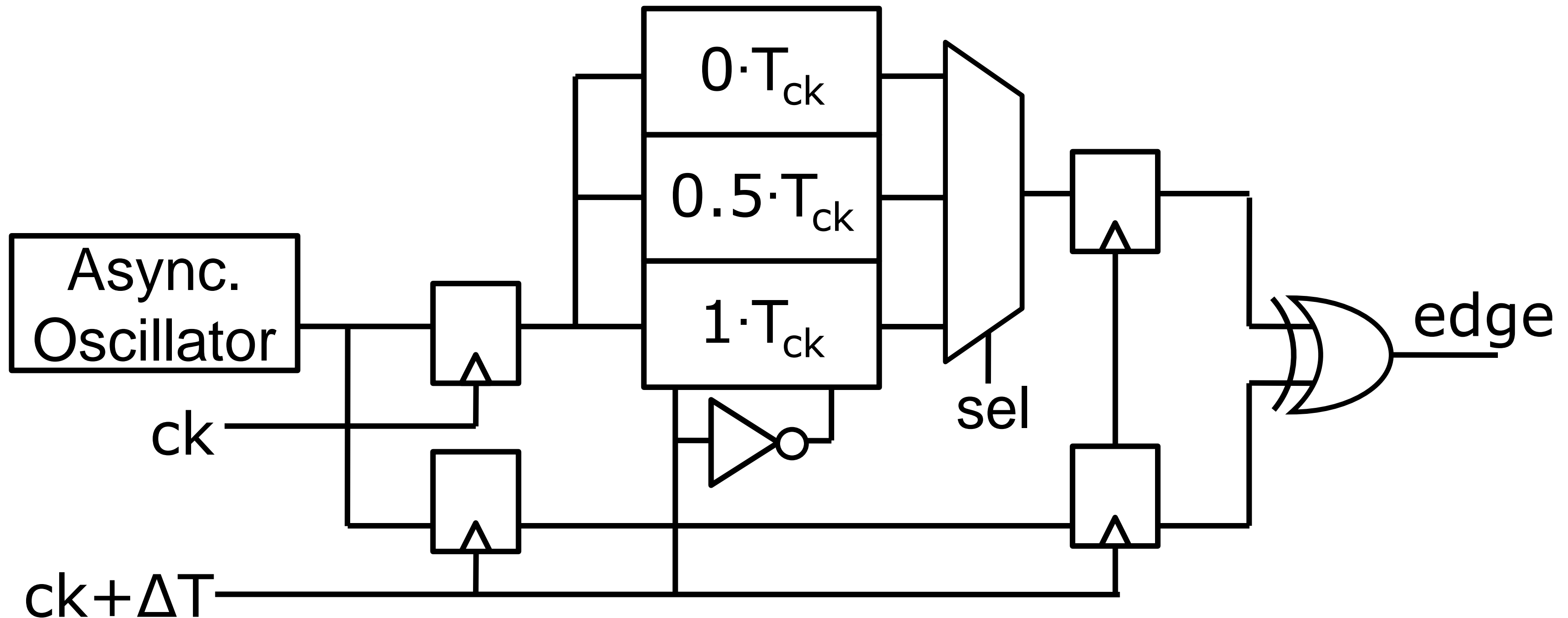
$$X = \Sigma Hits$$

$$p = \frac{\Delta T}{T},\ n = \Sigma Edges,$$

$$E\left[\frac{X}{n}\right] = p,\ \frac{\sigma}{n} = \left[\frac{p(1-p)}{n}\right]^{0.5}$$

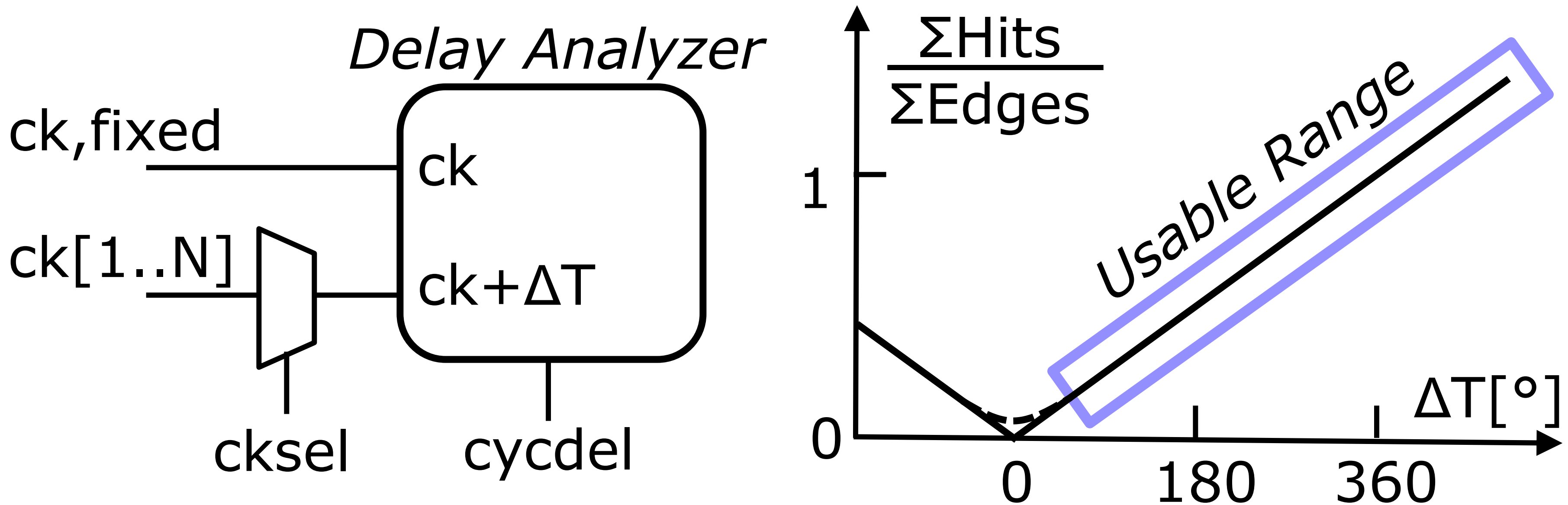
- Model w/ Binomial Distrib. (think “many coin flips”)
- Accuracy improves as $(1/\Sigma\mathrm{Edges})^{0.5}$
- Higher Resolution ↔ Longer measurement time

Synchronizer



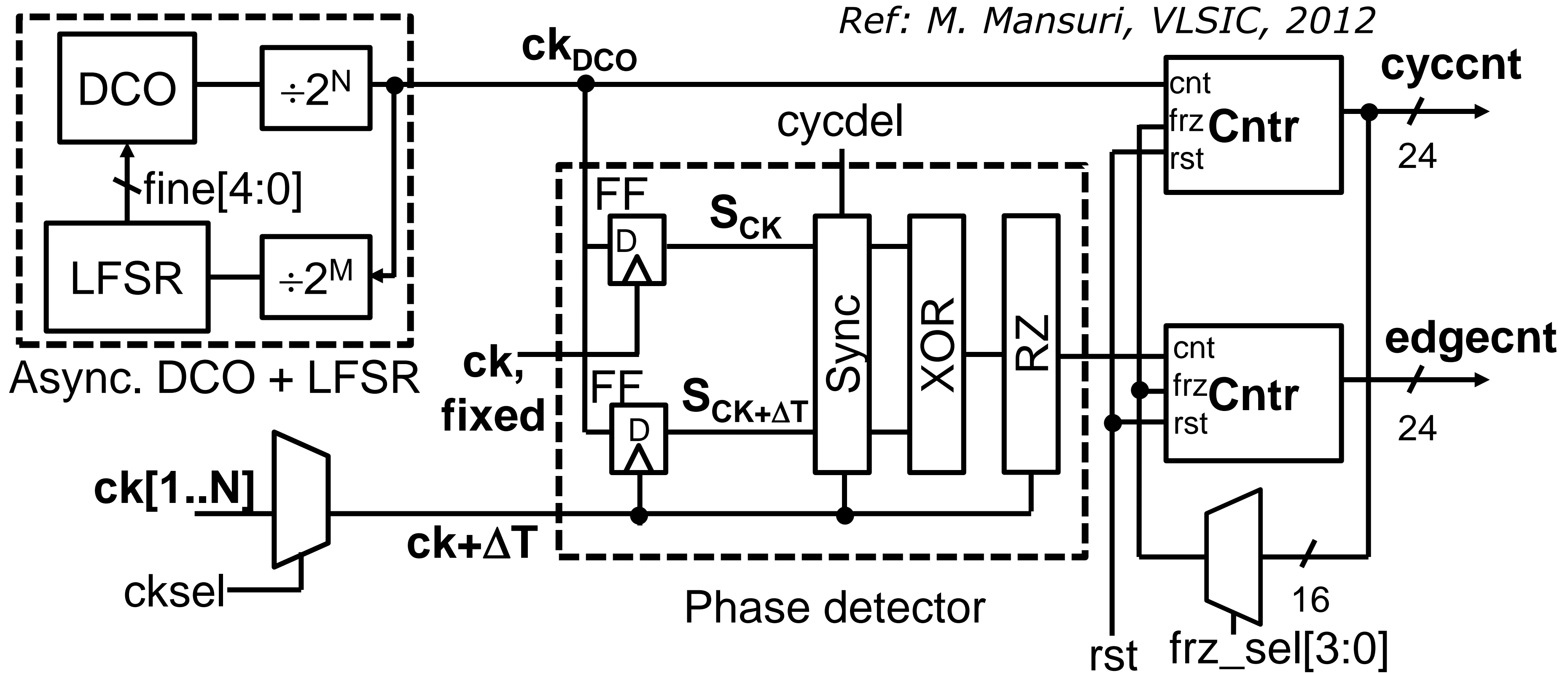
- Synchronizer aligns samples across full 360° range
- Clocks for $\Delta T = N \cdot T_{ck} + \Delta t$ are identical. Synchronizer adds programmable # of cycles of delay.

Delay Measurement Range



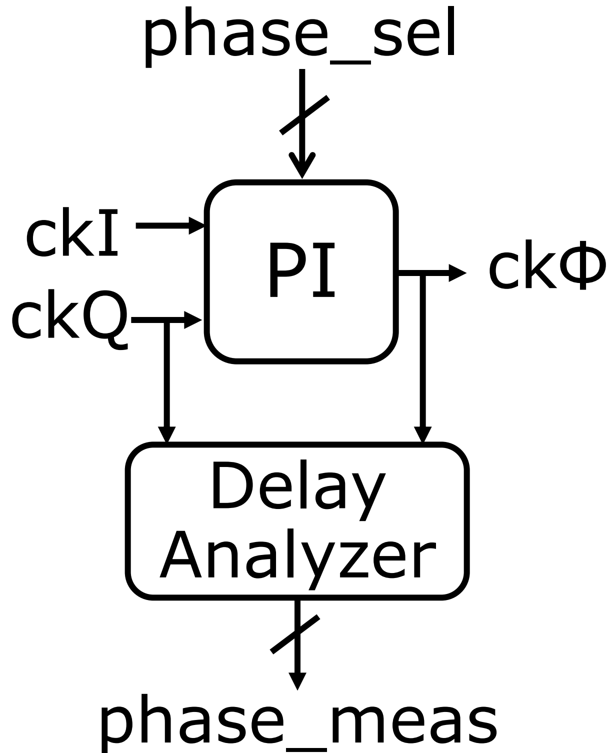
- Measure ck[1..N] relative to ck,fixed
  - ck[1..N] are all later than ck,fixed
  - Removes circuit mismatch (e.g. FF’s) except Mux
  - Use *cycdel* to select which edges to compare
  - Synchronizer extends range to >360°

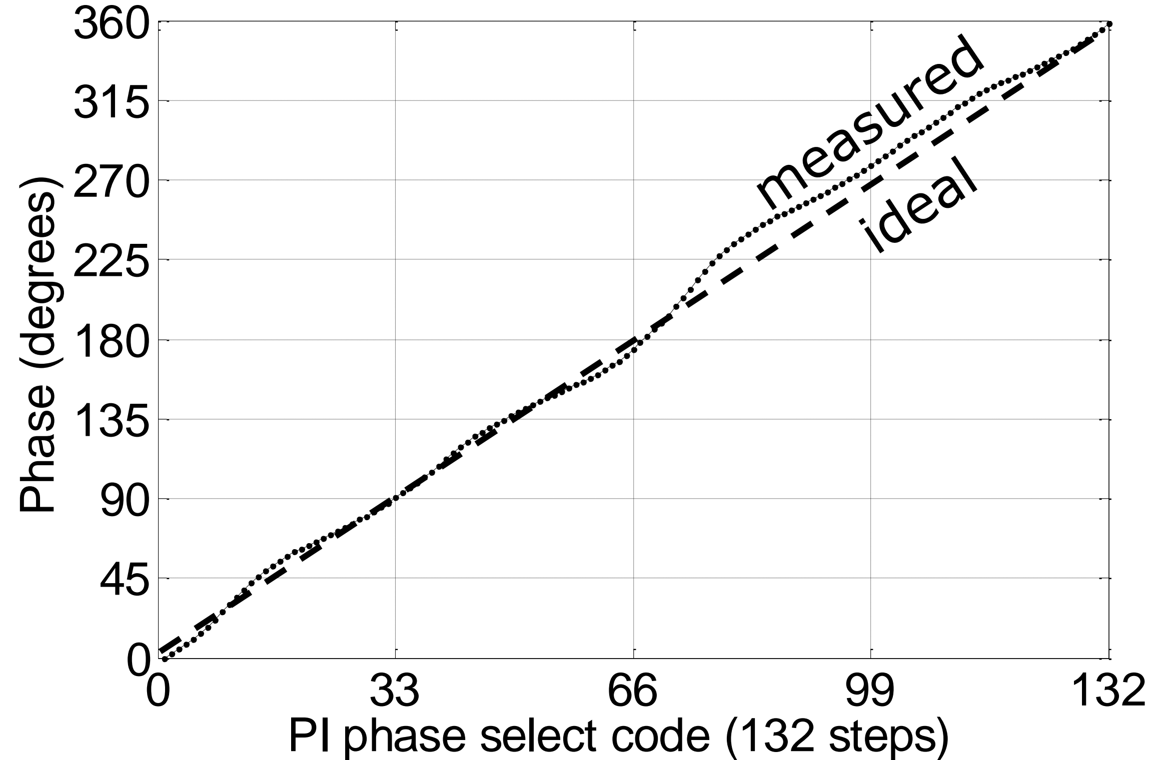
Detailed Circuit Implementation



- Entirely digital implementation
- Counter depth depends on required accuracy

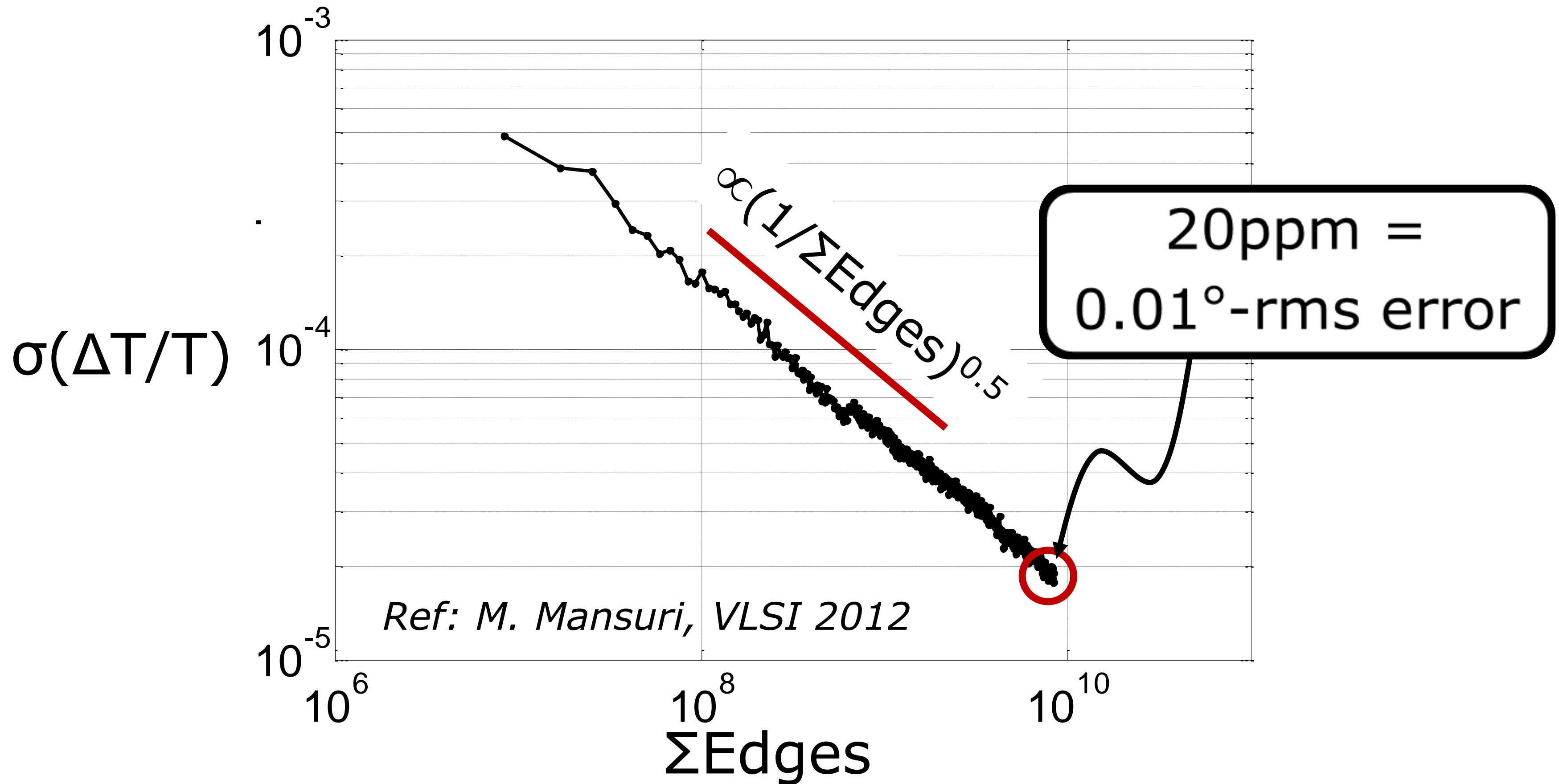
Measured Phase Interpolator (PI) Linearity





- Fully on-die measurement of quadrature PI w/ CDT
- Phase transfer function provides INL/DNL

Measured Phase Error – Repeatability



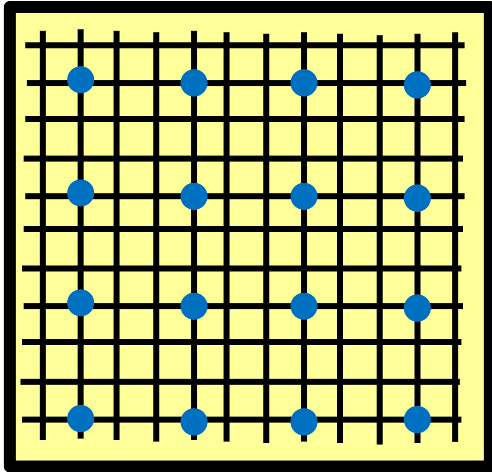
- Measurement error reduces as $(1/\Sigma \text{Edges})^{0.5}$

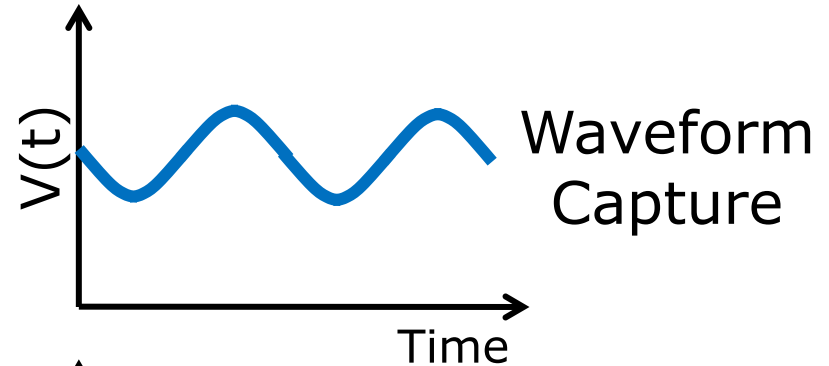
Outline

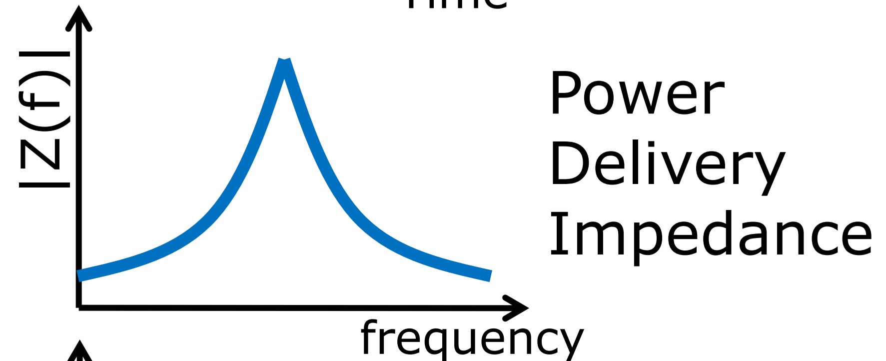
- Delay Measurement
- **Power Supply Characterization**
  - Power Supply metrics
  - Off-chip measurement limitations
  - Real vs. Equivalent time measurement
  - Supply noise waveform
  - Supply impedance
  - Supply noise spectrum
- I/O System Characterization

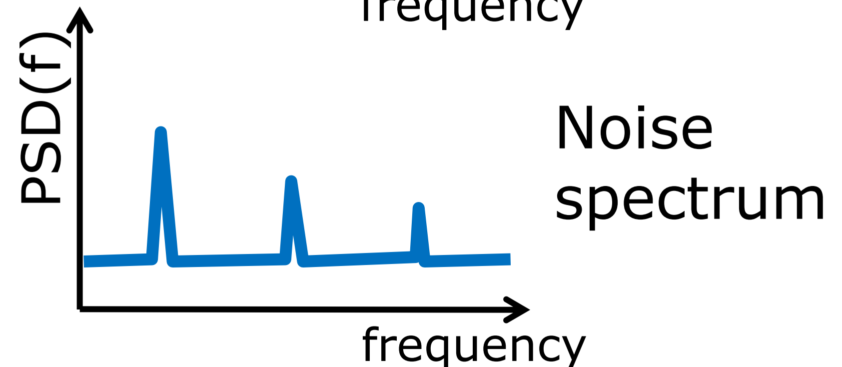
Power Supply Metrics

Power Supply Grid on Die





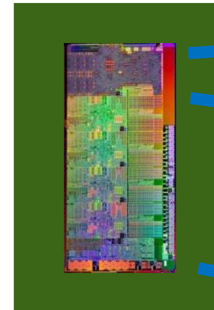




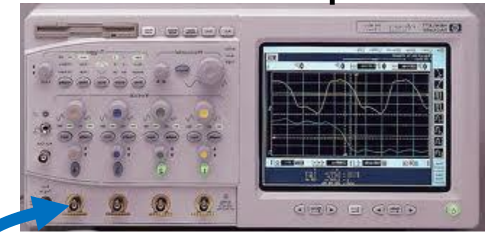
- Used to design, model and debug the chip
- Examples:
  - Quantify Vcc droop → V(t)
  - Verify Grid model → Z(f)
  - Find aggressors → PSD(f)

External Power Supply Measurements

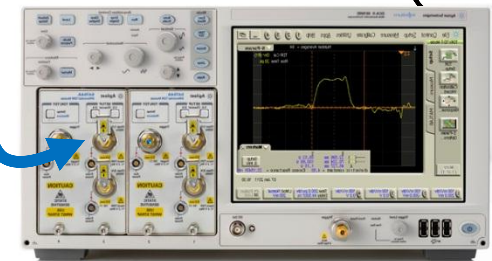
- Packages commonly have supply probes
- Off-chip measurement limitations
  - External probing loads the power supply
  - Probe measurements are not local
  - Limited # of probe points due to pkg routing
  - Package filters the supply measurements



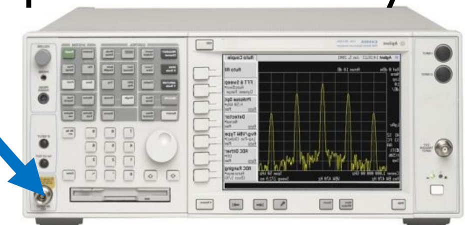
Oscilloscope



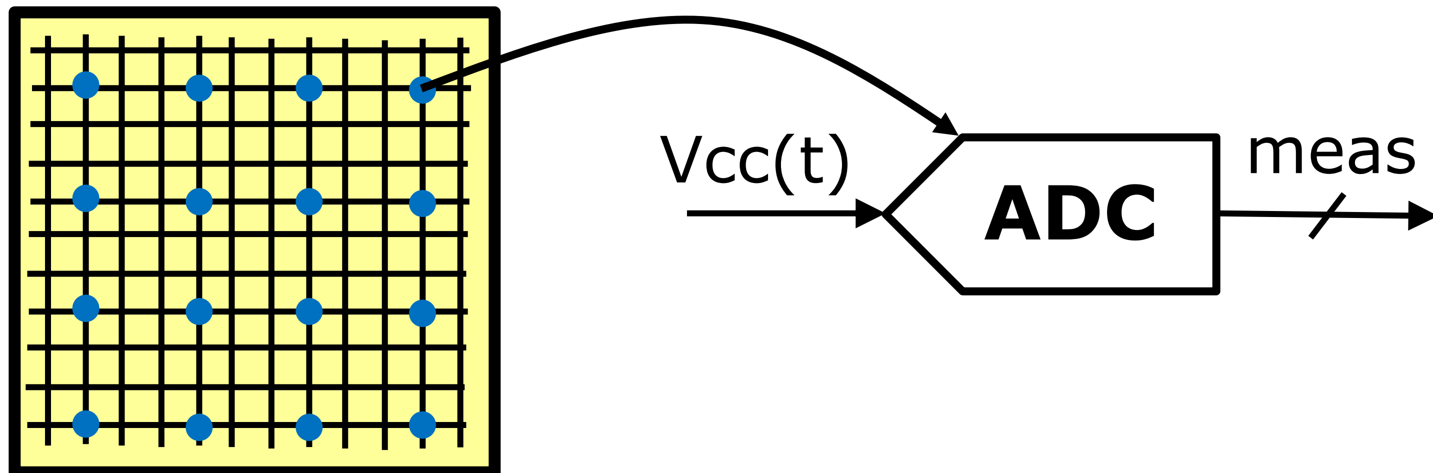
Time-Domain Reflectometer (TDR)



Spectrum Analyzer

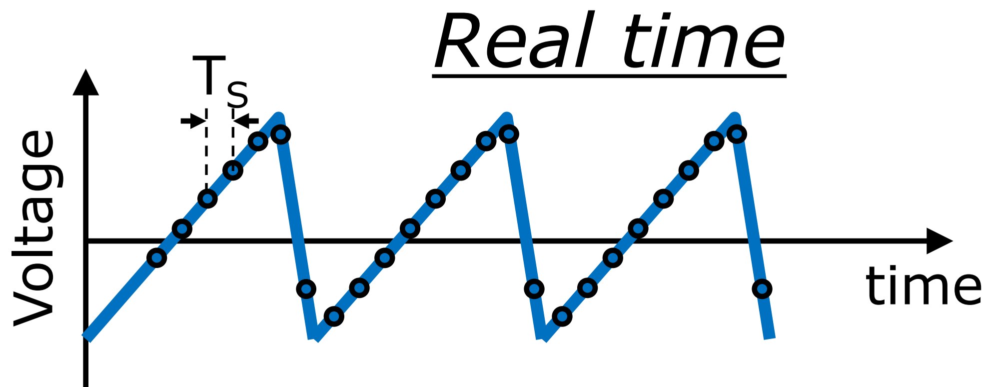


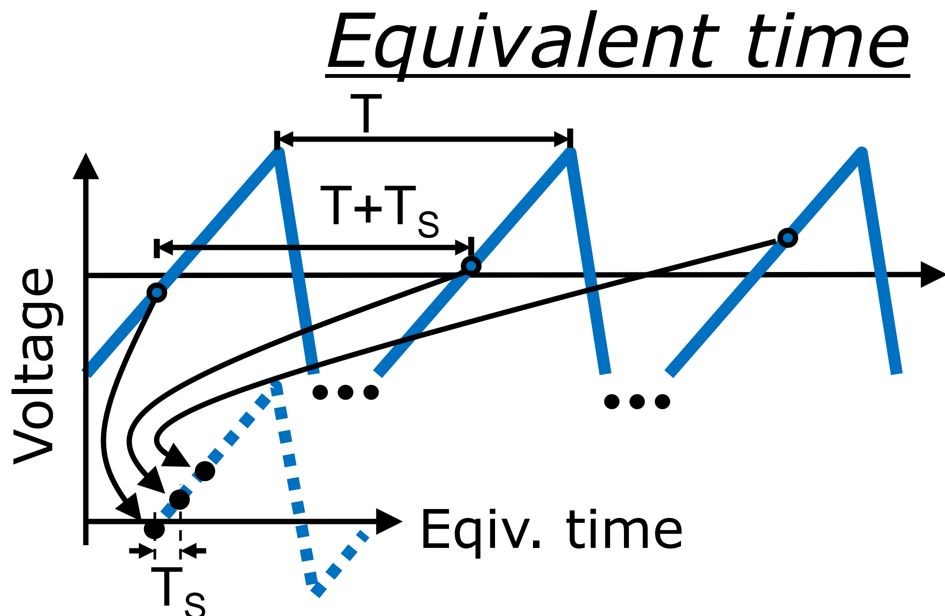
On-Die High-Speed ADC



- Ideally embed local ADCs to digitize these metrics
- High resolution (10+ bits) and BW (>1GHz) presents a significant implementation challenge

Real vs. Equivalent-Time Measurement

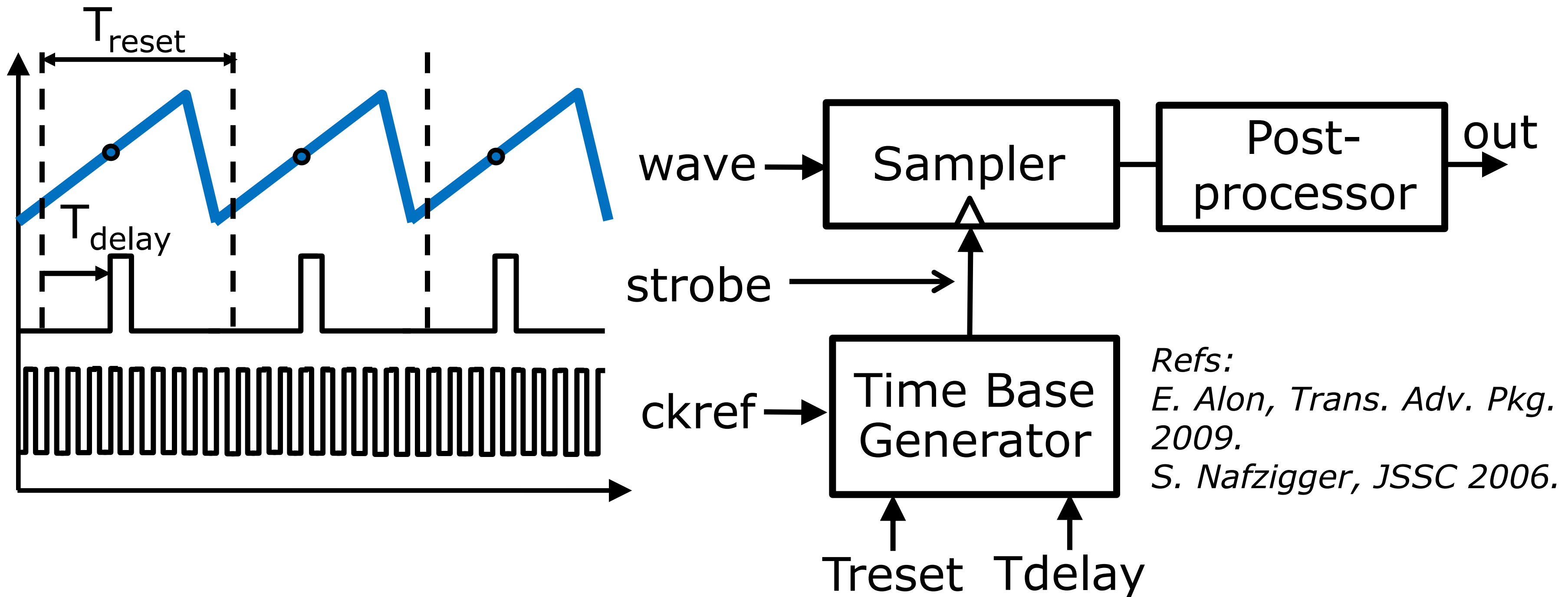




- ☺ One-shot meas.
- ☺ Most complete info
  - Time, spectral
- ☹ Limited by ADC f_{samp}, resolution

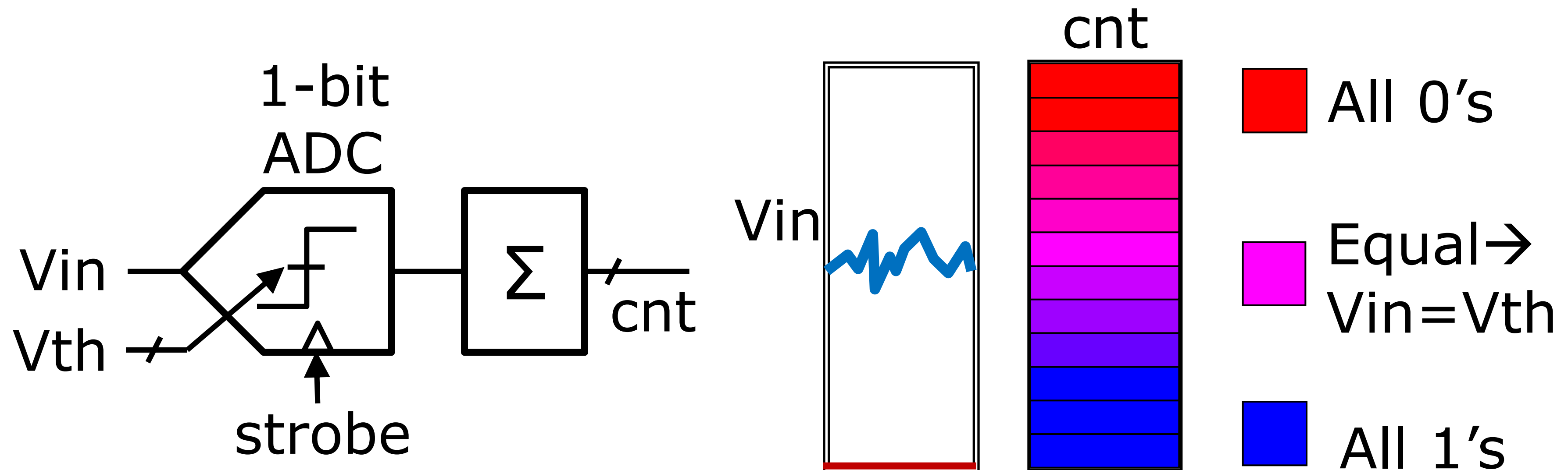
- 😐 Periodic waveforms
- 😐 No spectral info.
- ☺ Effective BW and resolution not limited by ADC

Equivalent-Time Measurement



- Time Base Generator (TBG) provides strobe
- Sweeps strobe position in equivalent time
- Sampler output is postprocessed (e.g. averaged)

Sampler Option #1: 1-bit Comparators



- Programmable threshold →Voltage CDF/PDF
- Center of this PDF is the Average Voltage (***μ***)
- CDF/PDF also captures Voltage Noise(e.g. **σ**)
  - …along with comparator noise and strobe jitter
  - Extract fit to distribution (normal, uniform, sinusoid)

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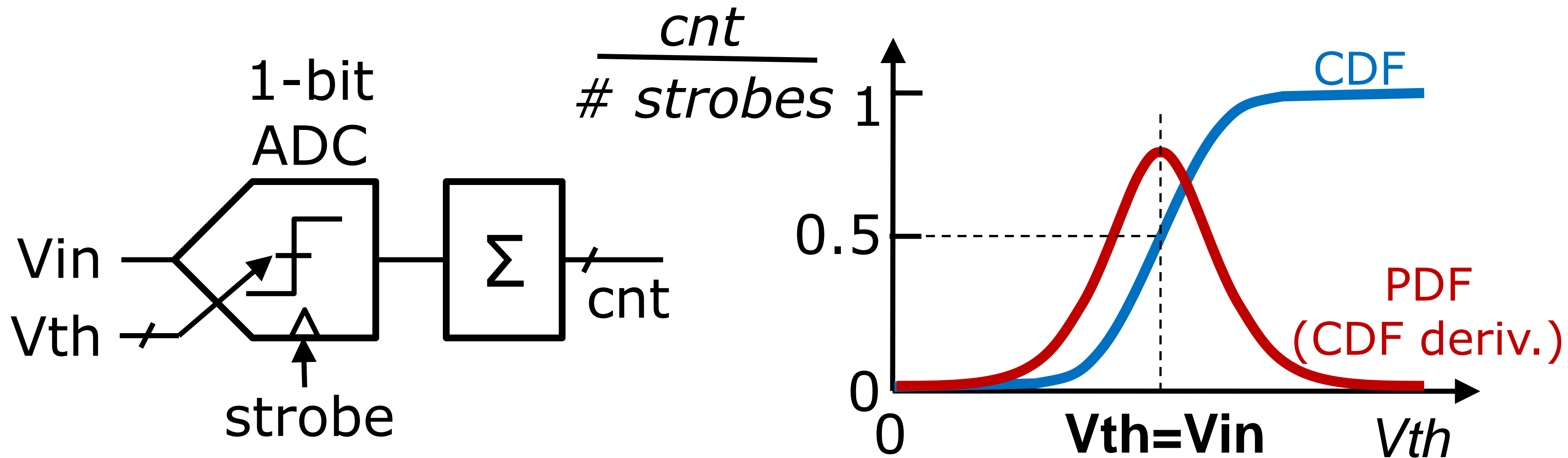

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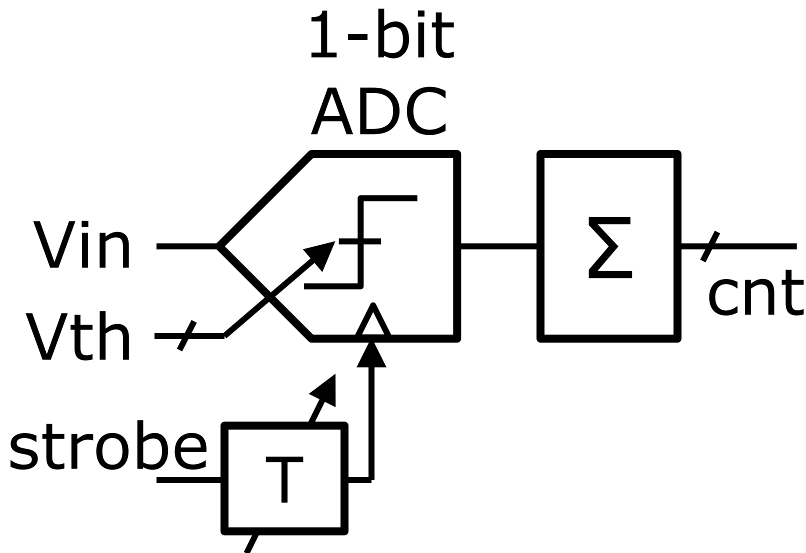
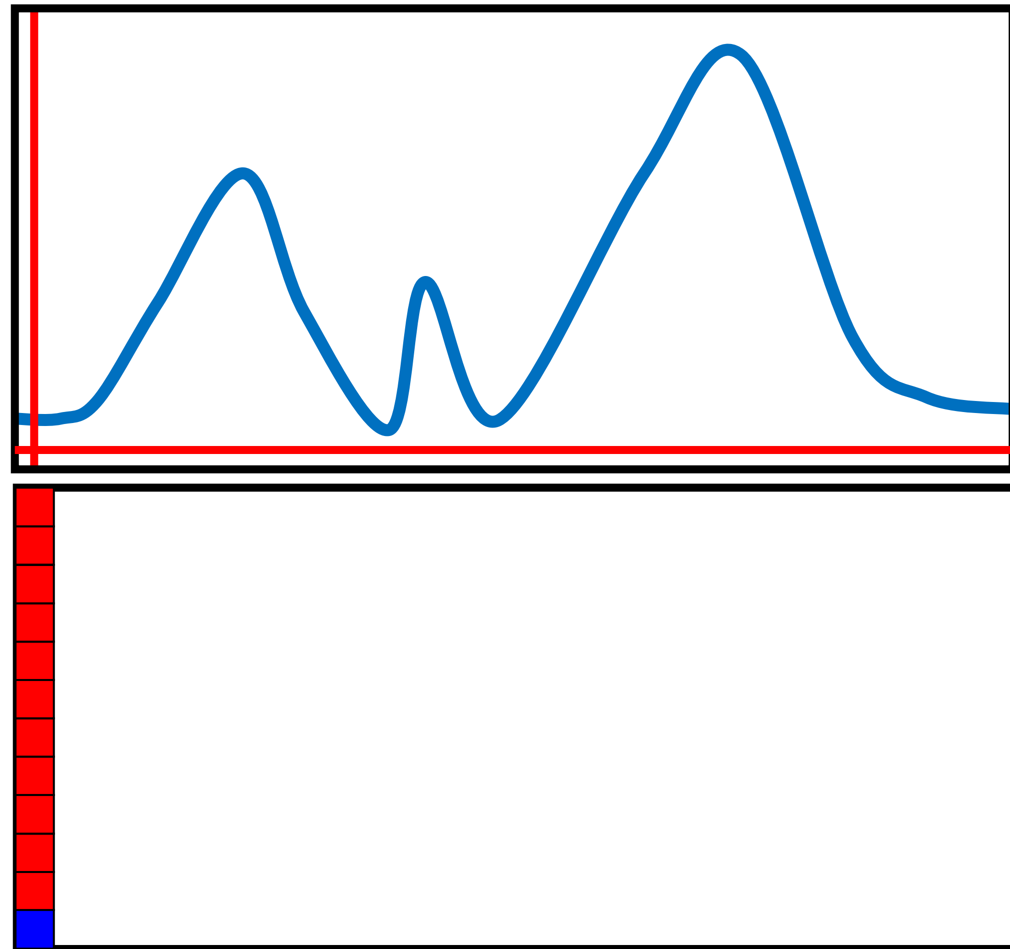
Waveform Capture w/ 1-bit Comp.



- Combine 1-bit ADC with Equivalent-Time sampling to get full Waveform Capture

Ref. K. Soumyanath, JSSC 1999.



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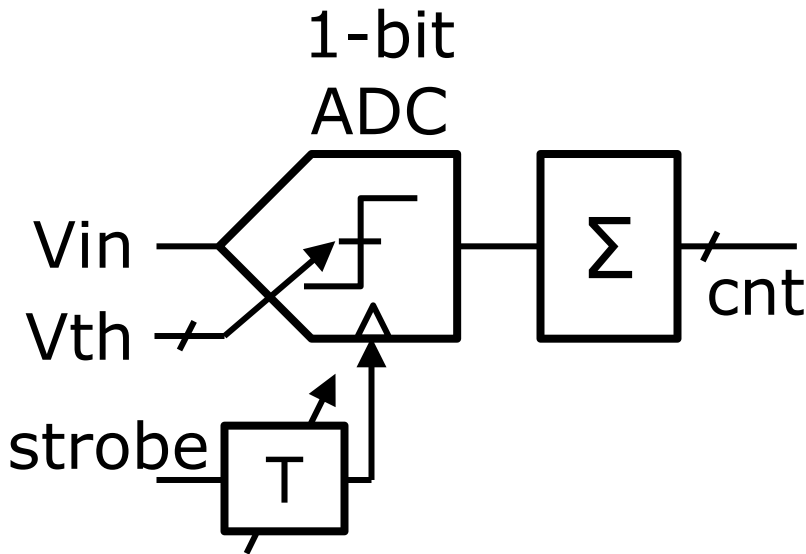

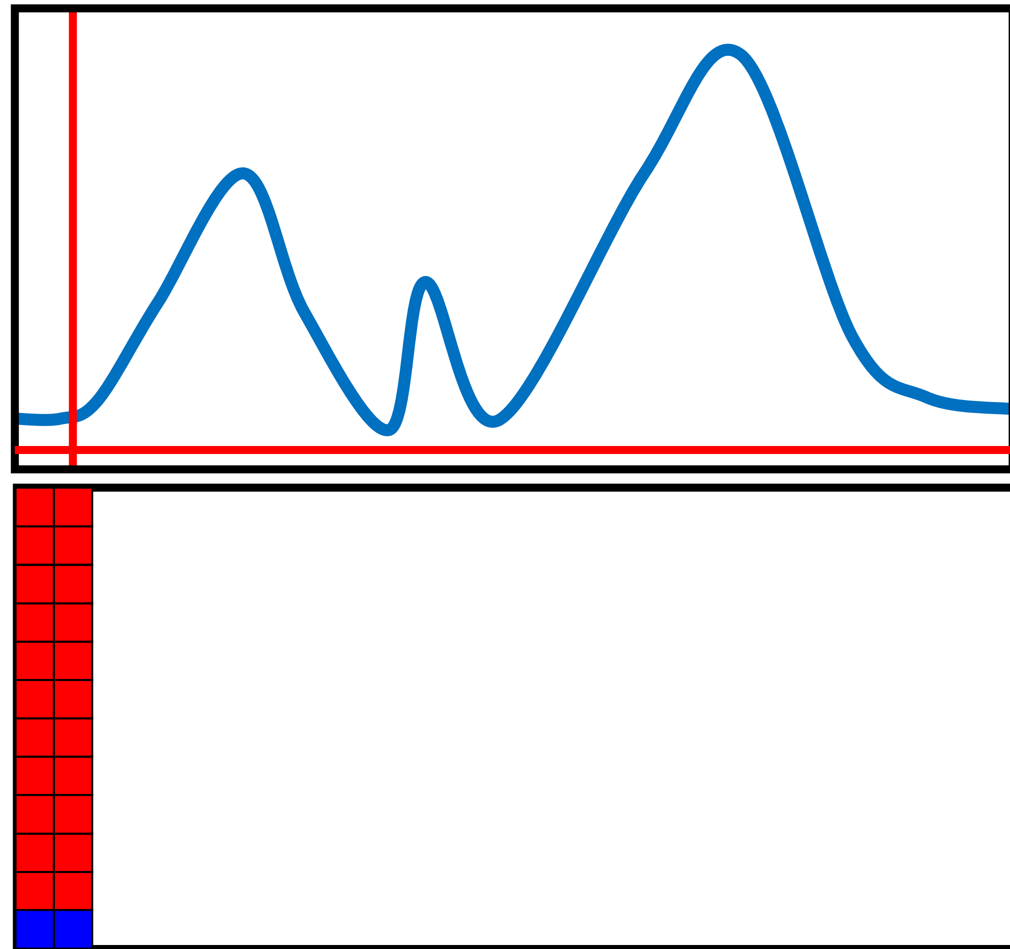

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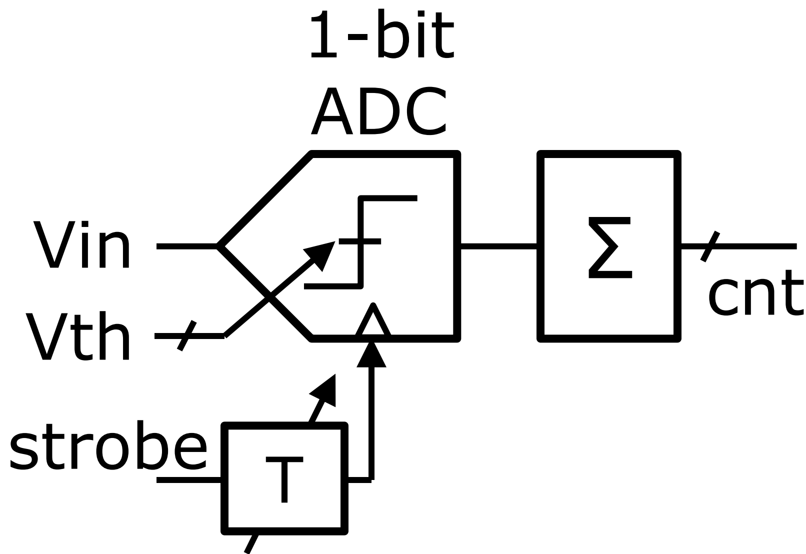

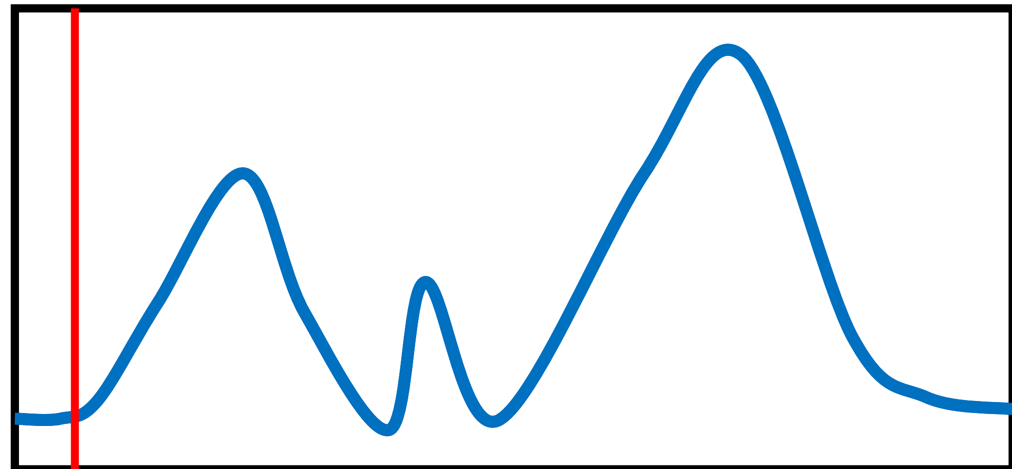

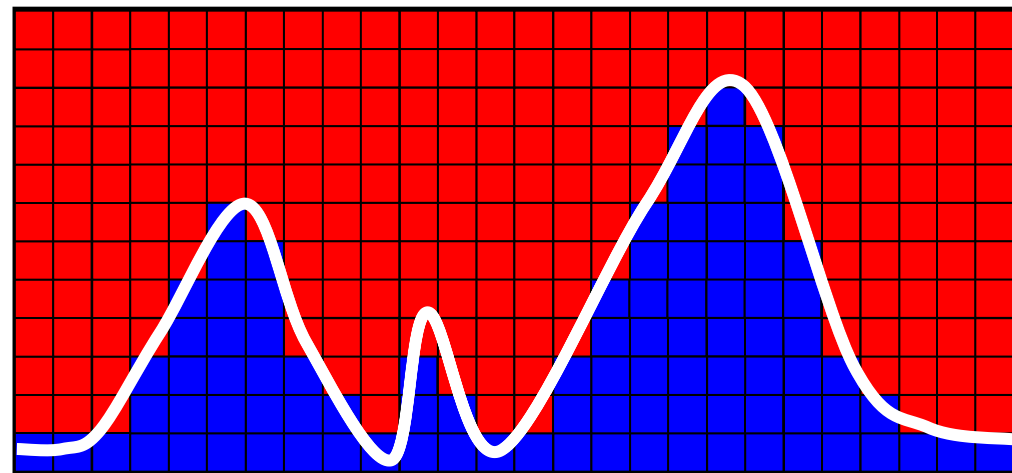

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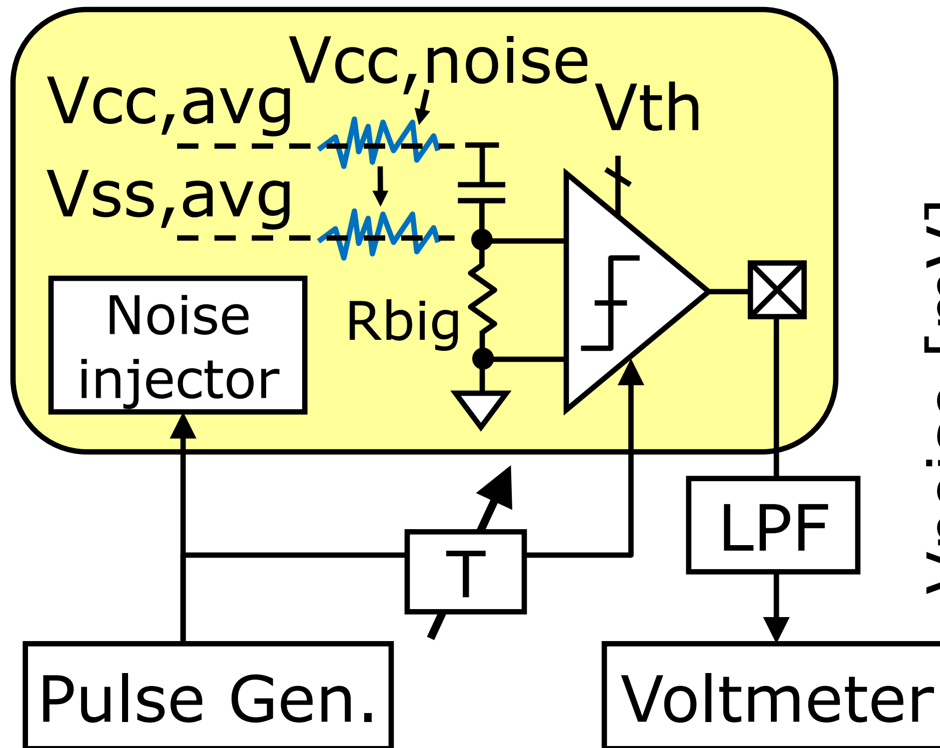
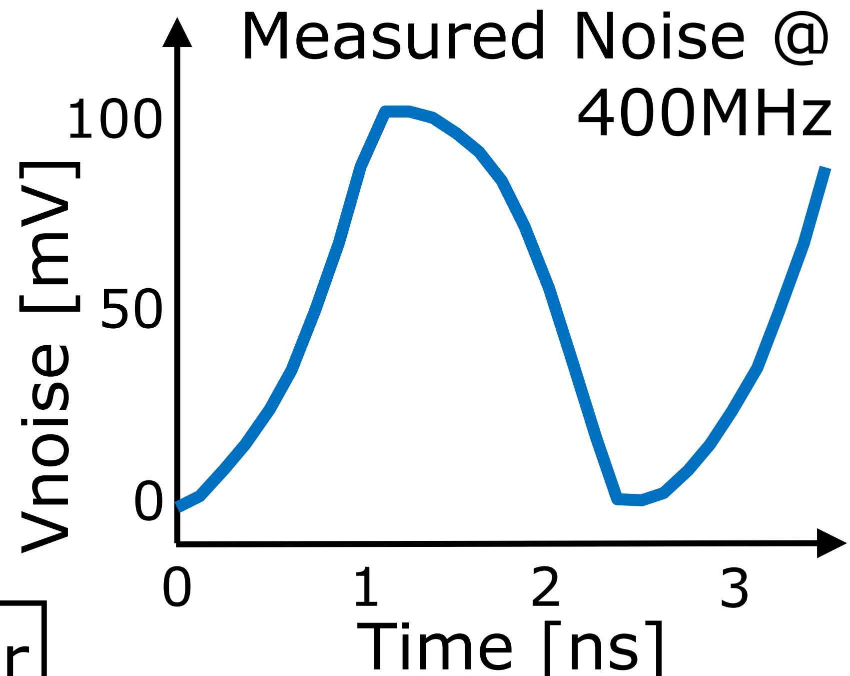
Example: Simple Power Supply Measurement

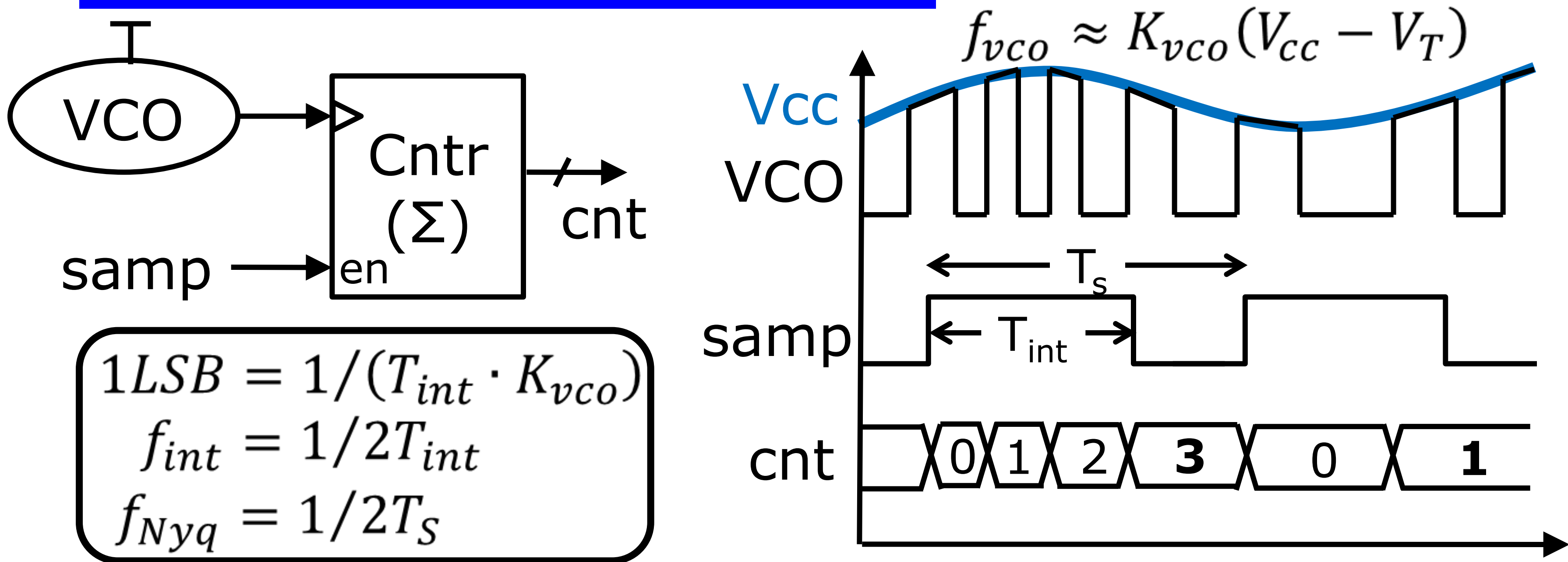




Ref: F. O'Mahony, VLSIC 2006

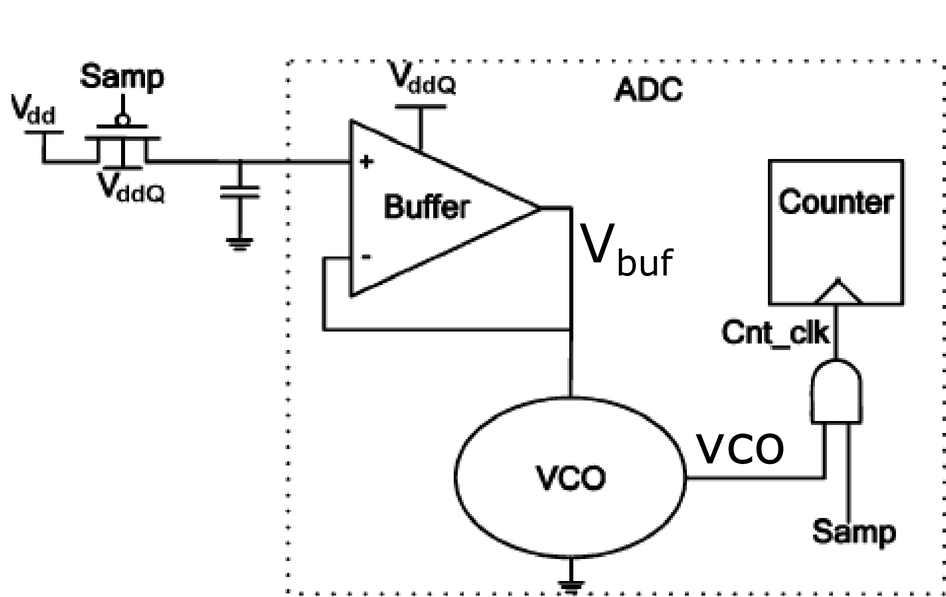
- Re-used RX sampler from to sample Vcc,noise
- AC couple Vcc,noise sets correct common mode for sampler
  - Limits measurement to freq > RC
- Simplest TBG – strobe is the delayed noise signal

Sampler Option #2: VCO-based ADC

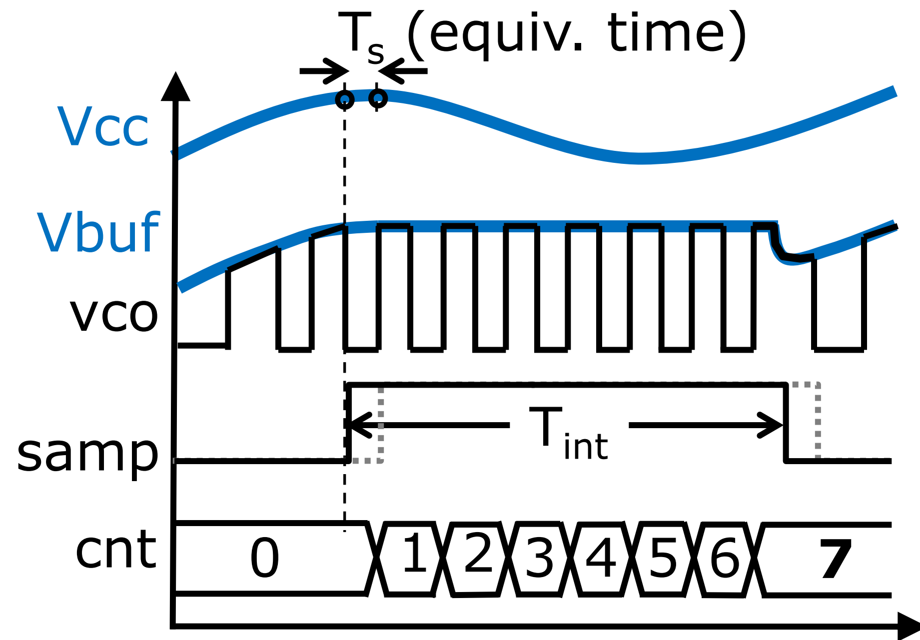


- Idea #1: Count Async. VCO edges during fixed ΔT
  - Pro: Directly attach VCO to power supply, real- or equivalent-time meas.
  - Con: Quant. error trades off with f_{int} and f_{Nyq}
- *This is a variation of the Code Density Test!*

Sampler Option #2: VCO-based ADC



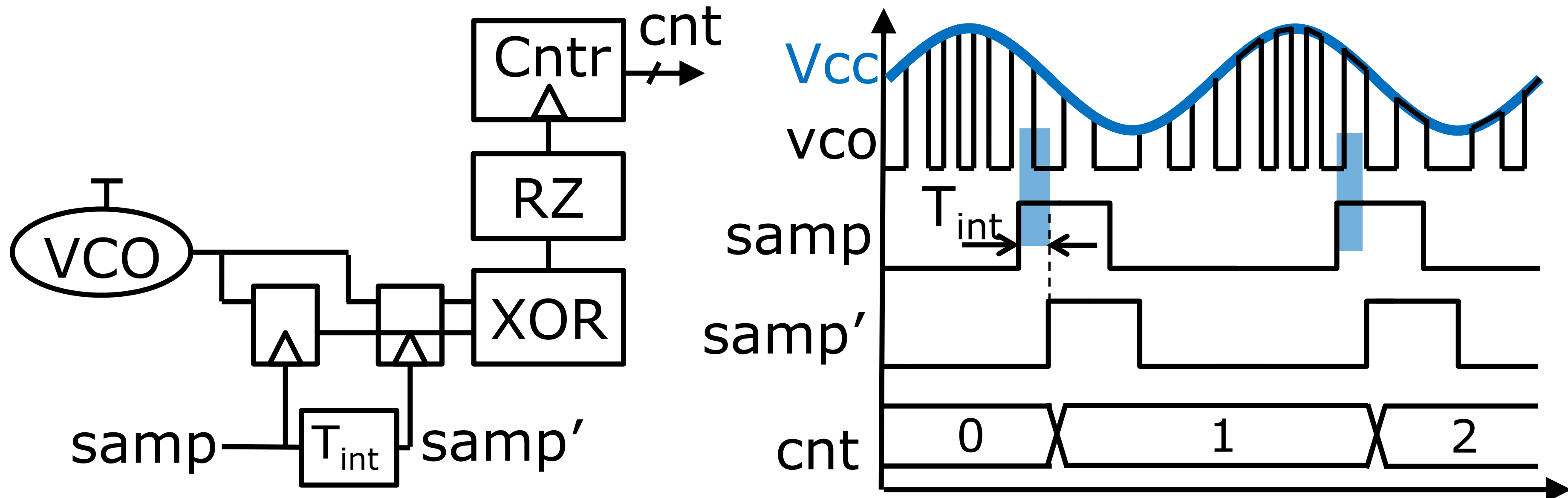
Ref: E. Alon, VLSIC 2004



- Idea #2: Sample-and-Hold the supply voltage
  - Pro: Quantization error is independent of f_{int} and f_{Nyq}*
  - Con: S/H leakage, Supply voltage buffer, Equivalent-Time measurement only (or else f_{Nyq} degrades)

**Note: This is the Equivalent-Time Nyquist frequency*

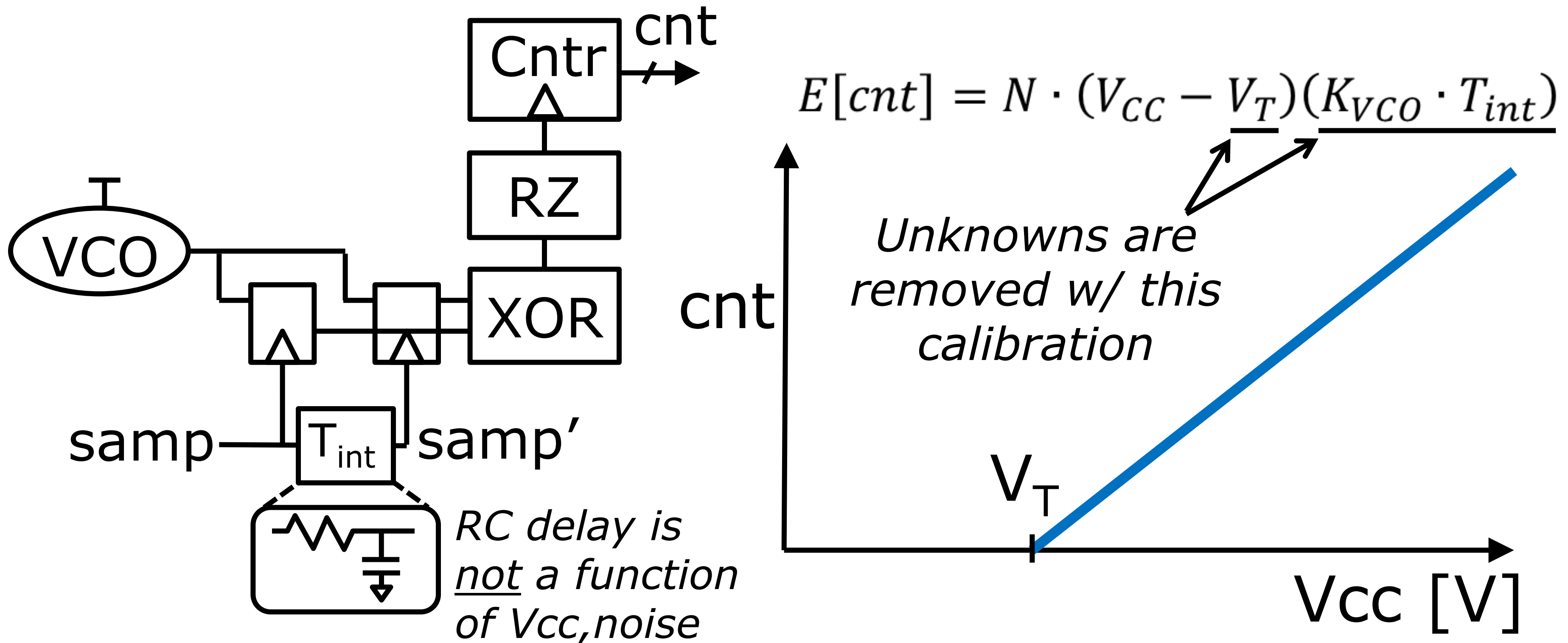
Sampler Option #2: VCO-based ADC



Ref: V. Abramzon, E. Alon, ESSCIRC 2005

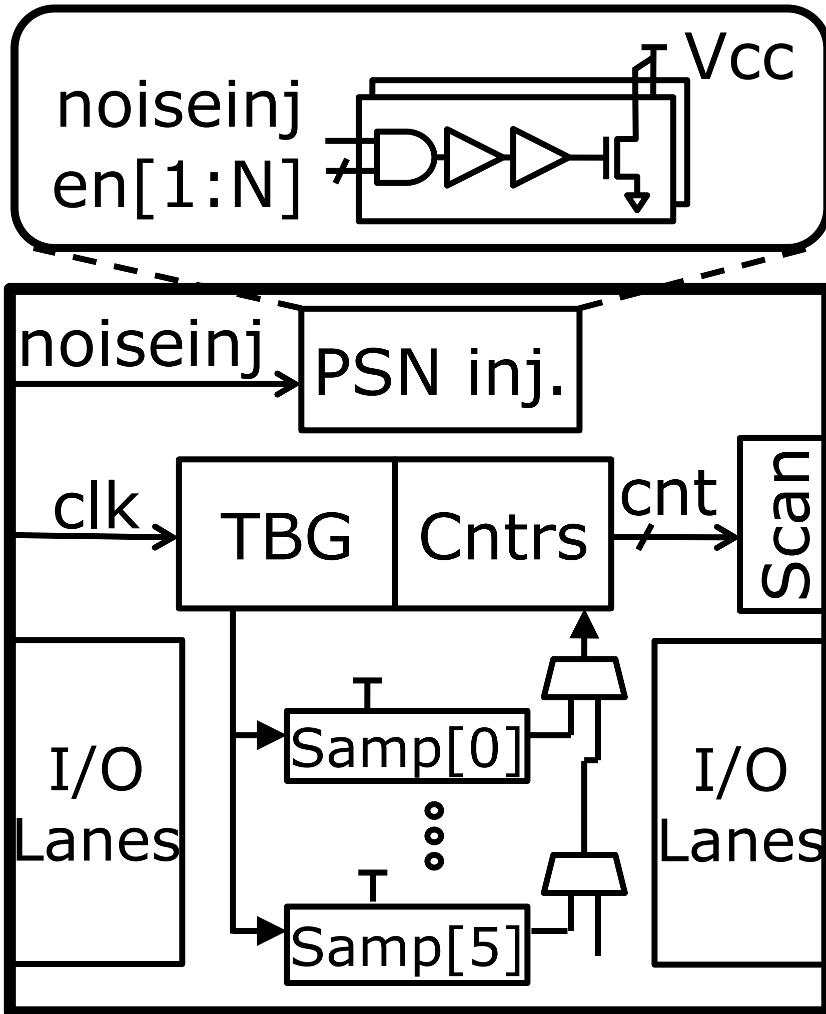
- Idea #3: Very short aperture with averaging
  - Pro: Quantization error independent of f_{int} and f_{Nyq}. Directly connect VCO to power supply. No sampling switch. Very short T_{int}, set by passive RC and calibrated.
  - Con: Not capable of real-time measurement, increased measurement time

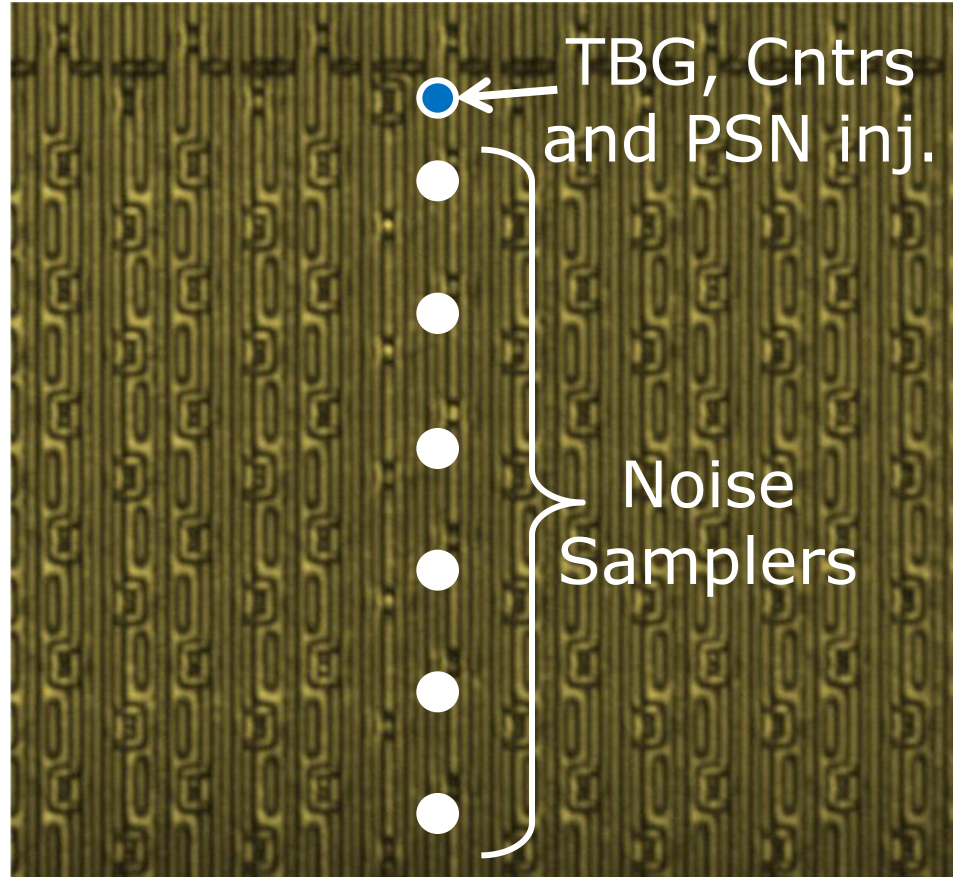
Sampler Calibration



- Map *Vcc→cnt* with DC sweep of Vcc
- Can be approximated as linear fit
- Avoid operating close to V_T - Variation/Linearity

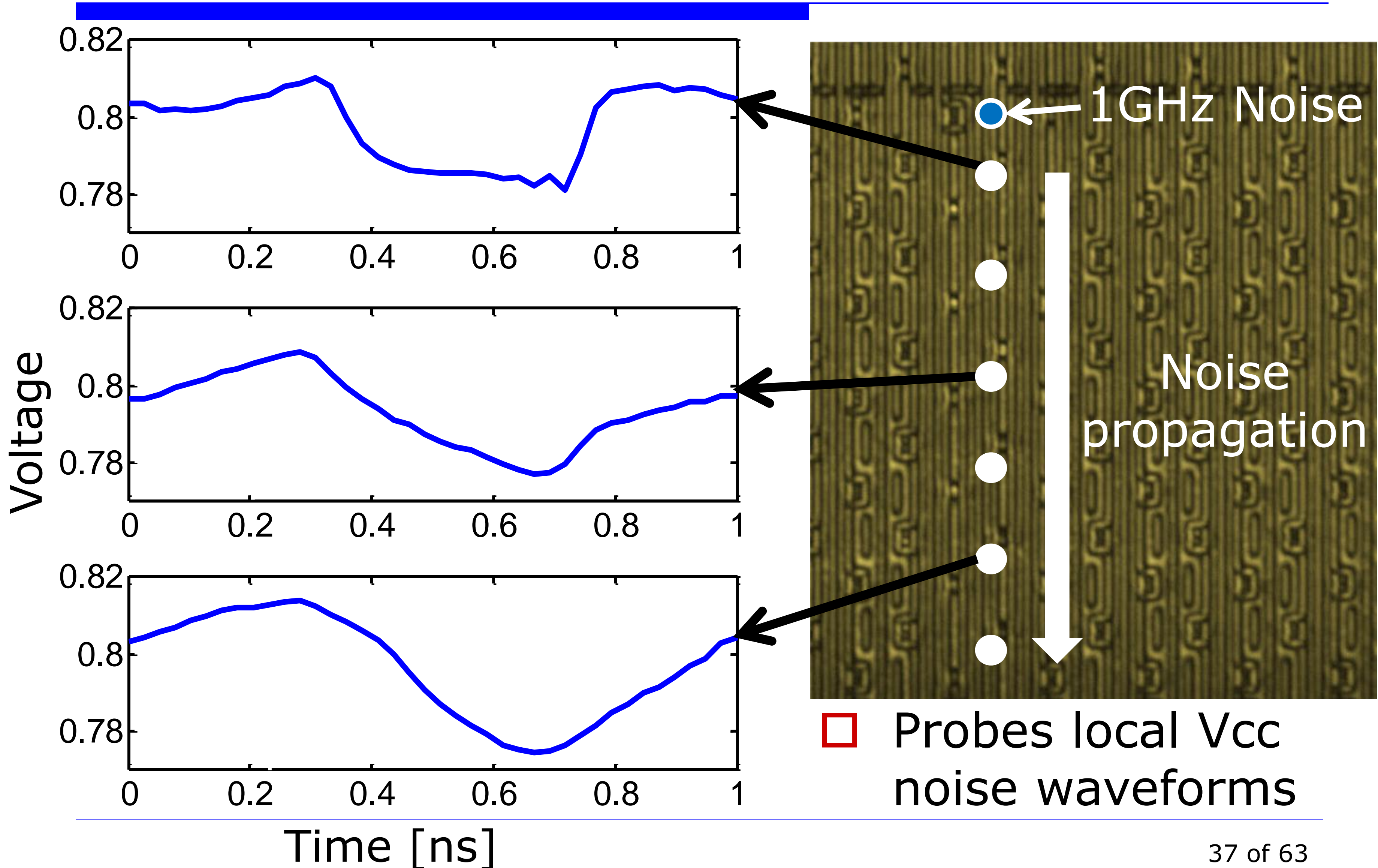
Supply Noise Meas. on I/O Testchip





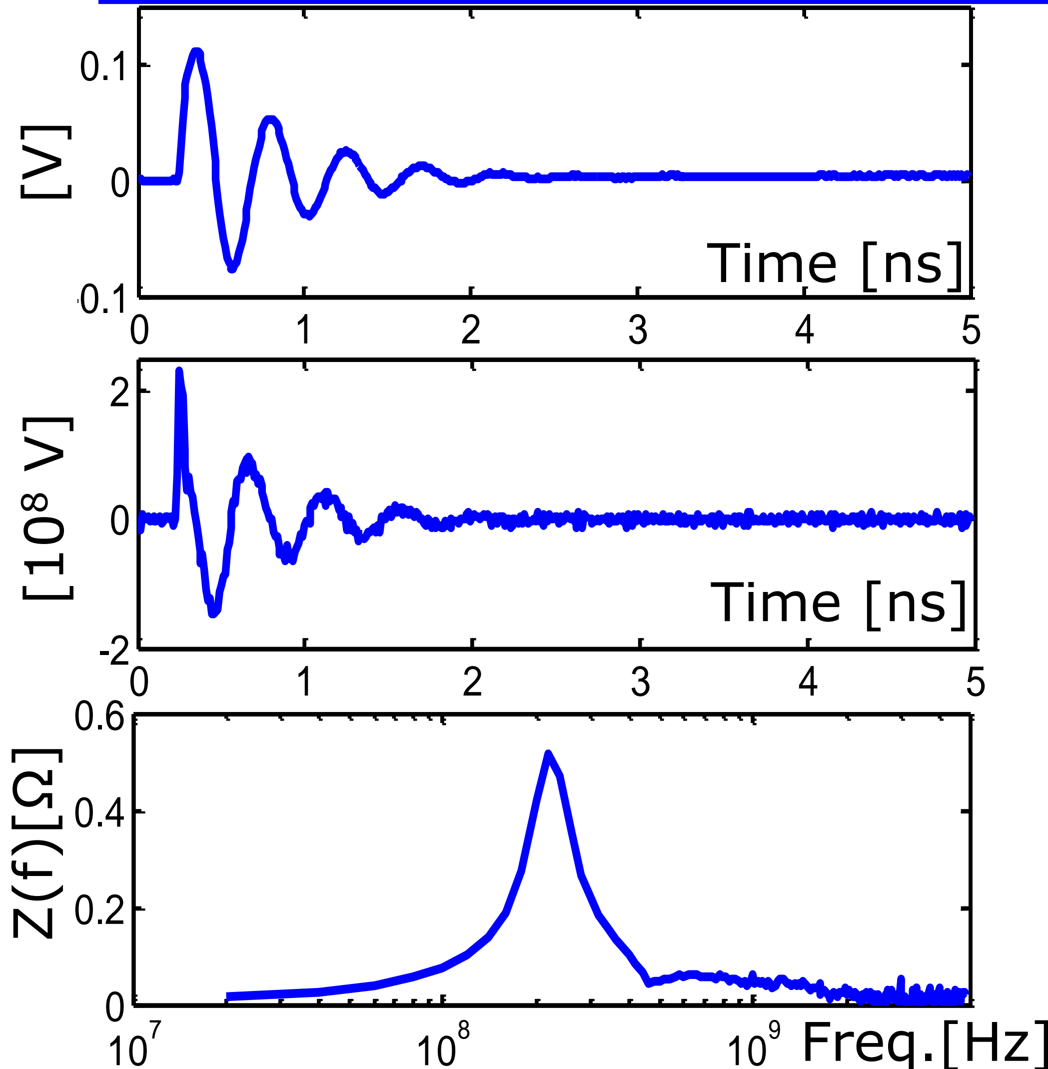
Ref: F. O'Mahony, ISSCC 2010

Periodic Noise Waveform Capture



- Probes local Vcc noise waveforms

Power Supply Impedance Meas.



Step Response
(w/ current step)

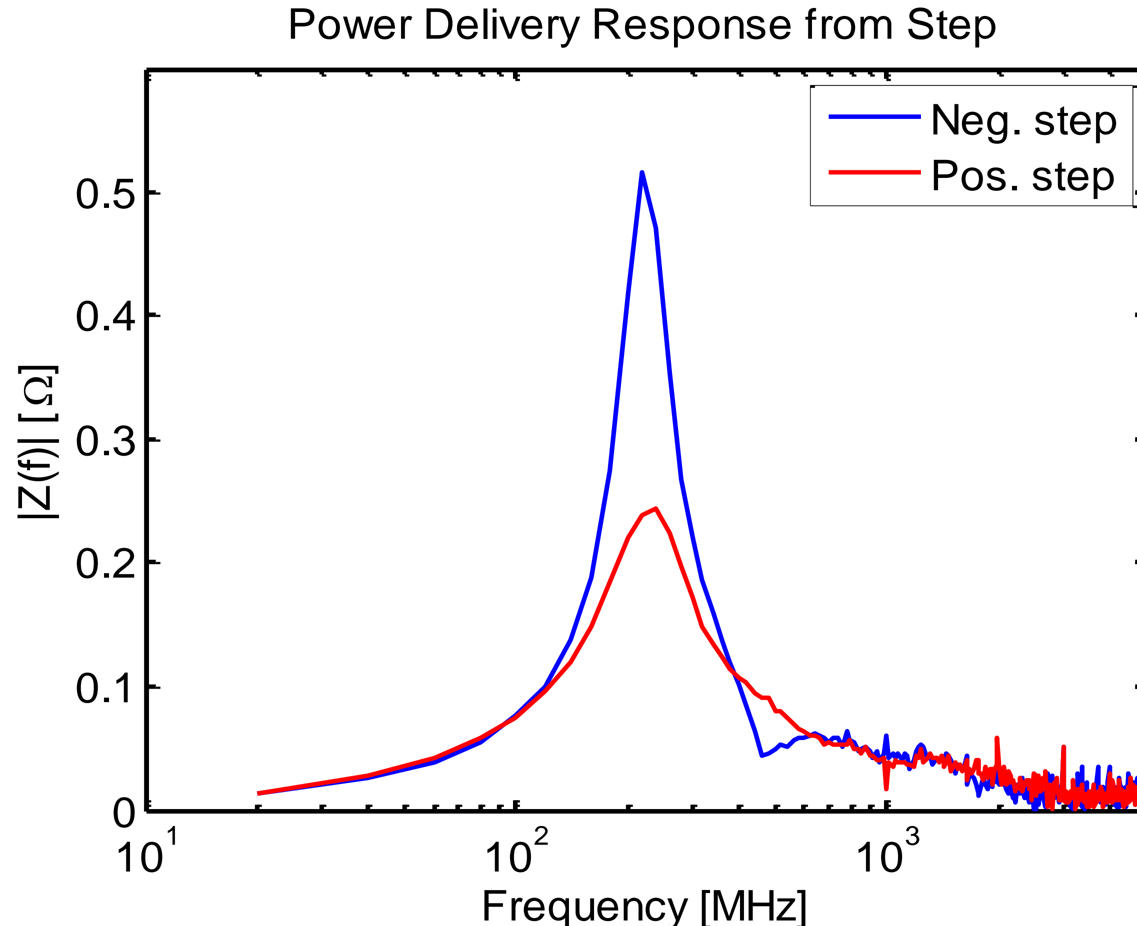
dV/dt

Impulse Response

DFT

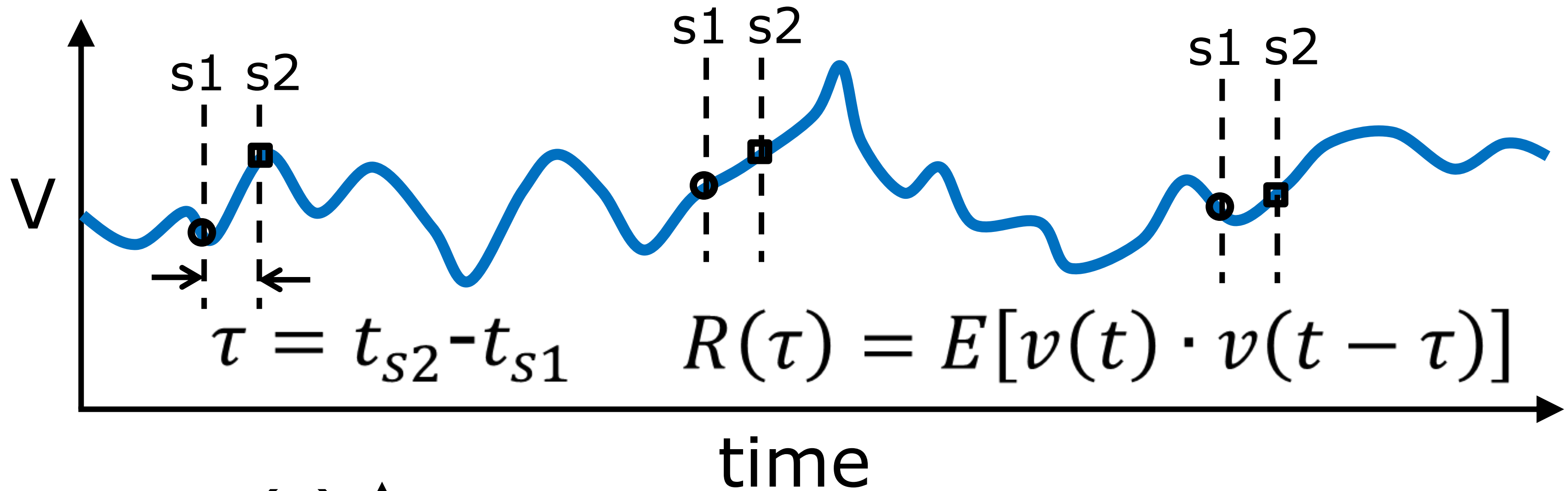
Freq. Response
Z(f)

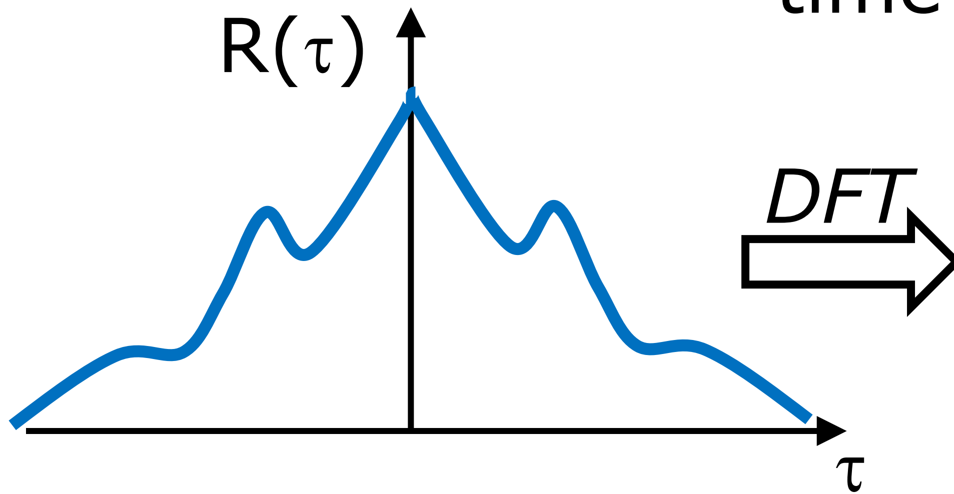
Impedance Measurement Example



- Note that Q depends on the power grid loading

Measuring PSD w/ Autocorrelation

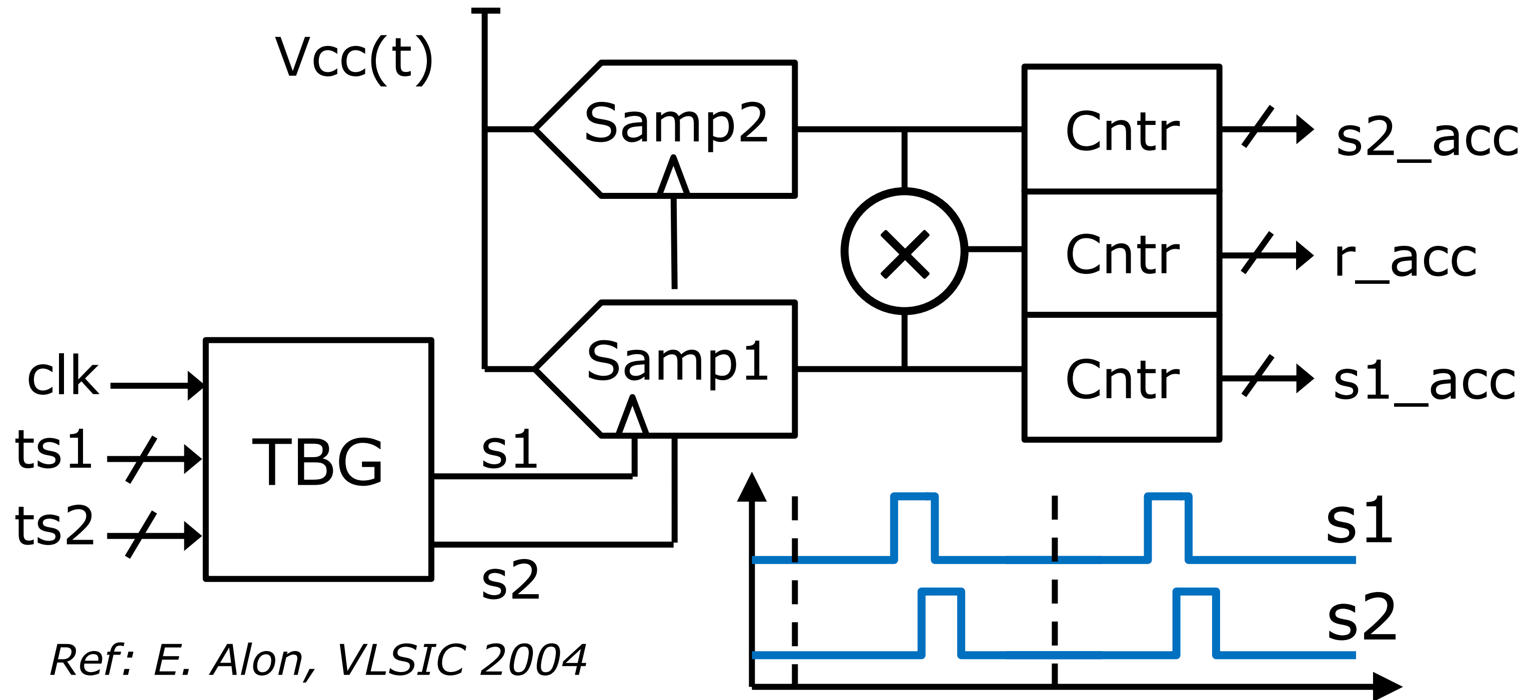




DFT ⇨

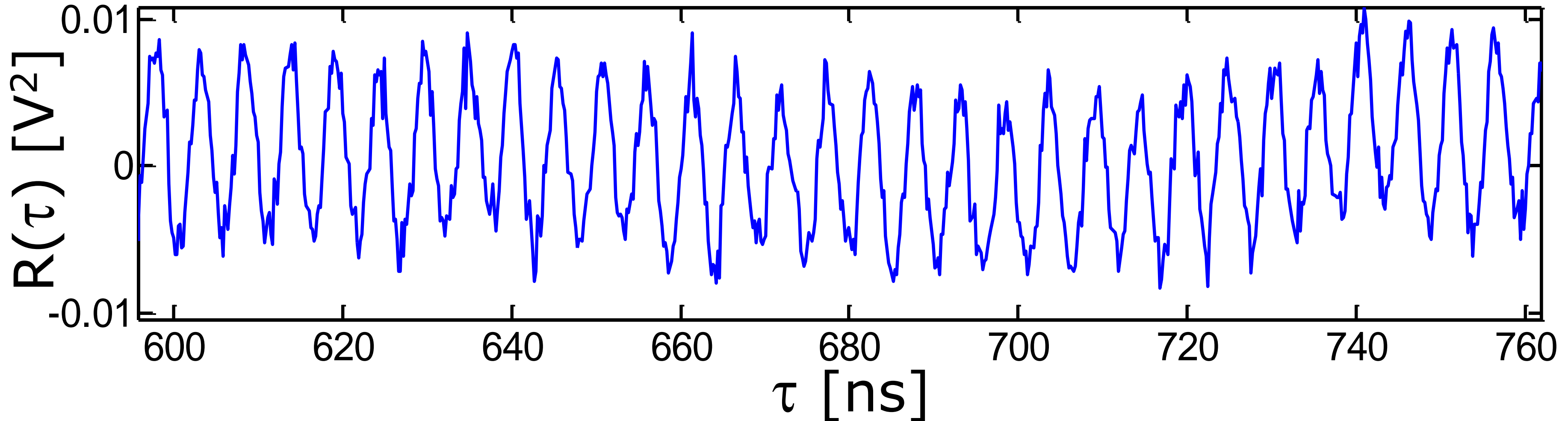
Power Spectral Density
PSD(f)

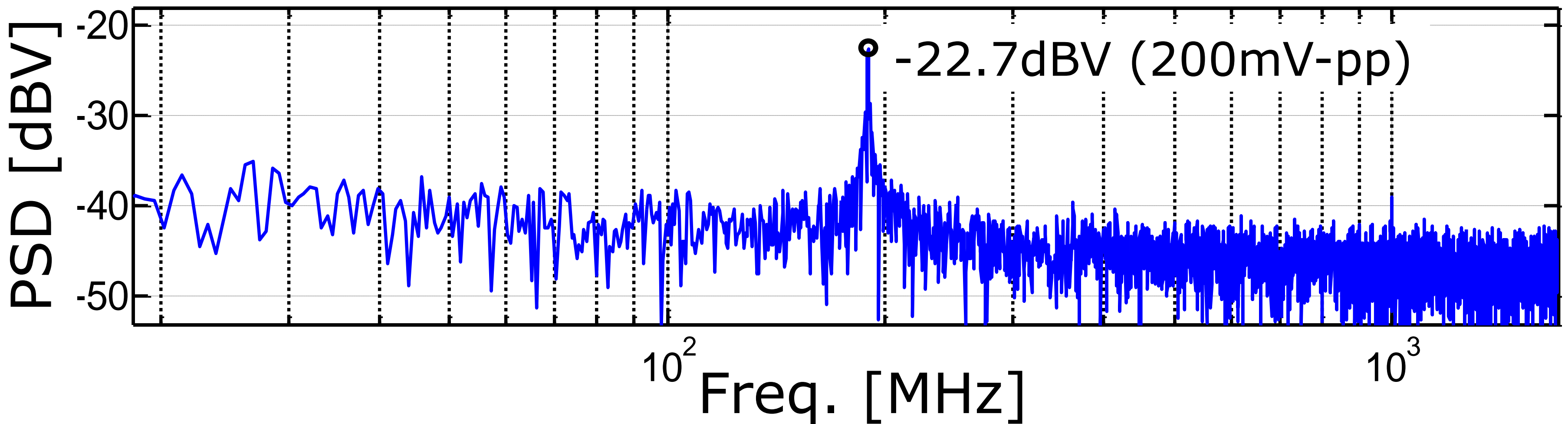
Circuitry for PSD Meas.



- Measure R(τ) with dual samplers
- Digitally sweep τ = ts2-ts1
- DFT of R(τ) = PSD (post-process off-chip)

PSD Measurement Example

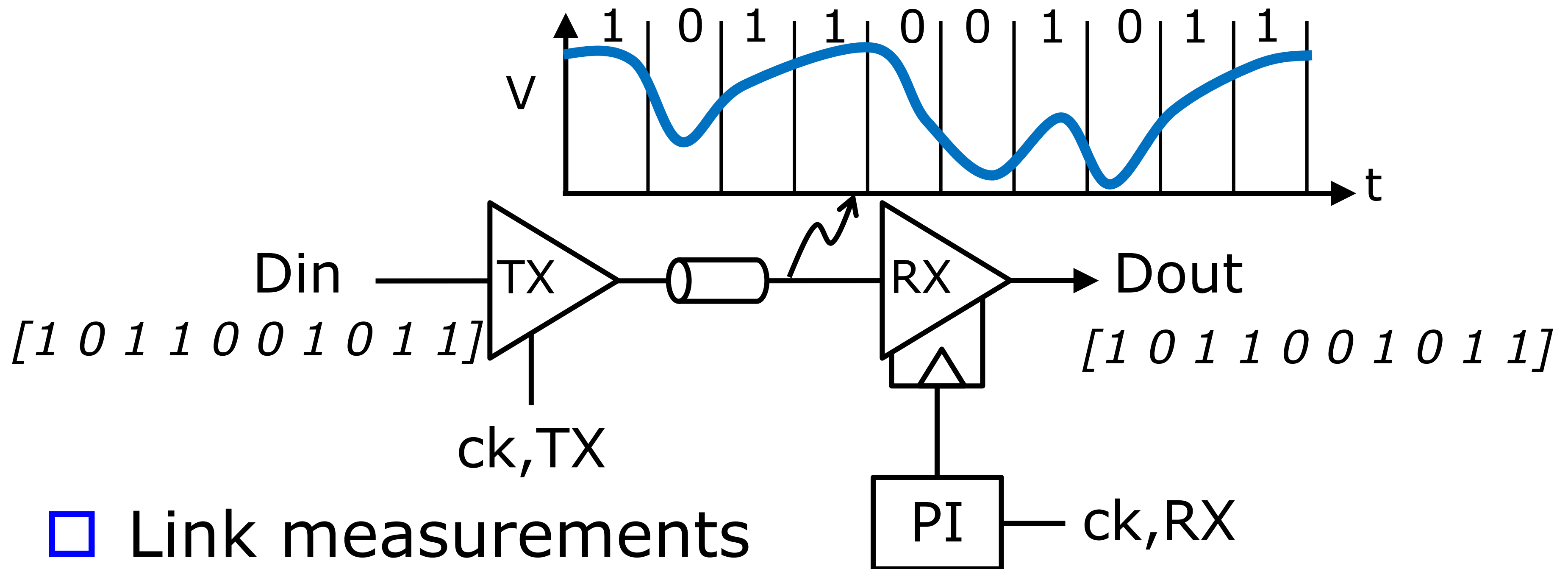




Outline

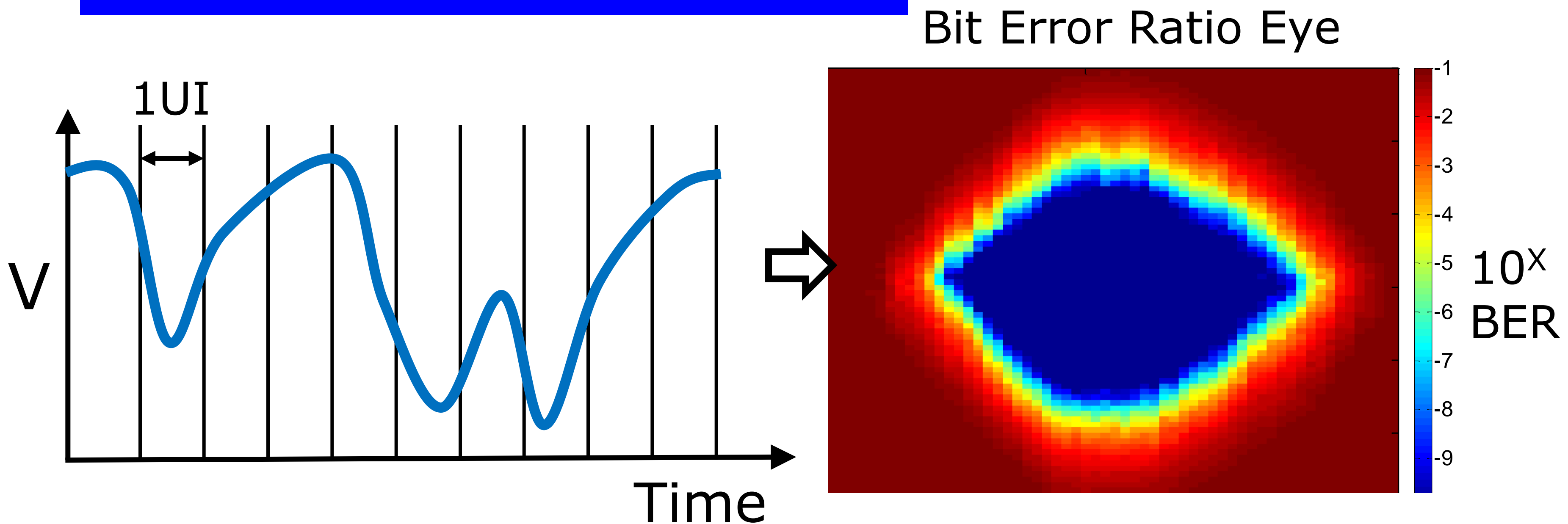
- Delay Measurement
- Power Supply Characterization
- **I/O System Characterization**
  - Bit Error Rate (BER) Eye
  - Waveform capture
  - RX noise
  - Clk-data jitter

Transceiver Metrics



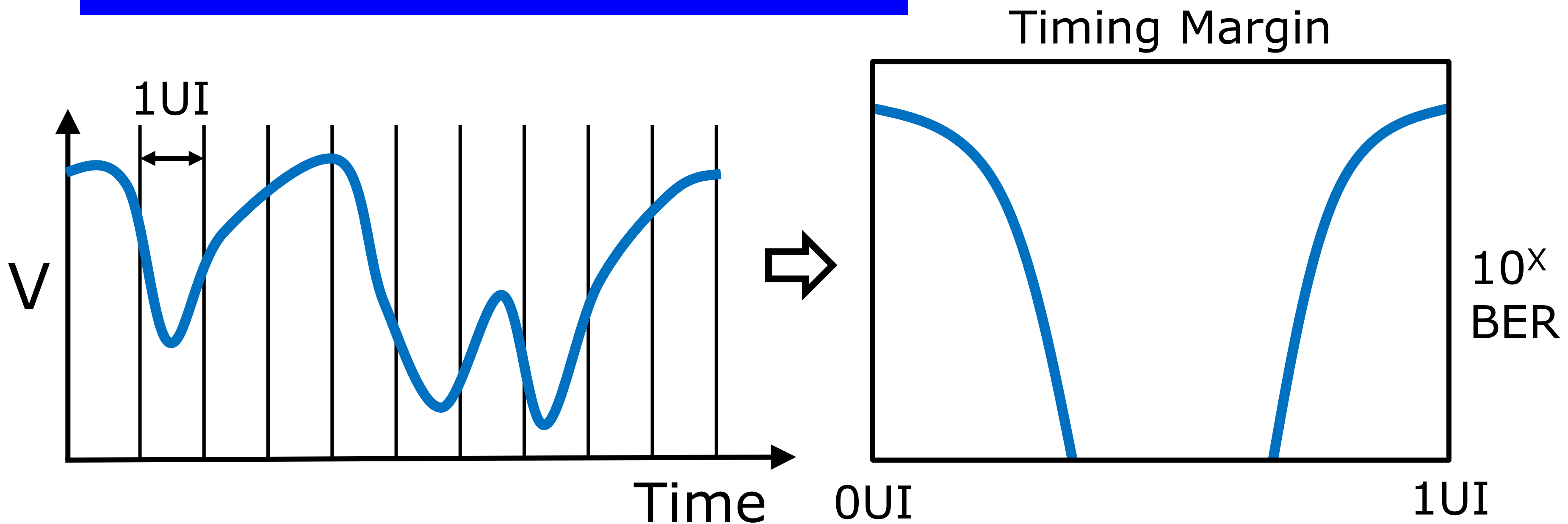
- Link measurements
  - BER eye / Eye Margins
  - Receiver noise
  - Clock/Data jitter
  - Waveform capture

BER Eye and Margins



- Probability of error in Equivalent time
- Sweeps Voltage and Equivalent Time
- “Margin” represents how robust the link is
- Voltage margin (vert.), Timing margin (horiz.)

BER Eye and Margins



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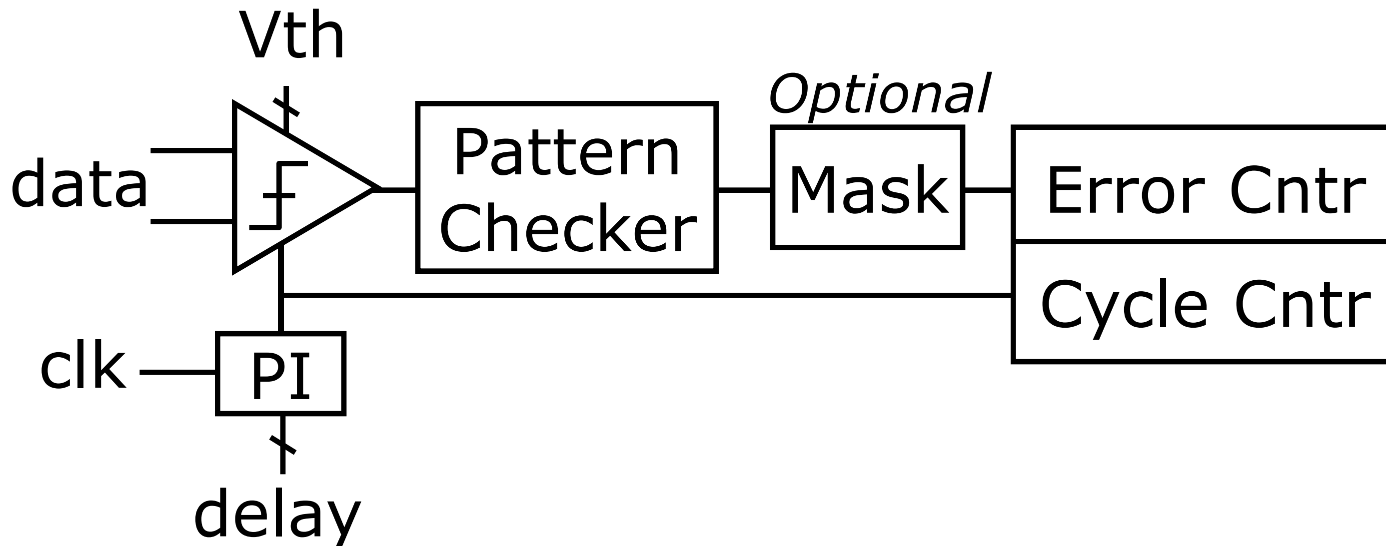
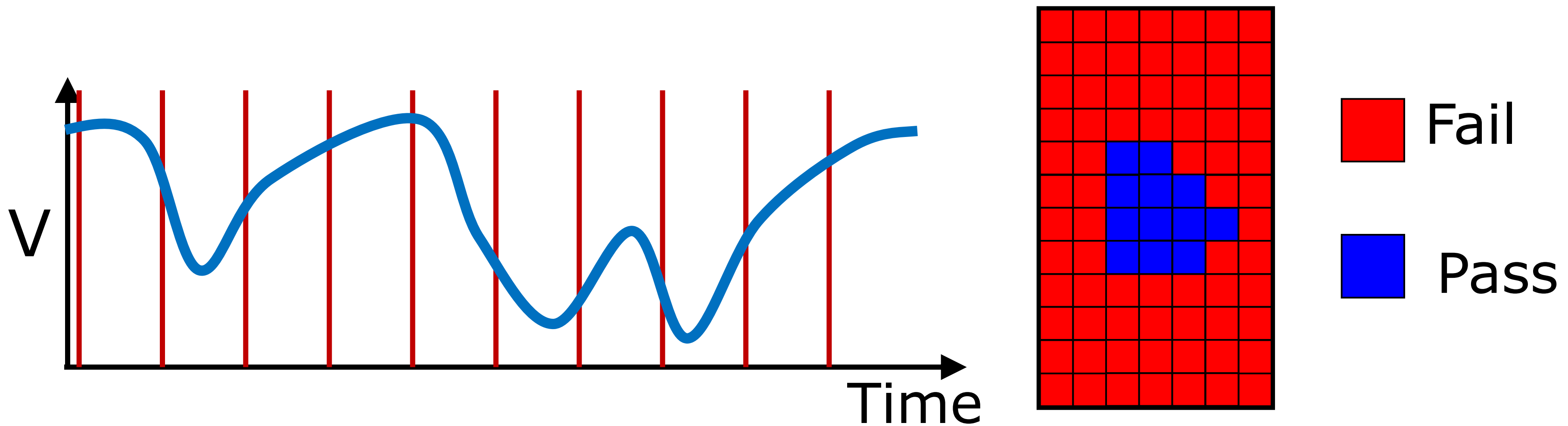
BER Eye Measurement



- Phase Interpolator (PI) → Time Sweep
- Sampler Offset → Voltage Sweep
- Masking can be used optionally to target certain characteristics
  - e.g. Loop-unrolled eye, Even/Odd eyes

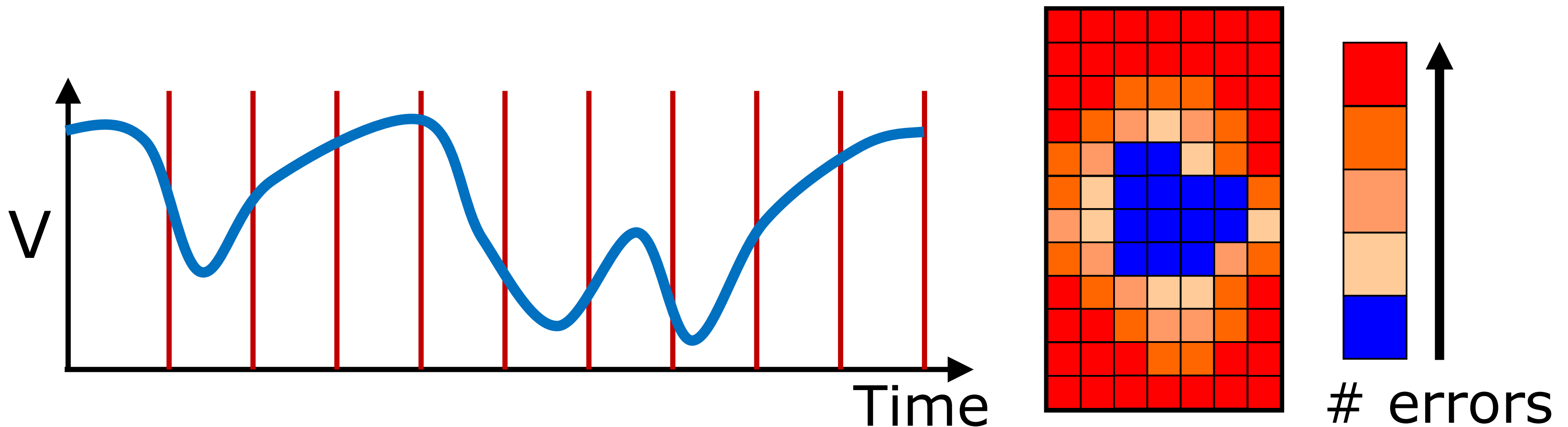
BER Eye Measurement



- Keep in mind N_{err}/N_{bits} is just an *estimation* of BER
- Rule of Thumb: 95% Confidence Level requires error-free transmission for N_{bits} = 3xBER$_{min}$
  - e.g. No errors for 3×10^{12} bits indicates BER$\leq 10^{-12}$ with 95% certainty

Ref: http://cp.literature.agilent.com/litweb/pdf/5989-2933EN.pdf

BER Eye Measurement



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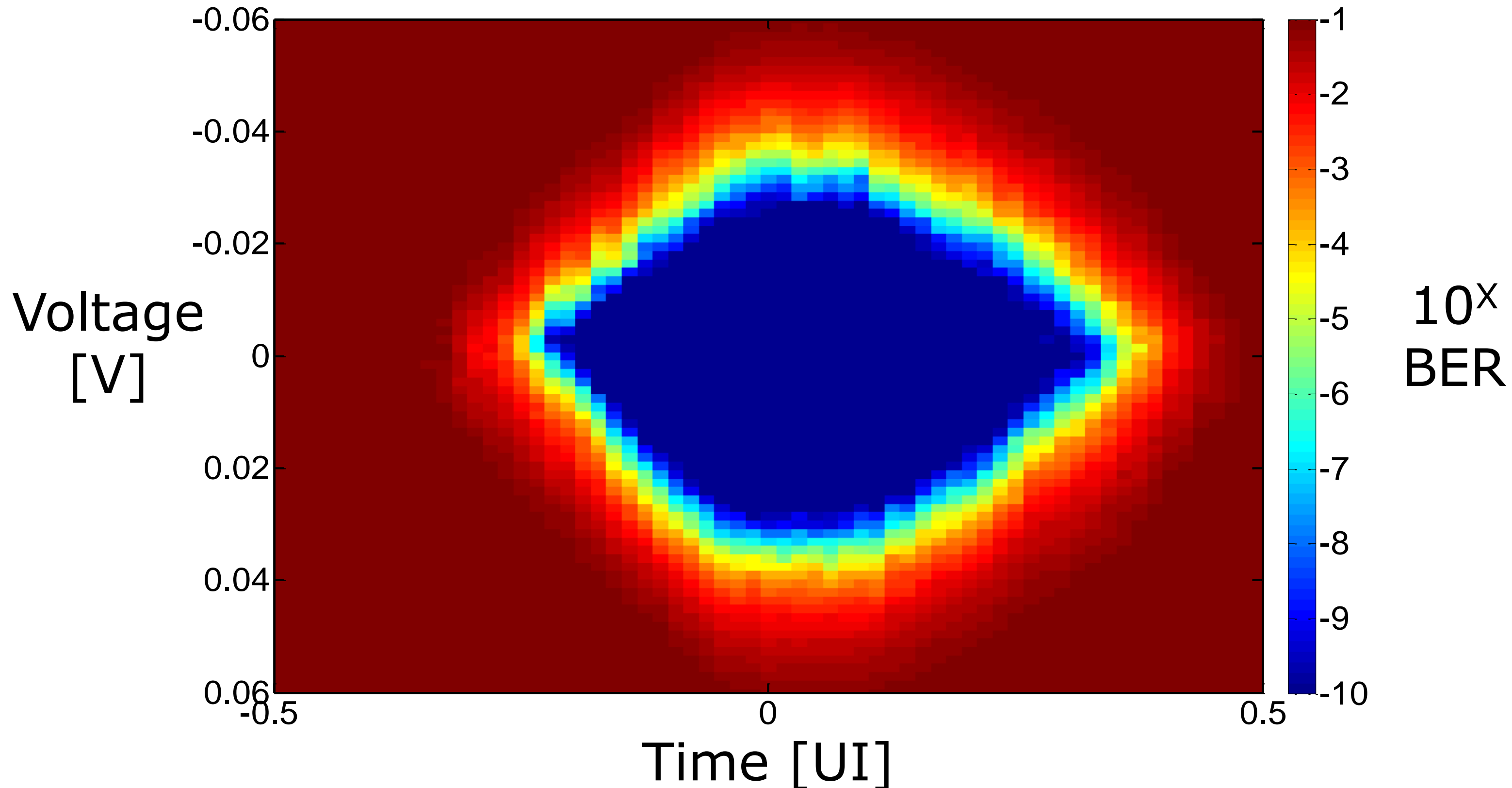
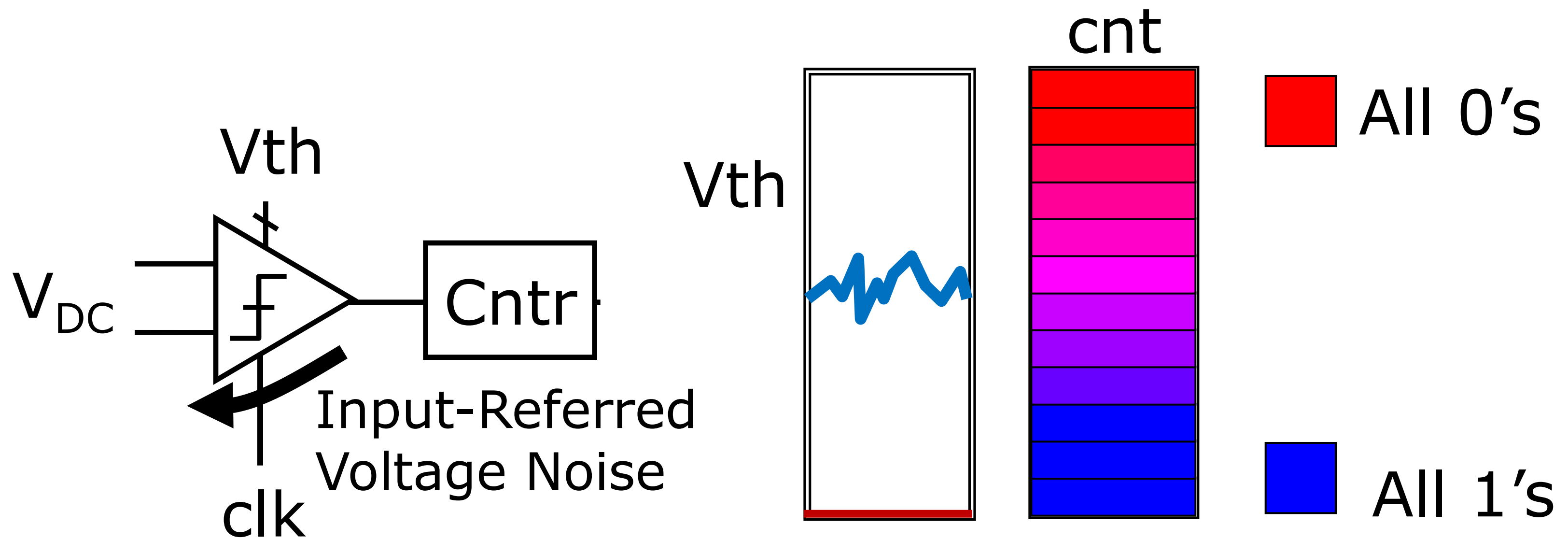
Measured BER Eye Example



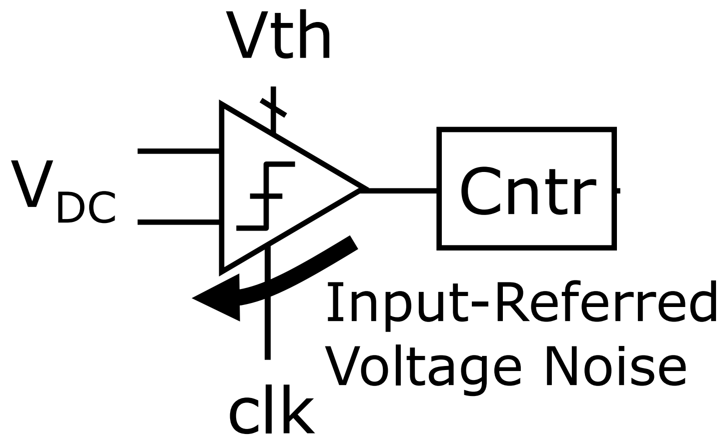
- Often measure a subset of points to save time
  - Voltage or Time Margin “bathtub” plots

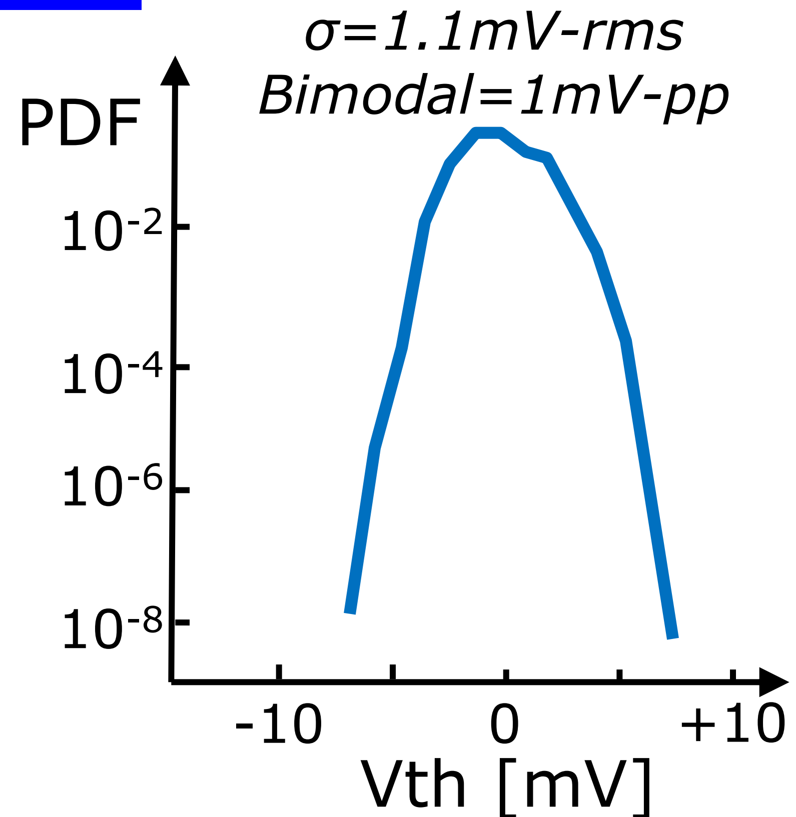
RX Sampler Characterization



- Voltage CDF (PDF) → RX characterization
- Reflects all RX noise as "input referred"
- Fully in-situ if TX provides V_{DC}

RX Sampler Characterization





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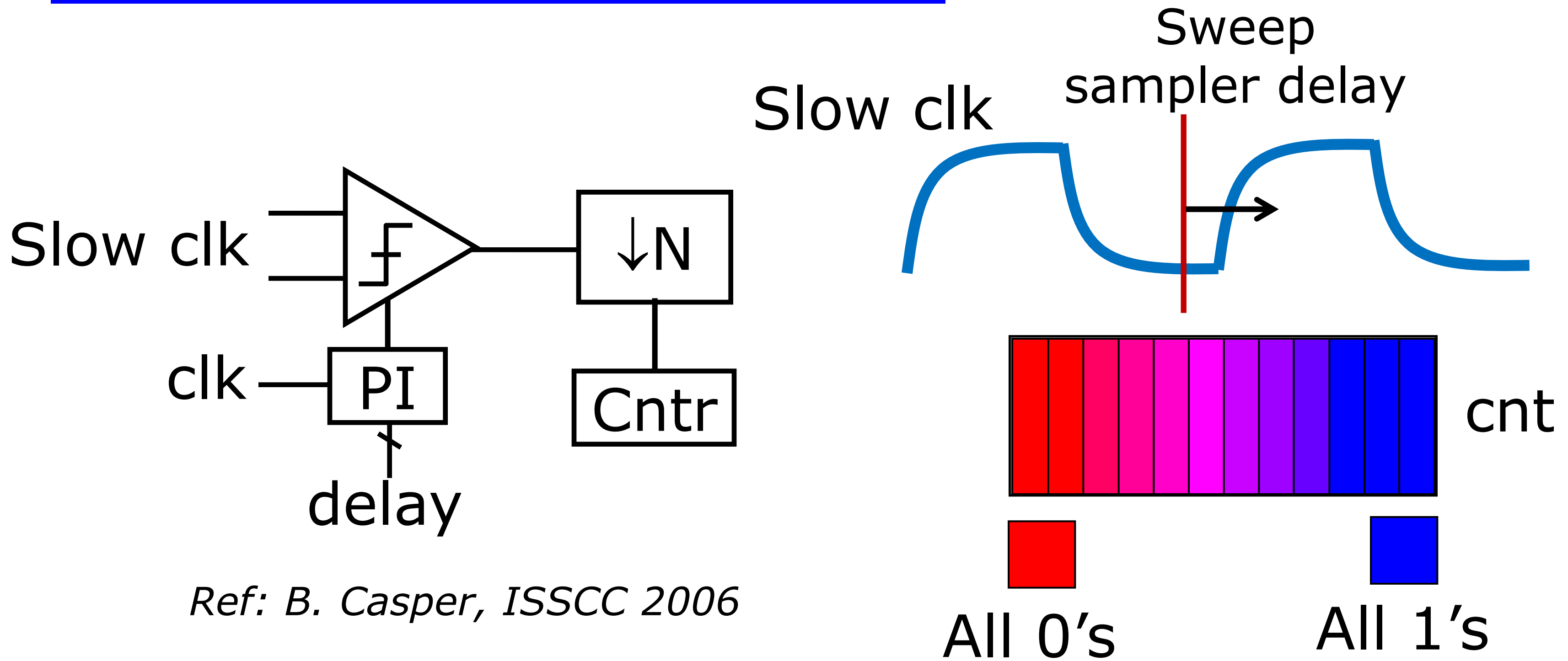
Clock-Data Jitter



Ref: B. Casper, ISSCC 2006

- Time CDF (PDF) → RX clk-data jitter
- Fully in-situ if TX provides "slow clock"
- Applicable to any clock circuit

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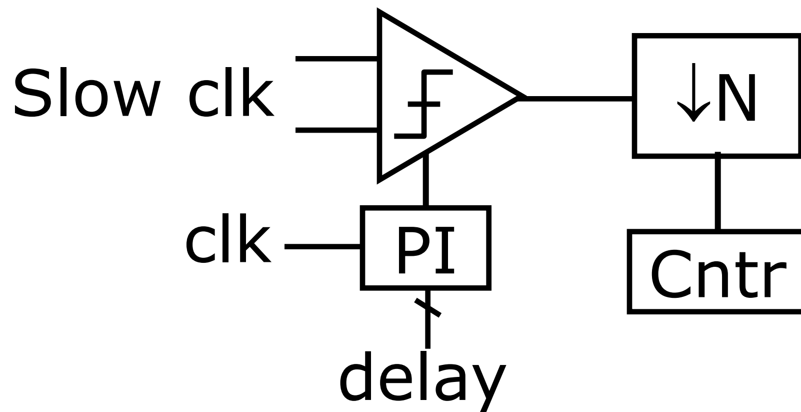

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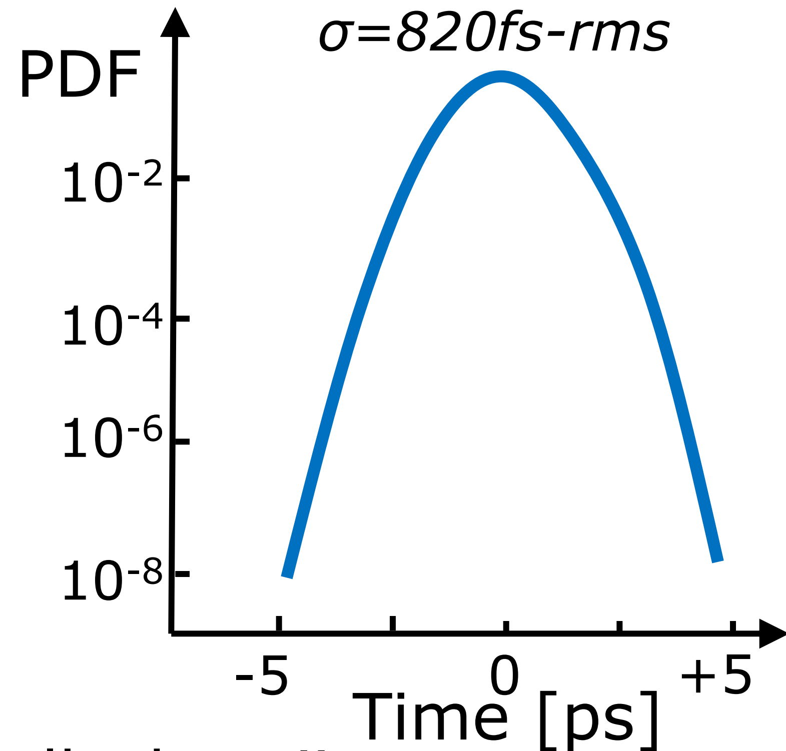

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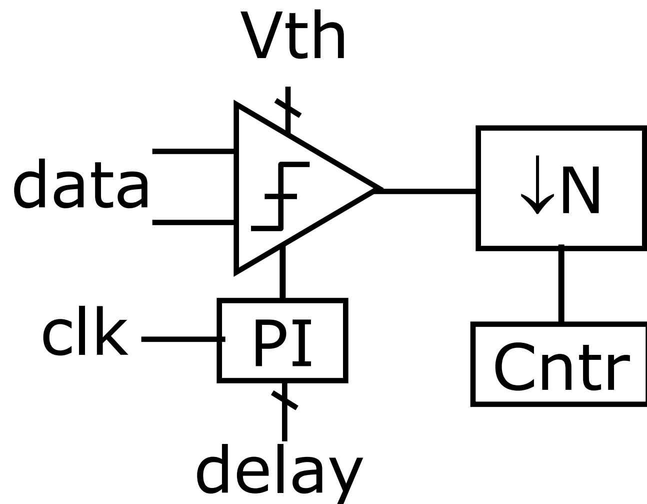
On-die waveform capture

- Mask 1:N periodic N-bit waveform
- CDF mean = V(t)
- PI sweeps time



Ref: B. Casper, JSSC 2003

Equiv. Time

On-die waveform capture

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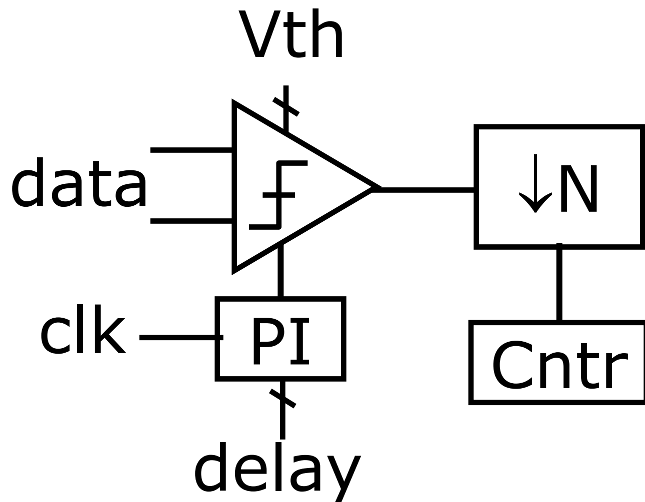

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Equiv. Time

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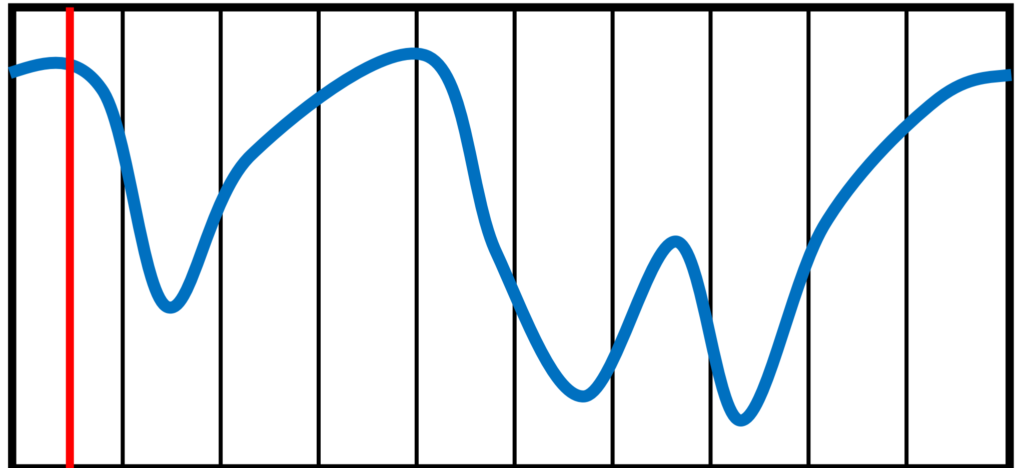
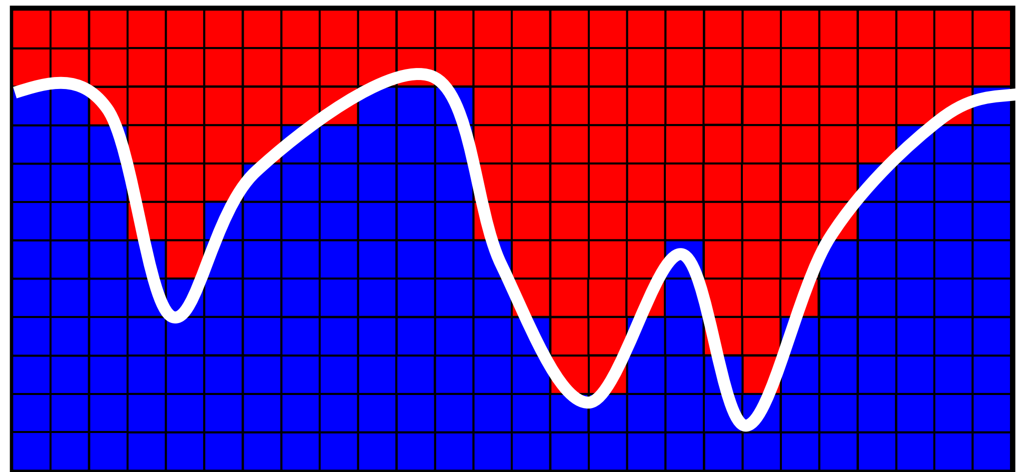
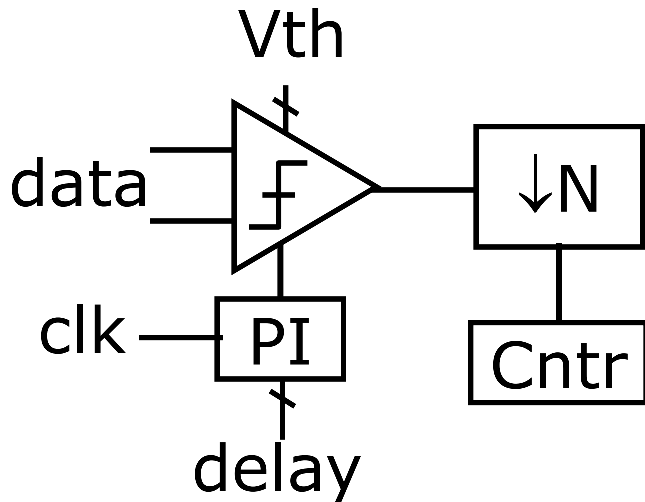




Equiv. Time



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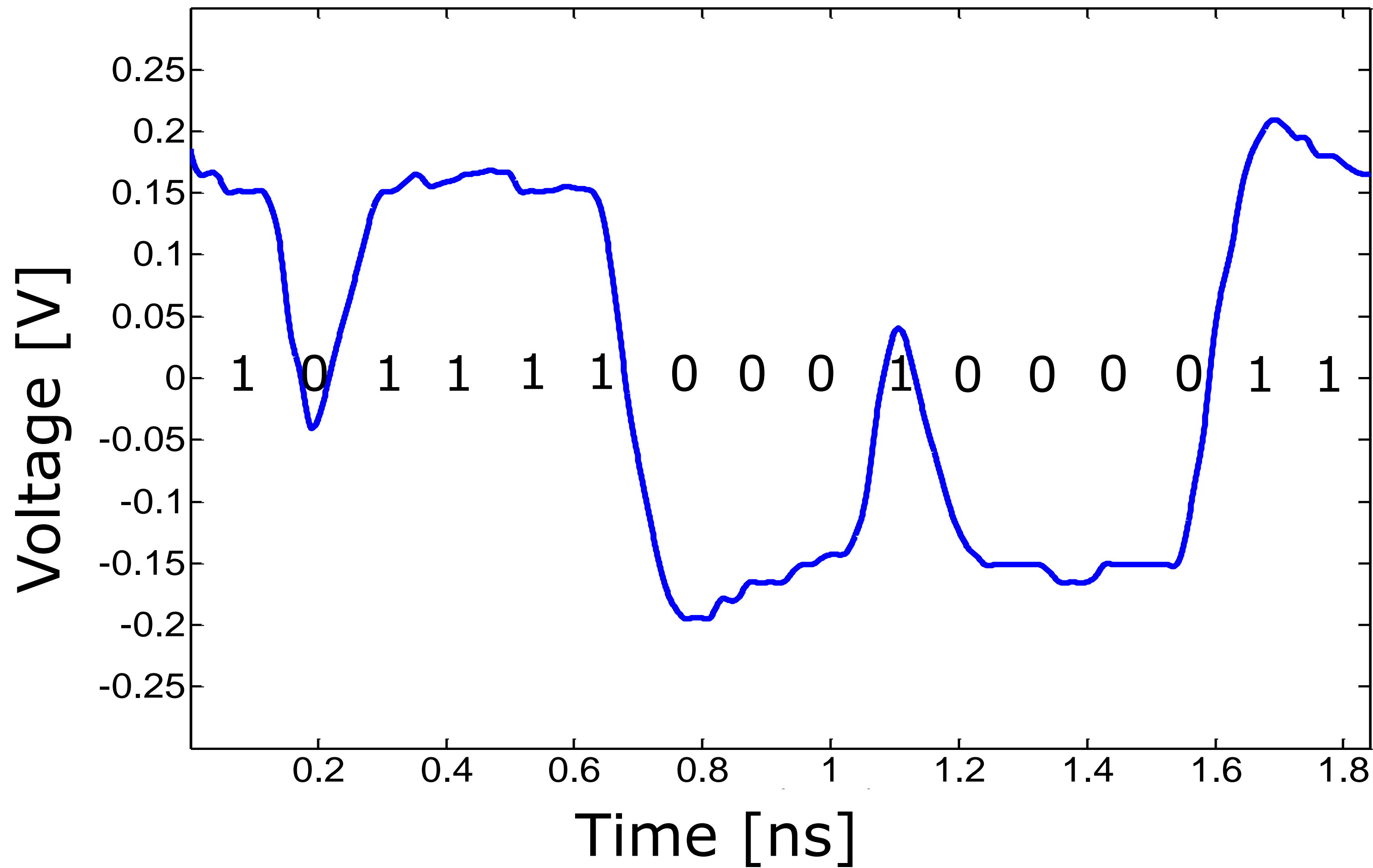
Waveform Capture Example



Summary

- On-die measurement is useful when:
  - No external equipment available
  - Accuracy lost by routing out to scopes
- A simple set of digital-friendly techniques provide accurate time and voltage on-chip
  - Code Density Test
  - Equivalent time/Sub-sampling/Bit Masking
  - Time/Voltage sweep with 1-bit ADC
- Use measurement circuits that are already on chip!
  - Offset comparators, phase shifters, digital counters, pattern checkers

Key Refs: Delay Measurement

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- L.-M Lee et. al, "A sub-10-ps multiphase sampling system using redundancy," *JSSC* Jan. 2006, pp. 265-273.
- L. Xia, et al., “Sub-2ps, static phase error calibration technique incorporating measurement uncertainty cancellation for multi-gigahertz time-interleaved T/H circuits,” *TCAS-I*, Jan. 2012, pp.1-9.
- Mansuri, M. et al., "An on-die all-digital delay measurement circuit with 250fs accuracy," *Symp. VLSI Circuits (VLSIC)* 2012, pp.98-99.

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- V.A. Abramzon et al., "Scalable circuits for supply noise measurement," *ESSCIRC 2005.,* pp. 463- 466.
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- F. O'Mahony et al., "A Low-Jitter PLL and Repeaterless Clock Distribution Network for a 20Gb/s Link," *Symp. VLSI Circuits (VLSIC),* 2006, pp.29

Key References: I/O Characterization

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- M. Takamiya, M. Mizuno, and K. Nakamura, "An on-chip 100GHz-sampling rate 8-channel sampling oscilloscope with Embedded sampling clock generator," *ISSCC* 2002.
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- M. Mueller et al., "Total Jitter Measurement at Low Probability Levels, Using Optimized BERT Scan Method", Agilent White Paper. http://cp.literature.agilent.com/litweb/pdf/5989-2933EN.pdf
- B. Casper et al., "A 20Gb/s Forwarded Clock Transceiver in 90nm CMOS," *ISSCC 2006*, pp.263-272.
- F. O'Mahony et al., "A 47x10 Gb/s 1.4 mW/Gb/s Parallel Interface in 45nm CMOS," *JSSC*, pp. 2828 - 2837, Dec. 2010.