P2851

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Type of Project: New IEEE Standard
Project Request Type: Initiation / New
PAR Request Date: 17 Sep 2019
PAR Approval Date: 07 Nov 2019
PAR Expiration Date: 31 Dec 2023
PAR Status: Active

1.1 Project Number: P2851
1.2 Type of Document: Standard
1.3 Life Cycle: Full Use

2.1 Project Title: Standard for Exchange/Interoperability Format for Functional Safety Analysis and Functional Safety Verification of IP, SoC and Mixed Signal ICs

3.1 Working Group: Exchange/Interoperability format for functional safety analysis and safety verification of IP, SoC and mixed signal ICs(C/DA/Functional Safety Format)

3.1.1 Contact Information for Working Group Chair:
Name: Riccardo Mariani
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3.1.2 Contact Information for Working Group Vice Chair:
None

3.2 Society and Committee: IEEE Computer Society/Design Automation(C/DA)

3.2.1 Contact Information for Standards Committee Chair:
Name: Stanley Krolikoski
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3.2.2 Contact Information for Standards Committee Vice Chair:
None

3.2.3 Contact Information for Standards Representative:
None

4.1 Type of Ballot: Entity
4.2 Expected Date of submission of draft to the IEEE SA for Initial Standards Committee Ballot: Dec 2020
4.3 Projected Completion Date for Submittal to RevCom: May 2021

5.1 Approximate number of entities expected to be actively involved in the development of this project: 15
5.2 Scope of proposed standard: This standard defines a data format with which results of functional safety analyses (such as FMEA (Failure Mode and Effects Analysis), FMEDA (Failure Modes, Effects and Diagnostic Analysis), FMECA (Failure Mode, Effects and Criticality analysis), FTA (Fault Tree analysis) and related functional safety verification activities - such as fault injection - executed for IPs (Intellectual Property. See note in section 8.1), SoCs (System on Chip) and mixed signal ICs (Integrated Circuit) can be exchanged and made available to system integrators. The format will define languages, data fields and parameters with which the result of those analyses and verification activities can be represented, in a technology independent way. The goal of the standard is to provide a common ground for EDA (Electronic Design Automation), SoC and IP vendors in needs of developing tools, SoC and IP for functional safety critical applications.

5.3 Is the completion of this standard contingent upon the completion of another standard? No
5.4 Purpose: This standard provides an exchangeable exchange/interoperability format for functional safety analysis and functional safety verification activities so as to facilitate IP vendors and SoC providers in delivering results to functional safety critical system integrators in a consistent way so as to also make possible Interoperability between tools provided by EDA vendors.
5.5 Need for the Project: The development of IPs and SoCs for functional safety critical applications is rapidly emerging due to the growth of applications such as automated driving or robotics. Standards such as ISO 26262 (automotive https://www.iso.org/standard/68383.html), IEC 61508 (industrial https://www.iec.ch/functionalsafety/) and many others are requiring IP vendors and SoC providers in executing functional safety analyses (such as FMEA, FMEDA, FMECA, FTA) and related functional safety verification activities - such as fault injection - and deliver results to system integrators. EDA vendors are also starting

to provide tools to automate those activities. However, at this time, there is not a common language or format to provide those results. In the end system integrators are struggling with many different types of data, so spending a huge amount of effort to reconsolidate, compare, integrate, combine the data. For that reason, the functional safety critical community is strongly asking for a solution to accelerate the functional safety engineering process while reducing risks and costs.

5.6 Stakeholders for the Standard: Automotive OEMs (Original Equipment Manufacturer), Tier1 Semiconductor Suppliers, IP and SoC providers, EDA vendors

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6.1 Intellectual Property

6.1.1 Is the Standards Committee aware of any copyright permissions needed for this project? No

6.1.2 Is the Standards Committee aware of possible registration activity related to this project? No

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7.1 Are there other standards or projects with a similar scope? No

7.2 Is it the intent to develop this document jointly with another organization? No

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8.1 Additional Explanatory Notes : Pre-designed semiconductor circuits are commonly known as "Intellectual Property" (or "IP") in the Electronics Industry