VHSIC and The First CMOS and Only Cryogenically Cooled Super Computer

David Bondurant
Former Honeywell Solid State Electronics Division VHSIC System Applications Manager

ETA10 Supercomputer at MET Office - UK’s National Weather Forecasting Service

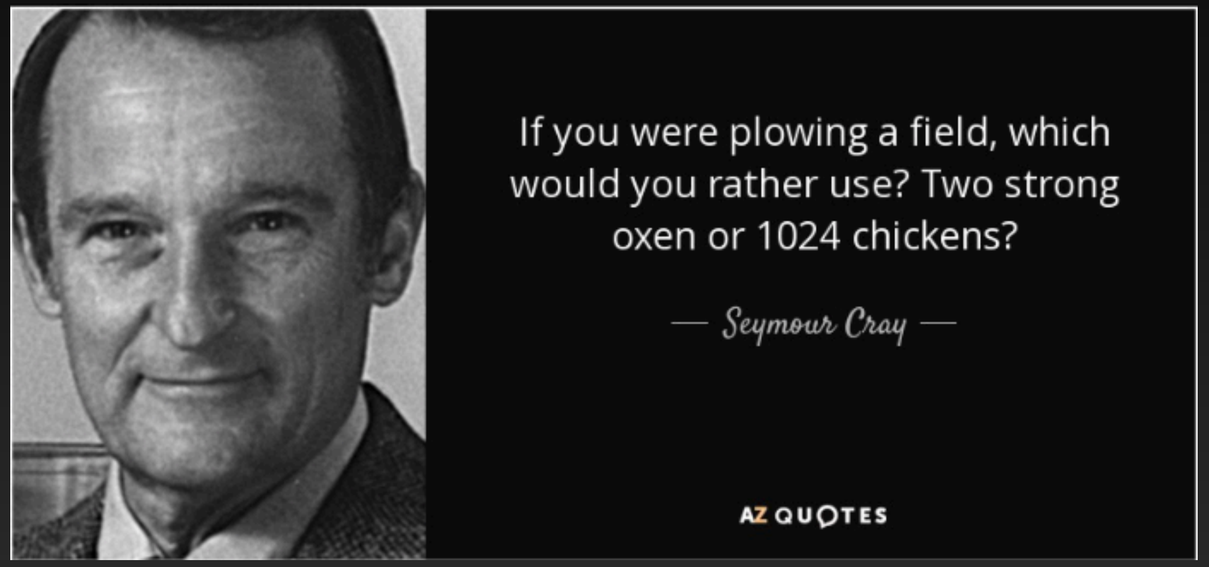
Sources

- “Very High Speed Integrated Circuits (VHSIC) Final Program Report 1980-1990, VHSIC Program Office”, Office of the Under Secretary of Defense for Acquisition, Deputy Director, Defense Research and Engineering for Research and Advanced Technology, September 30, 1990
- Carlson, Sullivan, Bach, and Resnick, “The ETA10 Liquid-Nitrogen-Cooled Supercomputer System”, IEEE Transactions on Electron Devices, Vol. 36, No. 8, August 1989.
- Cummings and Chase, “High Density Packaging for Supercomputers”
- Tony Vacca, “First Hand: The First CMOS And The Only Cryogenically Cooled Supercomputer”, ethw.org
- Robert Peglar, “The ETA Era or How to (Mis-)Manage a Company According to Control Data Corp.”, April 17, 1990

Background

- I graduated from Missouri S&T in May 1971
- My first job was at Control Data Corporation, the leading Supercomputer Company
- I worked in Memory Development
- CDC 7600 was in production, 8600 (Cray 1) was in development by Seymour Cray in Chippewa Falls, WI
- Star 100 Vector Processor was in Development in Arden Hills
- I was assigned to the development of the first DRAM Memory Module for a CDC Supercomputer
- I designed the DRAM Module Tester Using ECL Logic
- First DRAM Module was 4Kx32 using 128 1K DRAM Chips Mounted on 2 6x9 inch 12-Layer PCB with Freon Cooling

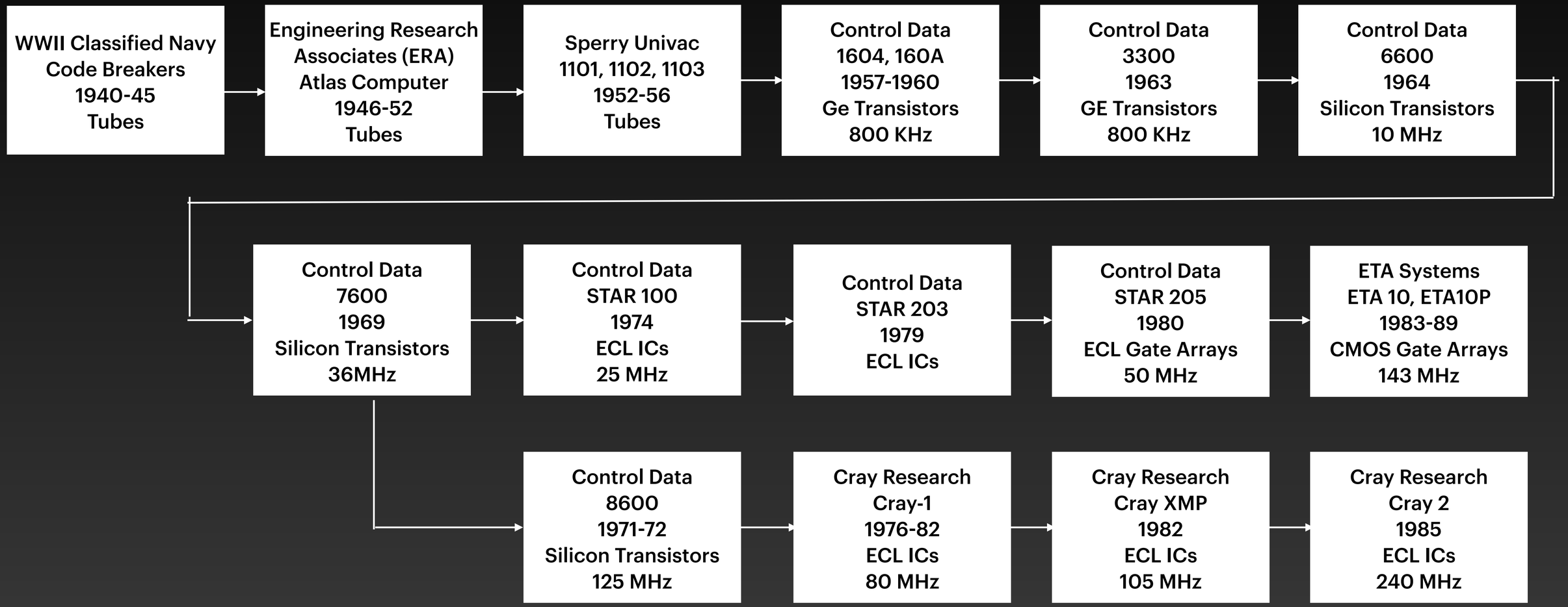
Control Data Corporation Arden Hills Development Center - June 1971



As long as we can make them smaller, we can make them faster.
~ Seymour Cray

#3 pencils and quadrille pads.(when asked what CAD tools he used to design the Cray I supercomputer)
~ Author: Seymour Cray

CDC/ETA System History Review



Sperry Univac

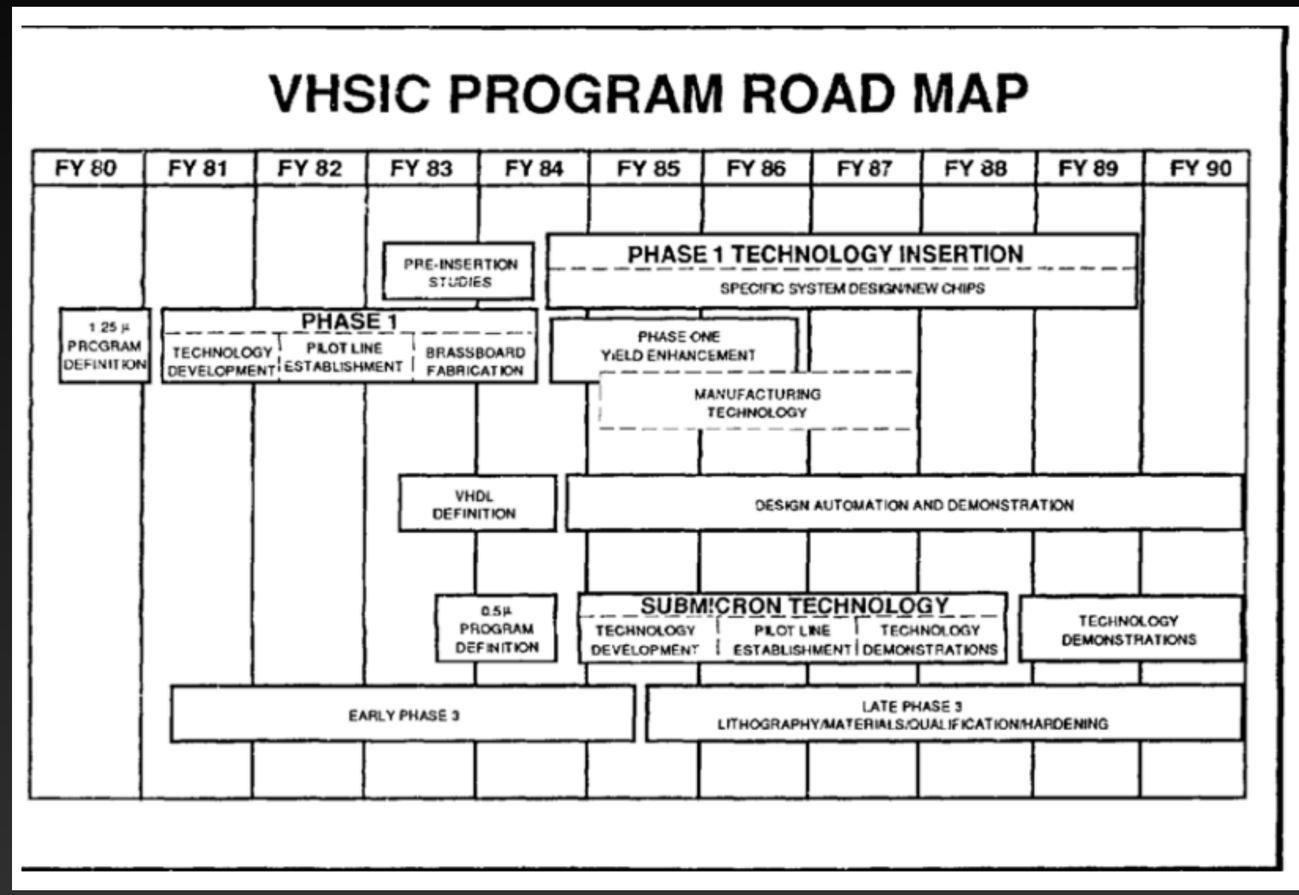
- I moved to Sperry Univac Defense Systems in 1972, the leading Navy military computer developer
- Developed Microprogrammed IOC and Disk Controller for Trident SPO using TTL Logic
- Upgraded & Qualifed Trident CP-890B and IO Processor for Trident Submarine (DTL Discrete logic)
- Developed circuit & packet switches for McAutoNet
- Developed 32-bit Alternate Avionics Computer for B-1 Bomber (TTL Logic, FPLA)
- Developed microprogrammable Signal Process Element (SPE) parallel processor for sonar & radar processing (TTL, Bit Slice uP, VLSI Multiply-Adder)
- Developed First Mil-STD-1553 serial multiplex I/O module for Air Force SEAFAC Lab, Wright Patterson
- Chipset Architect for TRW, Motorola, Univac VHSIC Phase 0 Project

Sperry Univac Defense System Eagan MN - June 1972-1980

VHSIC Program

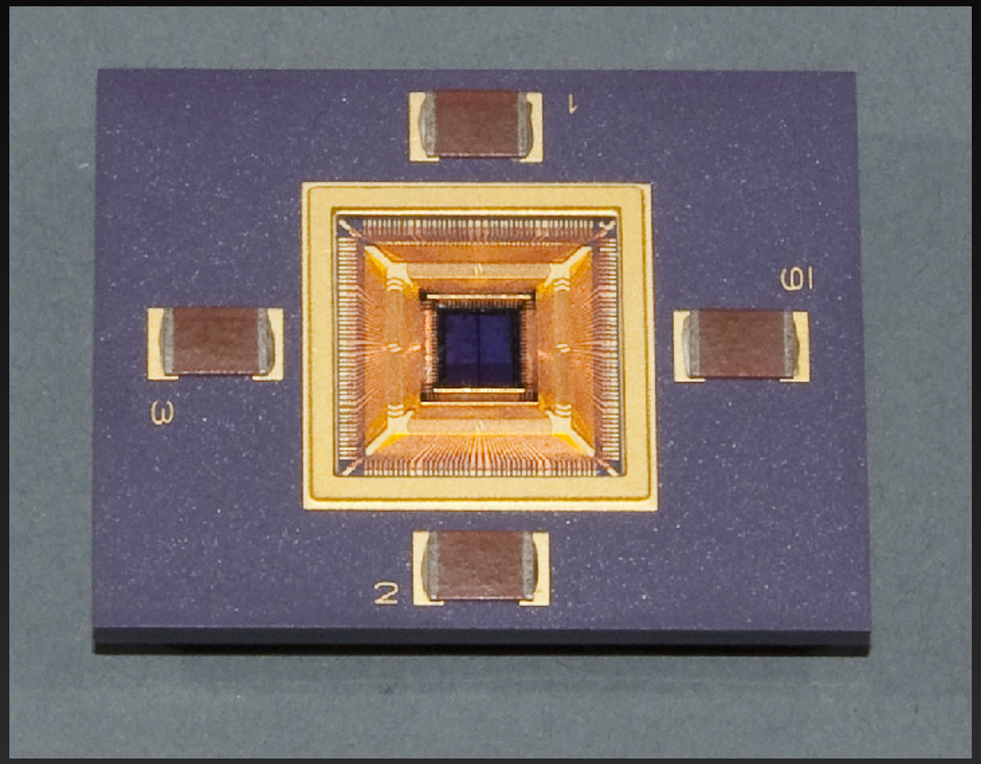
Very High Speed Integrated Circuits

- Prior to 1980, DoD determined that US military was lagging in deployment of leading edge technology in fielded system
- VHSIC Program started March 1980, during the next 10-years funded about $918M for 1.25 micron and 0.5 micron semiconductor development



Honeywell VHSIC Program
Phase 1

- A team of Honeywell & Motorola won 1 of 6 VHSIC programs
- Honeywell Solid State Electronics Division (Plymouth, MN) was the VHSIC technology developer
- Developed 3 VHSIC Process Technologies
  - 1.25 Micron ADB-3 Bipolar
  - 1.25 Micron CMOS-3
  - 1.25 Micron RiCMOS-3 (Radiation Hard CMOS)

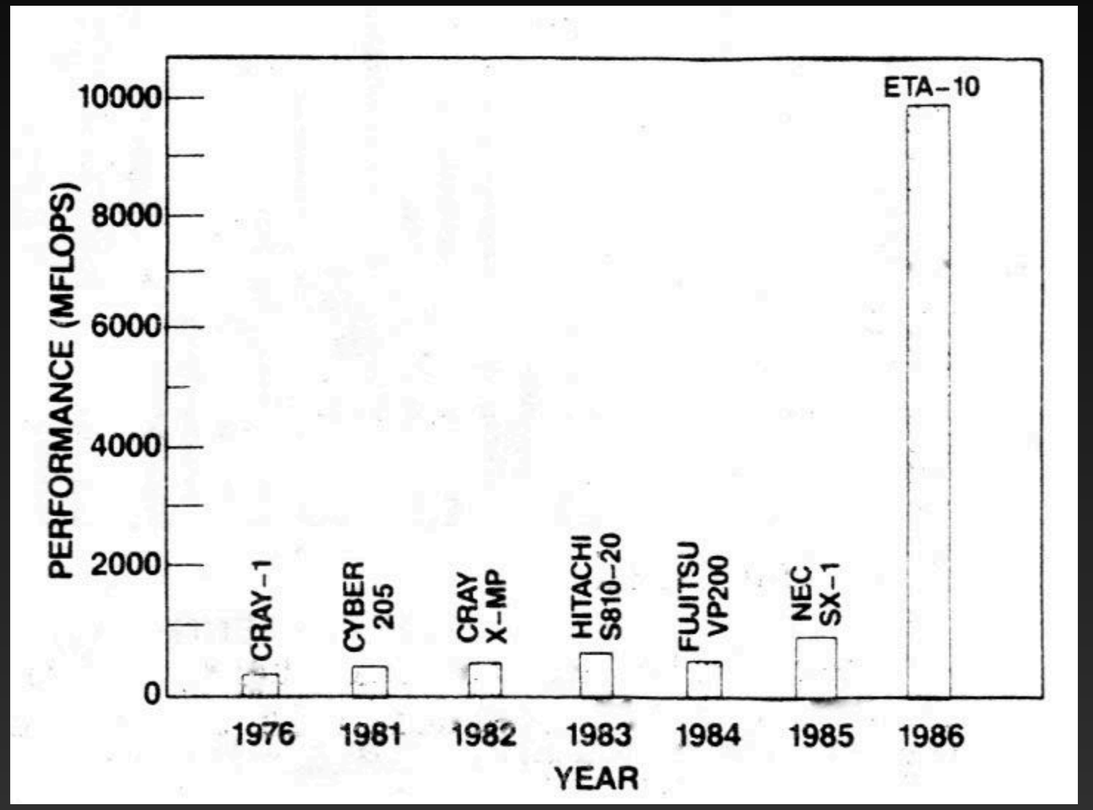


Honeywell 1.25 Micron Bipolar CML Parallel Processor Chip with TAB Leadframe, Pin Grid Array Package (Smithsonian Museum)

ETA systems logo

ETA 10 Development Activity

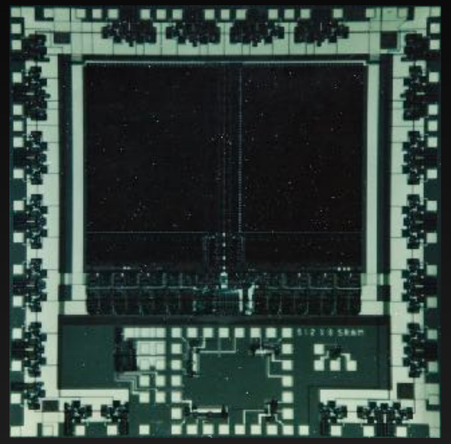
- In 1981, Control Data had just released the Cyber 205 Supercomputer
- CDC Advanced Design Lab began planning the next machine
  - Key players - Neil Lincoln, chief architect, Tony Vacca, chief technologist
- CDC needed fast development of a much faster & cheaper supercomputer due to competition from Cray Research and several Japanese companies
- Initial approach - Evolutionary 8K gate ECL Gate Array developed by CDC for a Motorola Bipolar process
- Neil Lincoln and his architecture team quickly determine Bipolar ECL too low density, high power, and too expensive to meet their goals

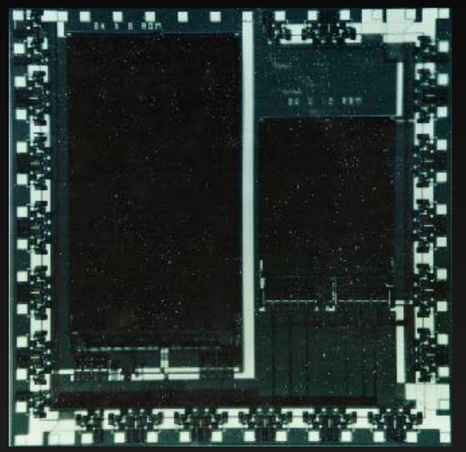


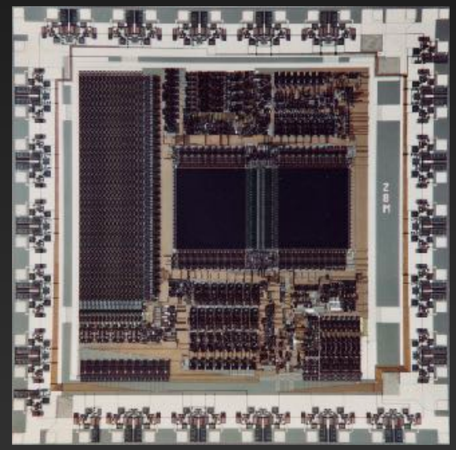
Supercomputer Performance 1980s

Honeywell VHSIC CMOS Activity

- At Honeywell Solid State Electronics (Plymouth), several VHSIC developments were underway
  - Bipolar Parallel Signal Processor (3 chips) - ADB-3
  - VLSI-6 16-bit Minicomputer on Chip - CMOS-3
  - Z-8 Microprocessor Macrocells for Custom Honeywell Residential Products - CMOS-3
- I was Design Manager the for Z-8 Microprocessor project team
- At CDC, Randy Bach was Project Engineer on a CMOS chip being developed for CDC Canada in 3 micron CMOS
- I present results of our Z-8 development program at an IEEE lunch meeting to several members of ETA team
- ETA Decided to implement ETA-10 using Honeywell VHSIC CMOS-3 Gate Array with 20K Gates operating at Liquid Nitrogen Temperatures (-300 Degree F)







Z-8 Microprocessor Macrocells

ETA systems logo

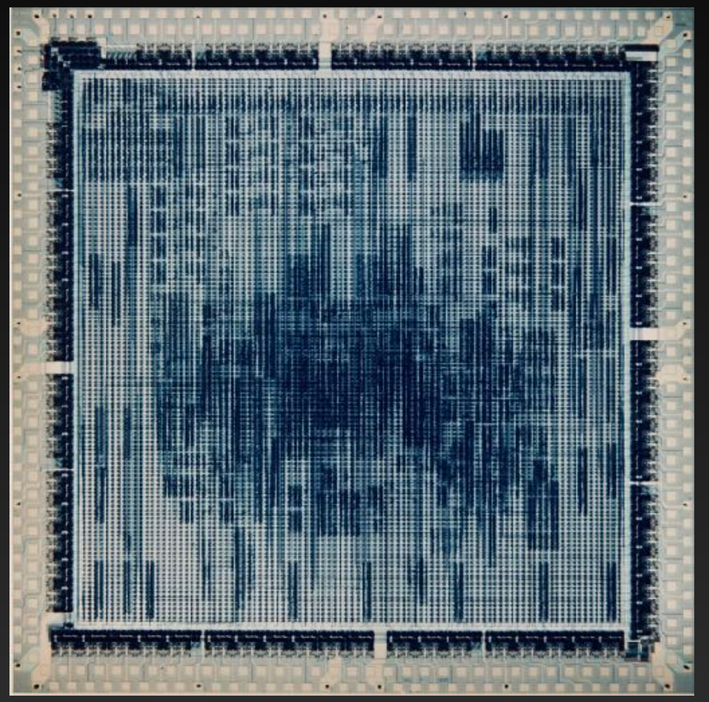
ETA-10 Program Results

- First Industry High Performance CMOS CPU
- First Industry Single Board Supercomputer CPU
- First Built-in Self-Test Computer
- First Industry Production Liquid Nitrogen CPU (and Only to Date)
- First CDC System to Use CAD for Chips, Boards, Logic Design, Test
- Multiple Price Points From Single Design

ETA10 Models	P	Q	E	G
Cycle Time (ns)	24	19	10.5	7
#Processors	1-2	1-2	1-4	2-8
CPU Memory MB/CPU	32	32	32	32
Shared Memory MB	64-512	64-512	256-1024	512-2048
Peak Performance MFLOPS	750	947	3429	10289
Cooling	Air	Air	Liquid Nitrogen (LN2)	Liquid Nitrogen (LN2)
Maximum I/O Units	4	4	9	16

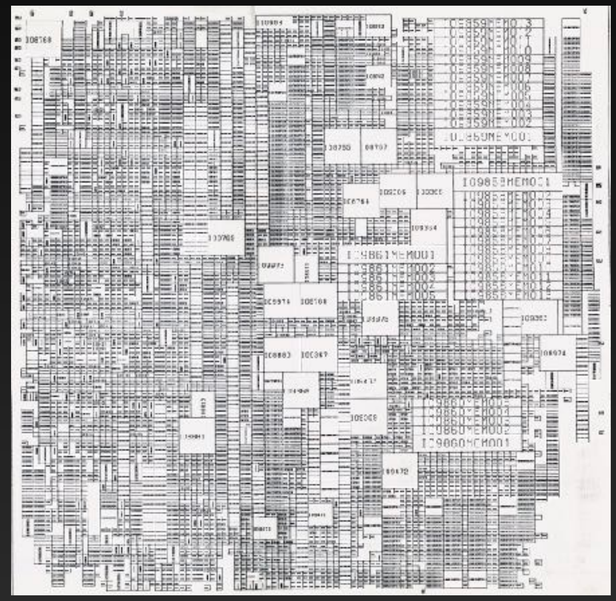
CPU Logic

- 1 cm 20K Gate 1.2 Micron CMOS Gate Array
- 284 I/O pads with solder bumps
- Effective 5 mil TAB Lead Pitch
- 2 input NAND Delay 860 ps room temp, 480 ps at -300 F
- Built-in Self-test for both Chip and Board Interface
- Parametric Cell Library for High Gate Utilization



20K Gate Array

284 I/O Pins



Placement Diagram Shows Parametric Cells

Built-In Self-test

- BIST Logic Added to Chip I/O
- Chip Test - Generates Own Test Operands and Calculates Test Signature for Automatic Logic Test
- Parametric I/O Test - All I/O can be set on or off, tristate on or off
- Wiring Tests - Test Operand entered on all chips and sent to all receiving chips, tests wiring for opens, shorts, grounded lines, etc.

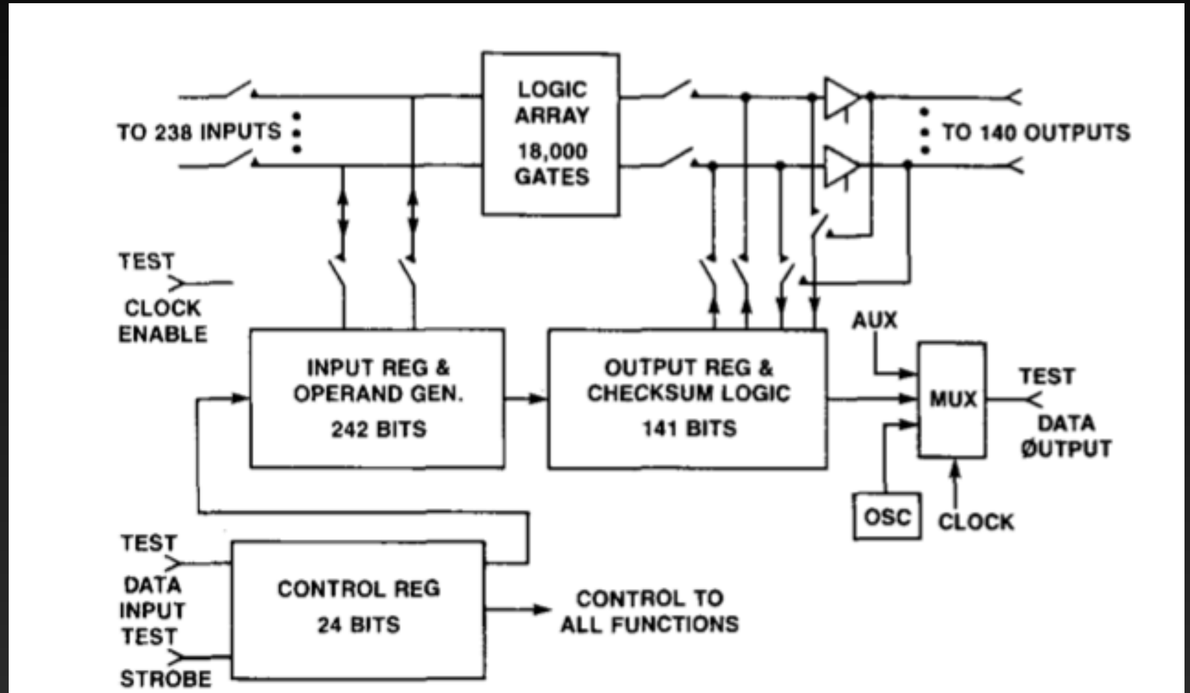
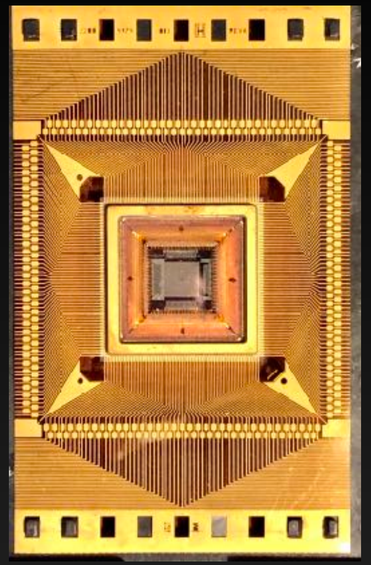


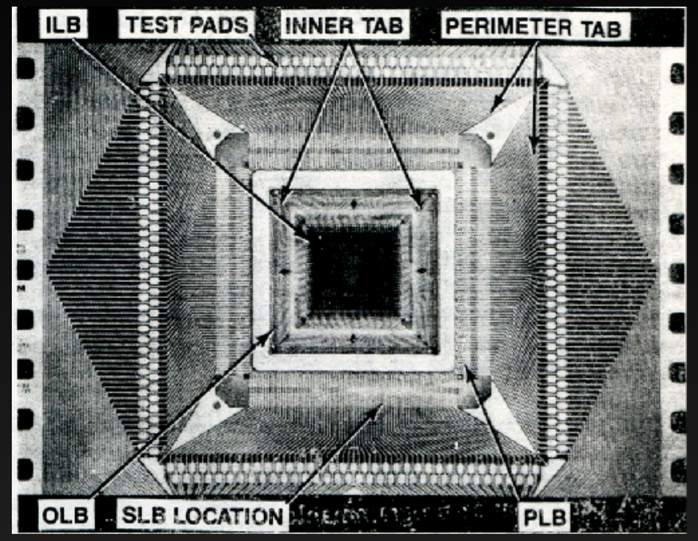
Fig. 2. Logic used for the built-in evaluation and self-test. The four pins labeled "TEST," the three blocks labeled "REG," and the output "MUX" are all dedicated to the test logic function.

Logic Packaging

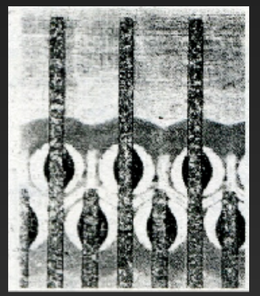
- Ceramic Chip Carrier with 11 mil Tape Automated Bonding (TAB) to Board Connection
- TAB Die Attachment to Package (5 mil Pitch)
- Solder Bumps on 20K Chip



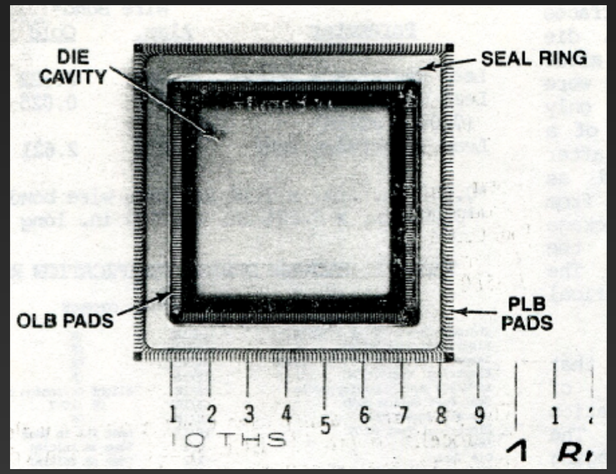
TAB Lead Frame



Perimeter & Inner TAB



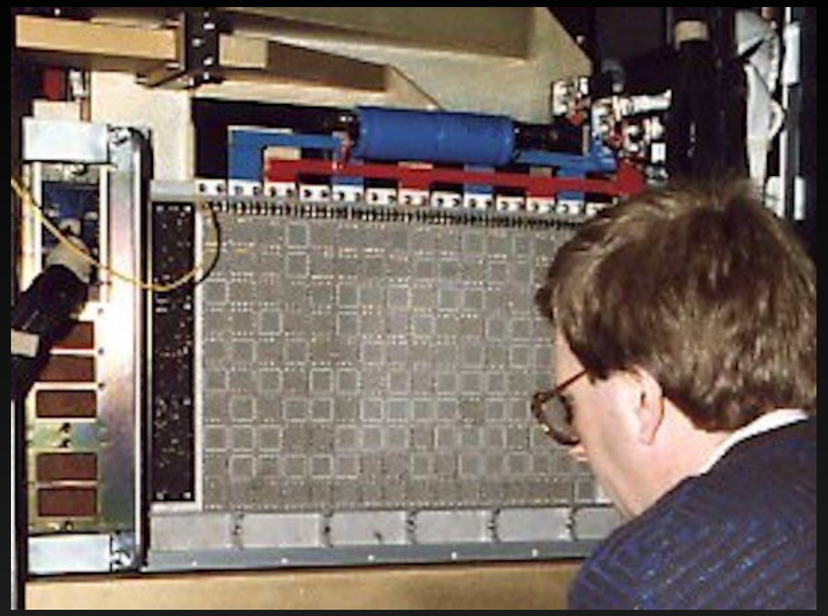
TAB to Solder Bumps



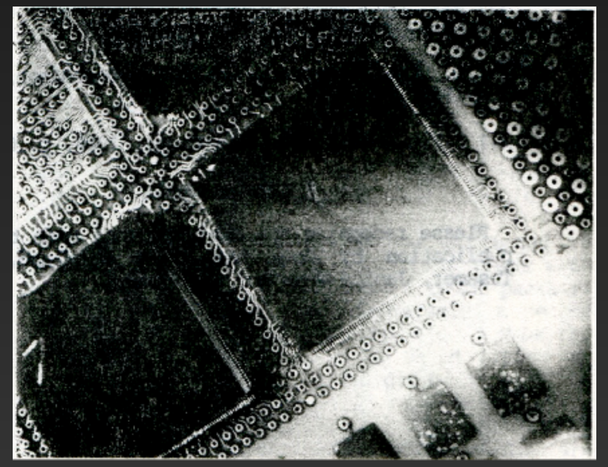
Chip Carrier w 11 mil Pitch

Single Board CPU

- ETA 10 Mounts 280 20K Chips On Single Board
- 16.5 x 22.5 x0.250 inch FR4 PCB
- 44 Layers (20 Signal, 22 Power, 2 Surface)
- 75,000 drilled through-board via
- 50,000 buried vias



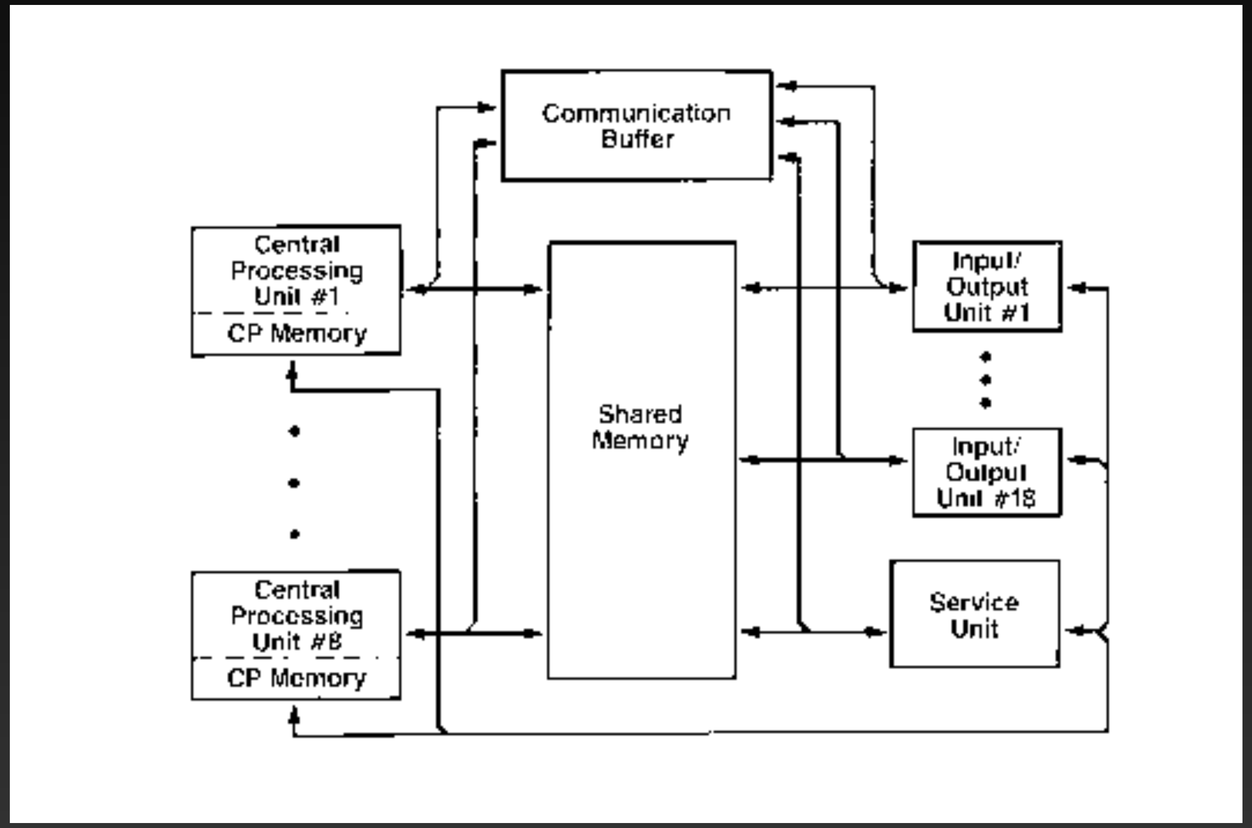
45-Layer CPU Board Supports 260 Chips



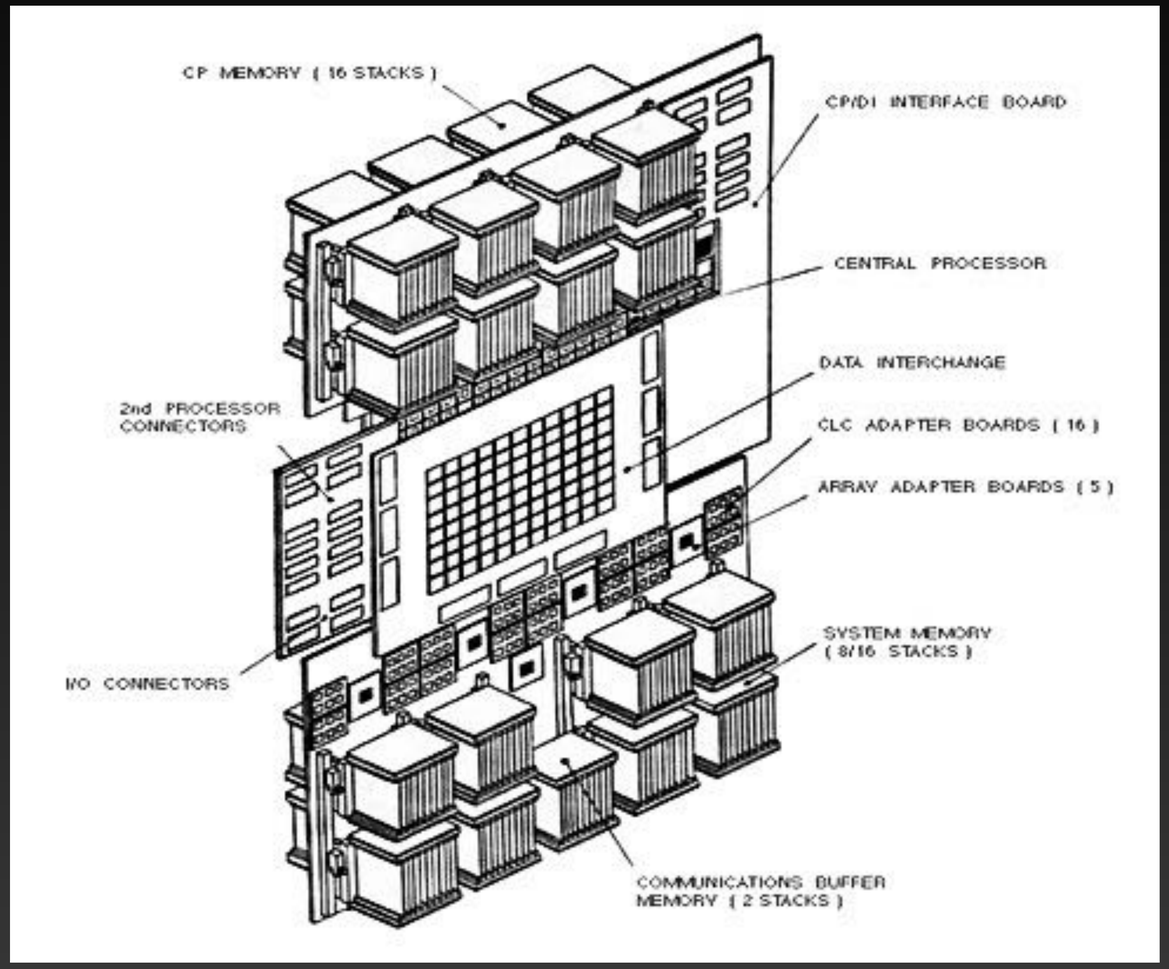
Chip Carrier on Board

System Level Design

- The ETA-10 System Architecture Consisted of:
  - 1-8 Single Board CPUs with Local CPU Memory/CPU
  - Shared Memory Between CPUs
  - 1-16 I/O Units
  - Communication Buffers
  - A Service Unit



System Configuration



Cryogenic Systems

- For Cryogenic CPUs, CPU Boards were mounted in Cryostat which contain 2 CPU
- Significant Plumbing and a Separate Cryogenerator was Required to Distribute Liquid Nitrogen at -300 Degrees F

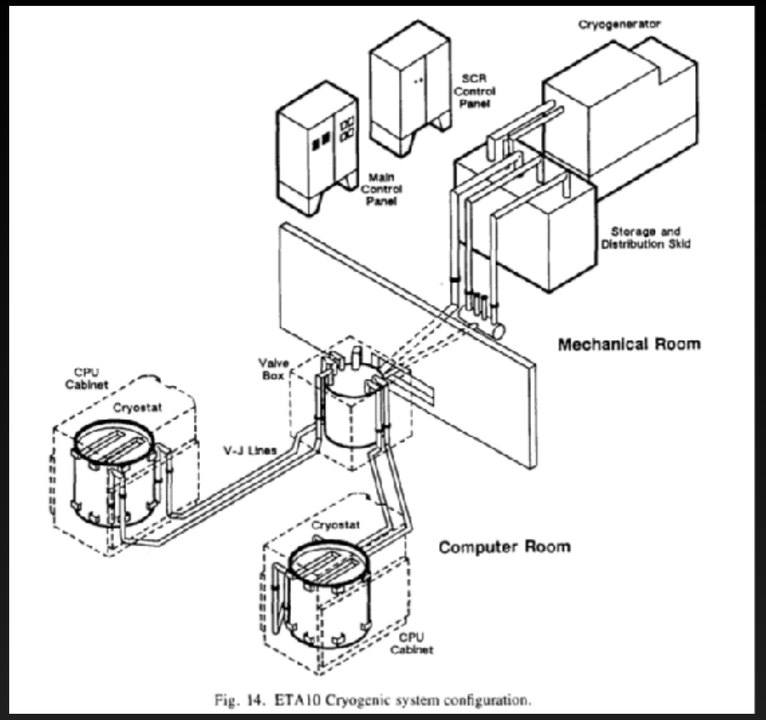
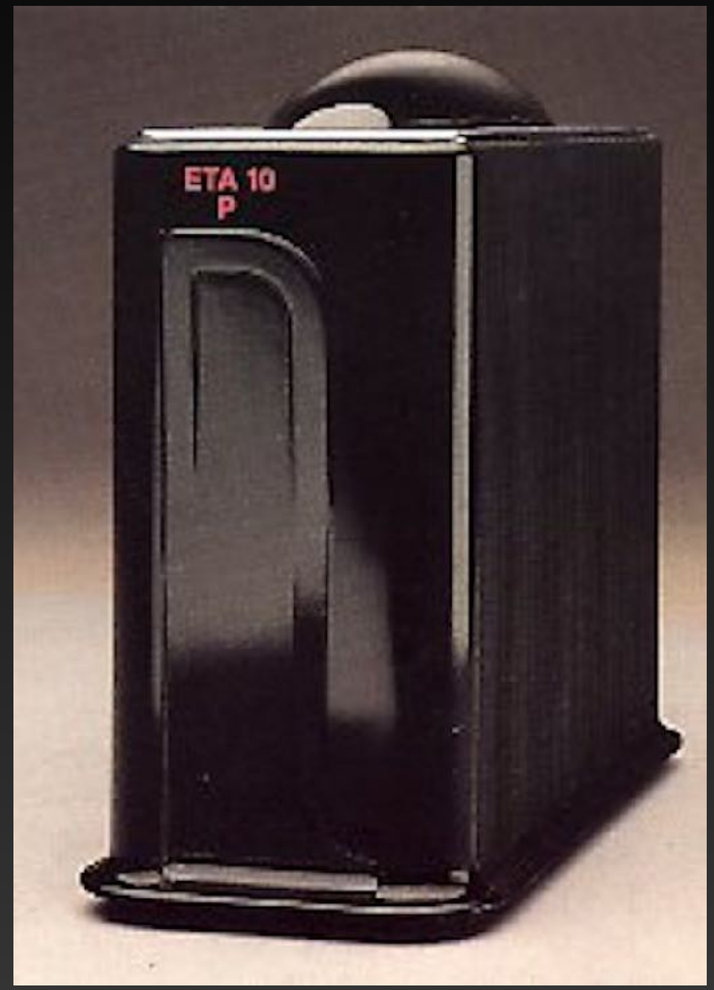


Fig. 14. ETA10 Cryogenic system configuration.

Final ETA-10 Systems

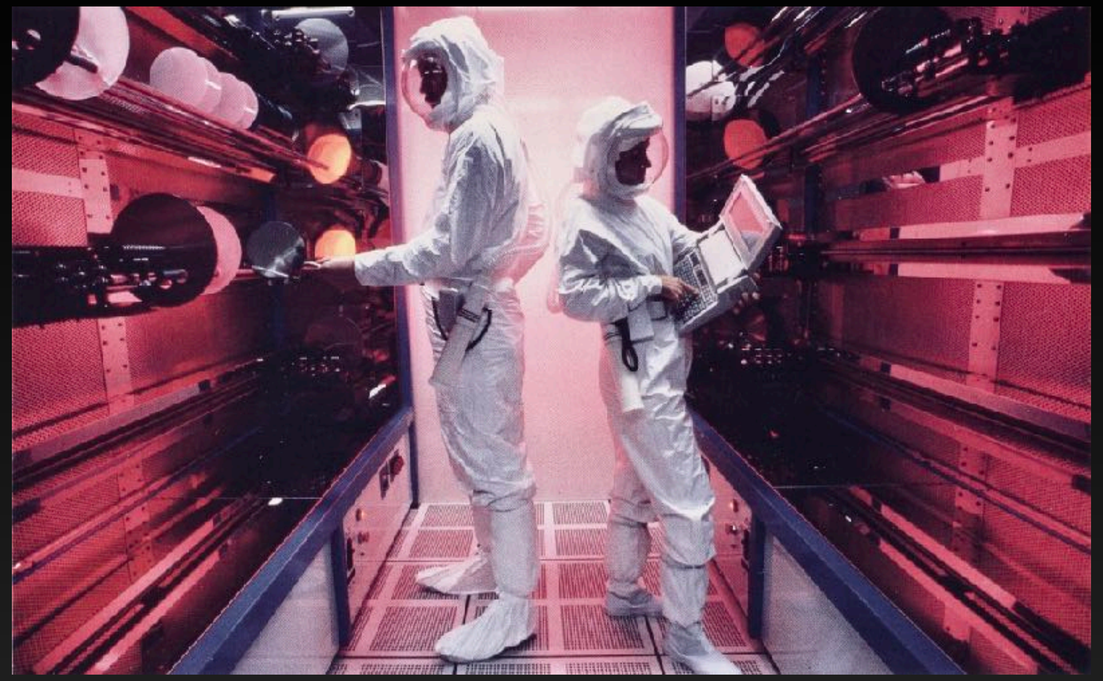
Cryogenically Cooled 7 ns ETA-10G

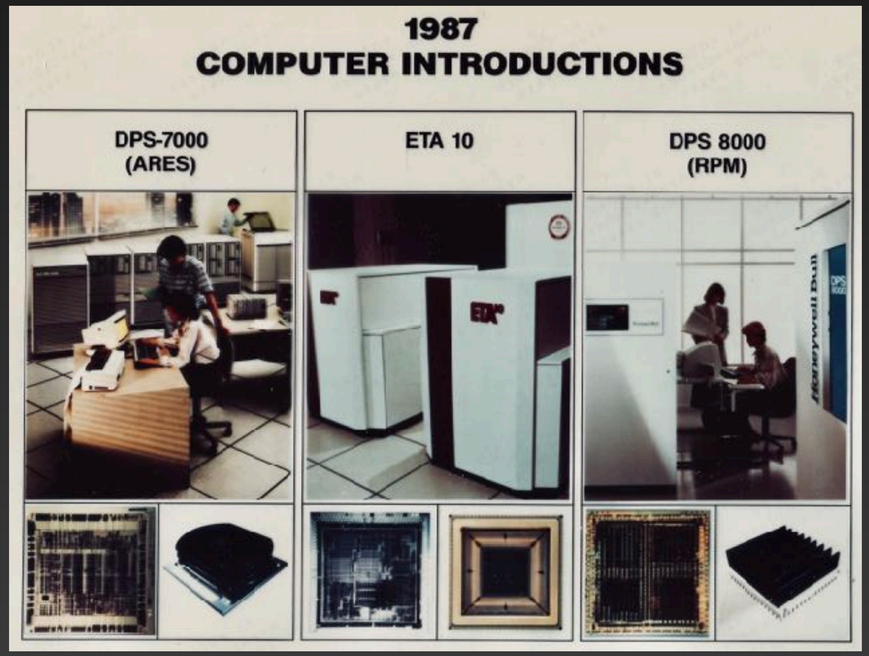


Air-cooled 24 ns ETA-10P

VHSIC Manufacturing

- Honeywell built the world’s first VHSIC manufacturing facility in Colorado Springs, CO by 1986
- Honeywell built 300 unique 20K gate array types for the ETA-10
- VHSIC Technology was also designed into the Honeywell DPS8000 and Honeywell Bull DSP-7000 mainframes
- Honeywell Digital Technologies recorded $62M Revenue from VHSIC Sales in 1987
- Honeywell was 8th largest ASIC Supplier in the world in 1987





Postscript

- A total of 27 ETA-10 Systems were sold (7 LN2 cooled, 20 Air-cooled) including:
  - Florida State University (SN#1, LN2)
  - Johnson Space Center
  - John von Neumann Center
  - Tokyo Institute of Technology (8 CPU, LN2)
  - Deutscher Wetterdienst, German Weather Service
  - UK Meteorlogical Service (UKMET)
  - Minnesota Supercomputer Center
- Key Problem with ETA-10 was late delivery of Unix OS
- On April 14, 1989, CDC Closed ETA Systems

Mekonnen, Kristiansen win the Boston Marathon/1C

4,000 to scrub up spill/3A

VARIETY
Heirs to Michelangelo
Atelier Lack art students learn a rich tradition

VARIETY
Mystery of the Bard
Holston examines 'Frontline' documentary

STATE EDITION
Brainerd couple are charged with neglect of baby who died/1B
Duluth voters to consider largest school bond issue in state's history/3B

Star Tribune

TUESDAY/ April 18/1989 NEWSPAPER OF THE TWIN CITIES

CDC fires 3,100, closes ETA

More than half of lost jobs in Twin Cities

By Steve Gross
Staff Writer

Control Data Corp. shrunk its money-losing computer operations Monday by terminating 3,100 people, taking a $490 million one-time charge and closing its ETA Systems supercomputer subsidiary in St. Paul. More than half of the dismissals will occur in the Twin Cities.

Yesterday's major cutback followed a long series of financial problems at Control Data that have resulted in cumulative net losses of nearly $806 million since 1984.

Securities analysts said, however, that yesterday's dramatic cutbacks will not by themselves rescue Control Data from its depressed financial condition. To do that, Control Data must become a smaller company and raise additional money by selling assets, they said.

John Buckner, chief financial officer, said yesterday that Control Data would sell some "non-major assets," but he declined to say which businesses he meant. Yesterday's dismissals represented about 9 percent of Control Data's 33,500 employees. The company's work force has shrunk steadily since 1984, when it had about 54,000 workers. CDC's dismissal of about 1,500 Minnesota

Control Data continued on 10A

Staff Photo by Stormi Greener

Robert Price, chairman and chief executive officer of Control Data Corp., announced layoffs of about 3,000 employees Monday.

Japanese gain with loss of ETA

By Josephine Marcotty
Staff Writer

The demise of ETA Systems, the supercomputer subsidiary shut down Monday by Control Data Corp., means that Minnesota must relinquish to the Japanese the title of supercomputer capital of the world.

ETA and Cray Research, also based in the Twin Cities, have been the only two U.S. companies in the fast-moving, high-stakes supercomputer industry. Although IBM may become a significant player in a few years, the only three other supercomputer companies in the world are based in Japan.

While ETA has always been a distant runner-up to the power of Cray, ETA's demise represents the loss of a combatant in the technology war between the United States and Japan.

"It is a blow to the whole effort to make the U.S. competitive in leading-edge technologies," said Gary Smaby, an analyst with New York-based Needham & Co. of CDC's action yesterday. "Our fortunes now are riding with IBM and Cray. We've lost one contender to keep us in the game."

Control Data launched ETA in 1983, vowing to develop front-line comput-

ETA continued on page 11A