Who Needs a Unique Registration Number?

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IEEE 1451.4 TEDS data is stored in one or more independently addressable memories, called nodes. Nodes may also contain functions other than memory.

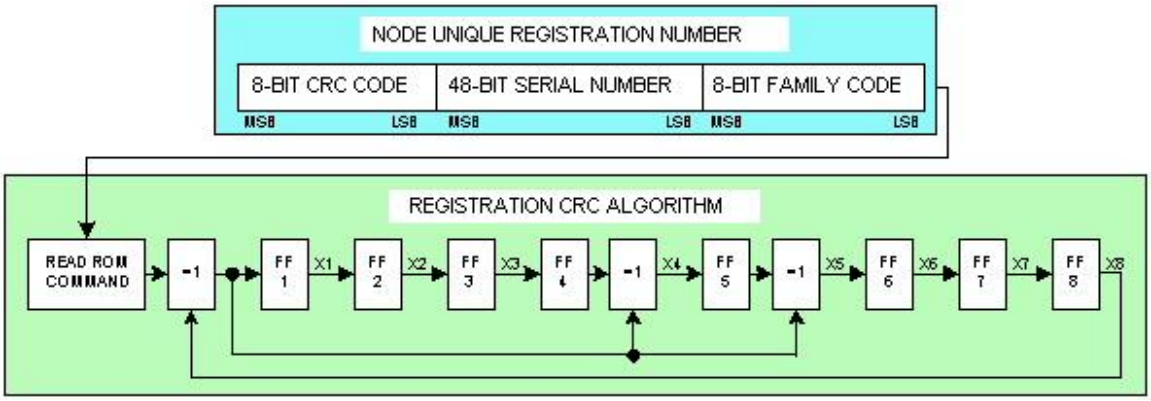
Each node must contain a permanently stored 64-bit unique registration number (URN), used to control access to the TEDS memory. The URN is the basis upon which node-addressable, digital communication takes place, within the multi-drop architecture of the IEEE 1451.4 Mixed Mode Interface. The URN contains an 8-bit family code to identify the functions available in the node and the command set to be used with the node. A 48-bit serial number and 8-bit cyclic redundancy check code (CRC) are also contained in the URN. The CRC allows several nodes in a multi-drop architecture to be identified and uniquely addressed.

The URN may be read from the node least significant bit (lsb) first using the *Read ROM* command. The first eight bits read from the 64-bit URN contain the family code of the node, lsb first, followed by the 48-bit unique serial number and then by the CRC code. The cyclic redundancy check is generated by a shift register punctuated by XOR functions, as illustrated below, to generate the CRC polynomial "$X^8 + X^5 + X^4 + 1$". Starting with the shift register cleared to zero, shifting the family code and serial number (the first 56 bits) into the register will result in register contents equal to the CRC byte value. Continuing to shift the 8-bit CRC byte into the register will clear it to zero, if no read errors have occurred. A non-zero result indicates that a data error has occurred.

CRC errors are most often due to data collisions between two (or more) nodes transmitting simultaneously, as they reply to a *Read ROM* command. The wired-AND nature of the bus will give priority to logic state 0. This is the basis of the *Search ROM* command, in which nodes return one bit of the URN at a time, followed by its complement, to the master. Should data and complement values both be zero, the master can only surmise that two (or more) nodes are present, with unequal values for that bit. The master then sends either a one or a zero, and the node(s) not matching that value, for that bit, drop into an inactive mode, awaiting reset. Continuation of this bit-by-bit elimination process inactivates all but one node, after all 64-bits have been polled.

Additional information on the use of the CRC may be found in the literature for the *Maxim/Dallas Semiconductor iButton Protocol*. [i]

Figure 1 URN bit map and CRC generation



All IEEE 1451.4 transducers storing TEDS data in the transducer and transmitting that data on the mixed mode interface (MMI) must use a node(s) containing a URN(s).

Most often, a transducer manufacturer will choose a commercially available memory node device for installation in a product and this will contain the URN, as delivered from the device manufacturer. [ii] Transducer manufacturers desiring to implement custom node designs, by utilizing a micro-controller program or ASIC, for example, must also install a URN into the design. Each device must have a separate URN, guaranteeing unique access to each node. Unique registration numbers are available for purchase in blocks of 4096, by contacting the IEEE Registration Authority. [iii]

Unique registration numbers purchased from the IEEE are supplied in blocks of 4096 individual numbers, between the hexadecimal values of 0 hex and FFF hex. The bit map for IEEE URN codes is detailed below. The family code always contains the value FD hex (1111 1101 binary). The block number occupies 36 bits, allowing up to 68.7 billion blocks to be assigned. Each block contains 4096 individual serial numbers to be assigned to as many devices, represented by 12 bits and hex codes from 0 through FFF. In the most significant byte is the CRC code.

Figure 2 IEEE Std 1451.4 URN Bit Map

MS bit LS bit

CRC code (8 bits)	Serial Number (12 bits)	Block Number (36 bits)	1451.4 Family Code (8 bits)
0-FF hex	0-FFF hex	68.7 billion blocks available	FD hex

[i] *Book of iButton Standards*, Maxim/Dallas Semiconductor, Appendix 1, pp.125-129, edition 08-12-97.
[ii] Data Sheet, "DS2430A 256-Bit 1-Wire EEPROM," Maxim/Dallas Semiconductor, p.2, edition 02-20-02.
[iii] C/O IEEE Standards Association, 445 Hoes Lane, PO Box 1331, Piscataway, NJ 08855-1331, USA, or at www.standards.ieee.org