

# The 10BASE-T1S OA3p Interface

Enabling Advantages for the All-Ethernet Vehicle



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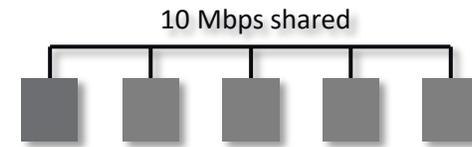
SMART | CONNECTED | SECURE

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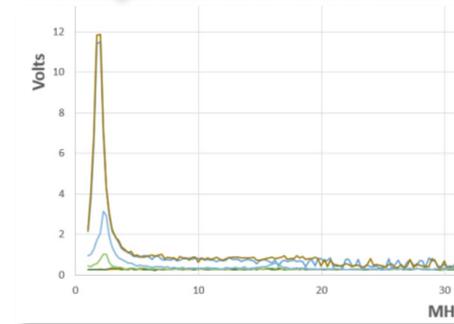
# 10BASE-T1S

## A Short Refresher

- **Ethernet on a UTP bus line**
  - 10 Mbps shared
  - Half-duplex
  - 2 to at least 8 nodes
  - Up to at least 25 m
  - No collisions
- **Reflections due to multidrop**
  - High common mode voltages
  - Requires high voltage process for semiconductors

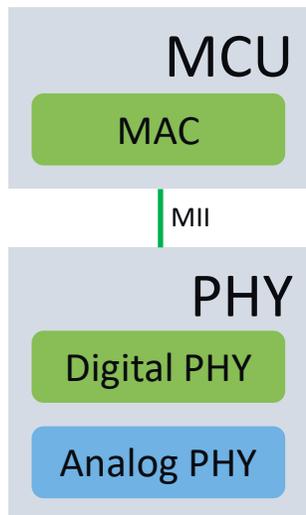


Voltages seen at different nodes

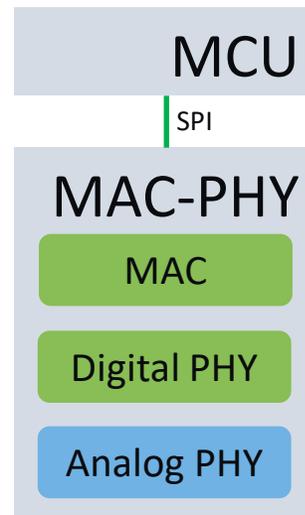


# Connectivity Options

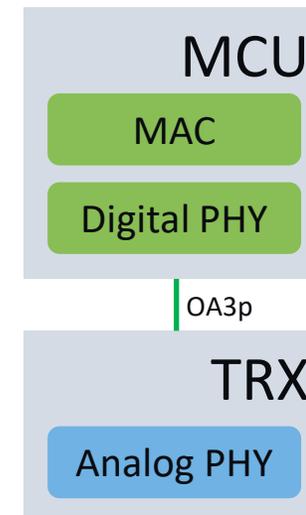
## Overview



Existing MCUs,  
Switches



Small MCUs

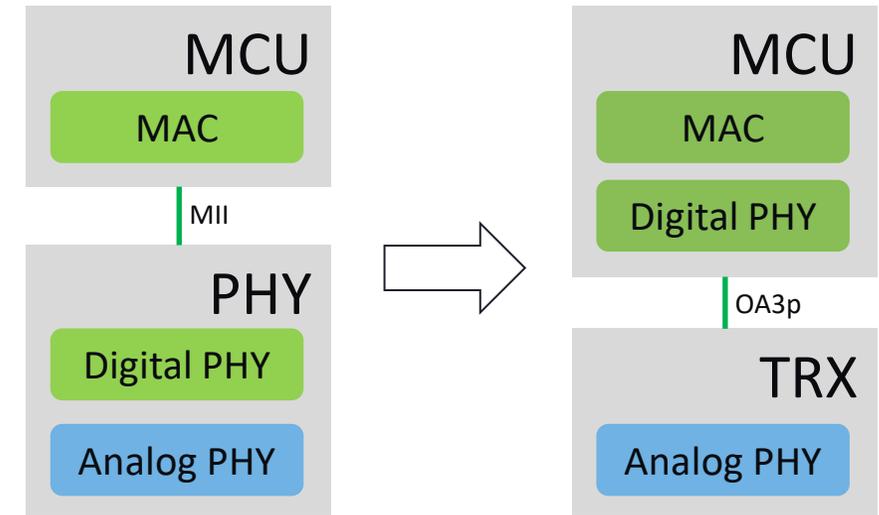


**New!**

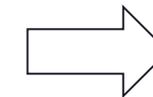
# Motivation for OA3p

## MII to OA3p

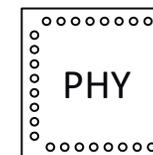
		PHY	TRX	Reduction
<b>Die Size</b>	Digital PHY PHY → MCU	e.g., 130nm	e.g., 40nm	<b>90%</b>
	MCU Pads for interfacing	18	3	<b>87%</b>
	PHY/TRX Pads	32	8	<b>75%</b>
<b>Form Factor</b>	Pins	32	8	<b>75%</b>
	Package / PCB real estate	5x5 mm <sup>2</sup>	3x3 mm <sup>2</sup>	<b>64%</b>
	Crystal	needed	-	<b>100%</b>
<b>Power Consumption</b>	Digital PHY PHY → MCU	Pads 3.3V Digital 1.8V	1.0V	<b>Up to 75%</b>



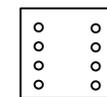
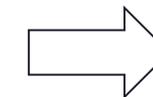
130nm



40nm



PHY



TRX

# 10BASE-T1S Digital PHY

## Functions and Integration

- **Functions**

- PLCA Physical Layer Collision Avoidance
- PCS Physical Coding Sublayer
- PMA Physical Media Attachment
- TC10 Wake/sleep management

- **IEEE compliance**

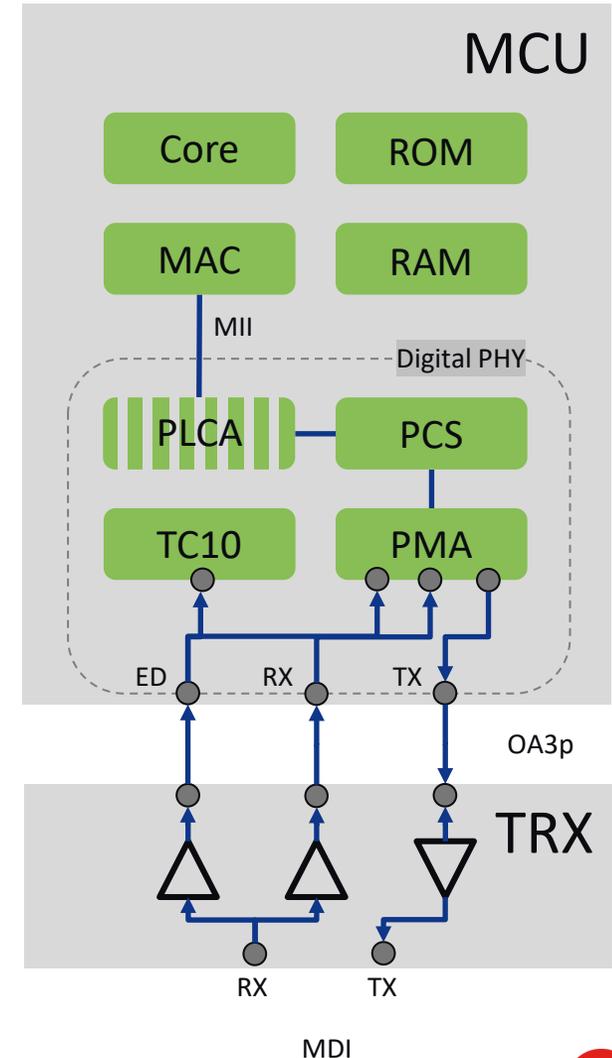
- No new/additional logic in digital PHY
- Only signal amplification and level comparison in TRX
- No storage/logical treatment of signals from PMA to MDI

➤ Fully IEEE compliant at MII and MDI

- **Objective**

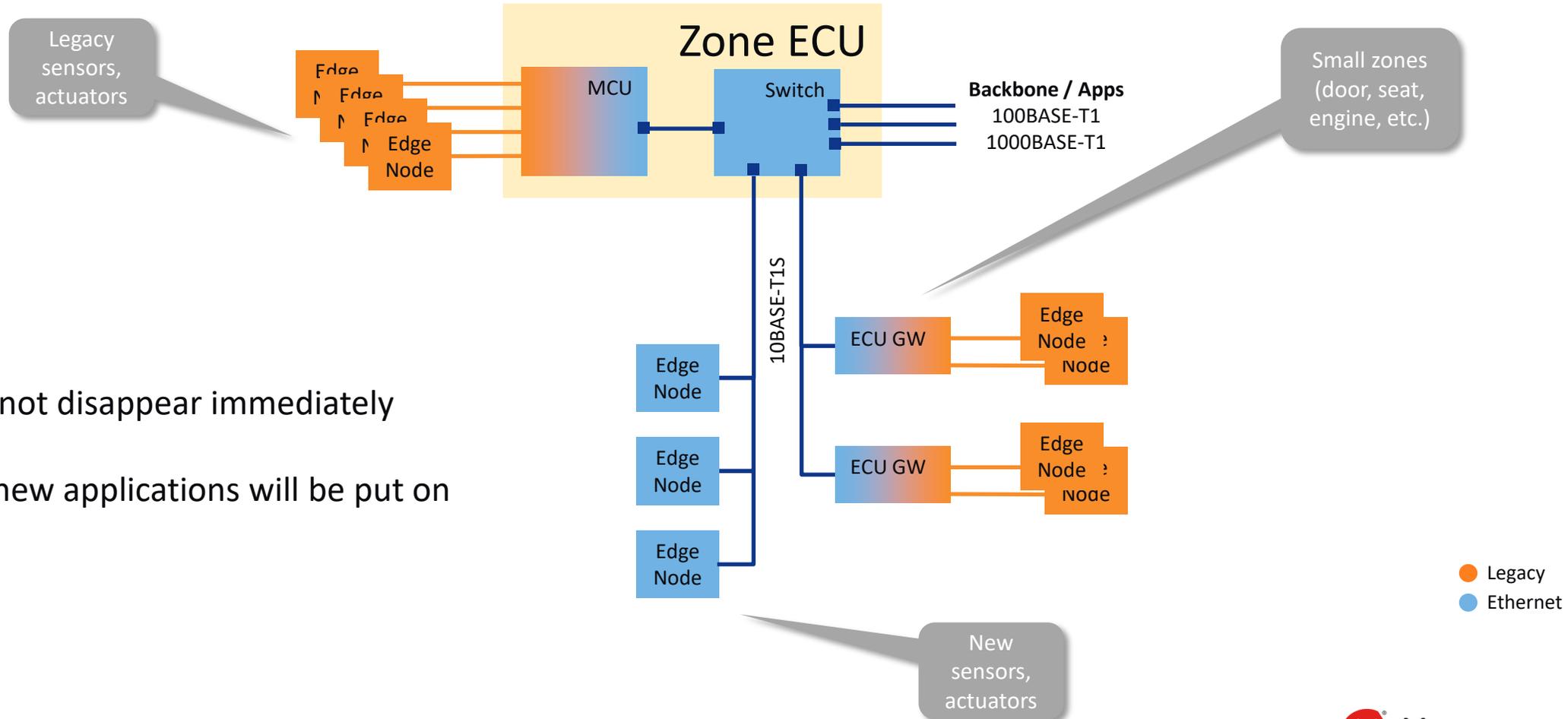
- Pure digital IP → Easy integration in all processes

➤ Fast technology rollout in MCUs and switches



# 10BASE-T1S in Zone Architecture

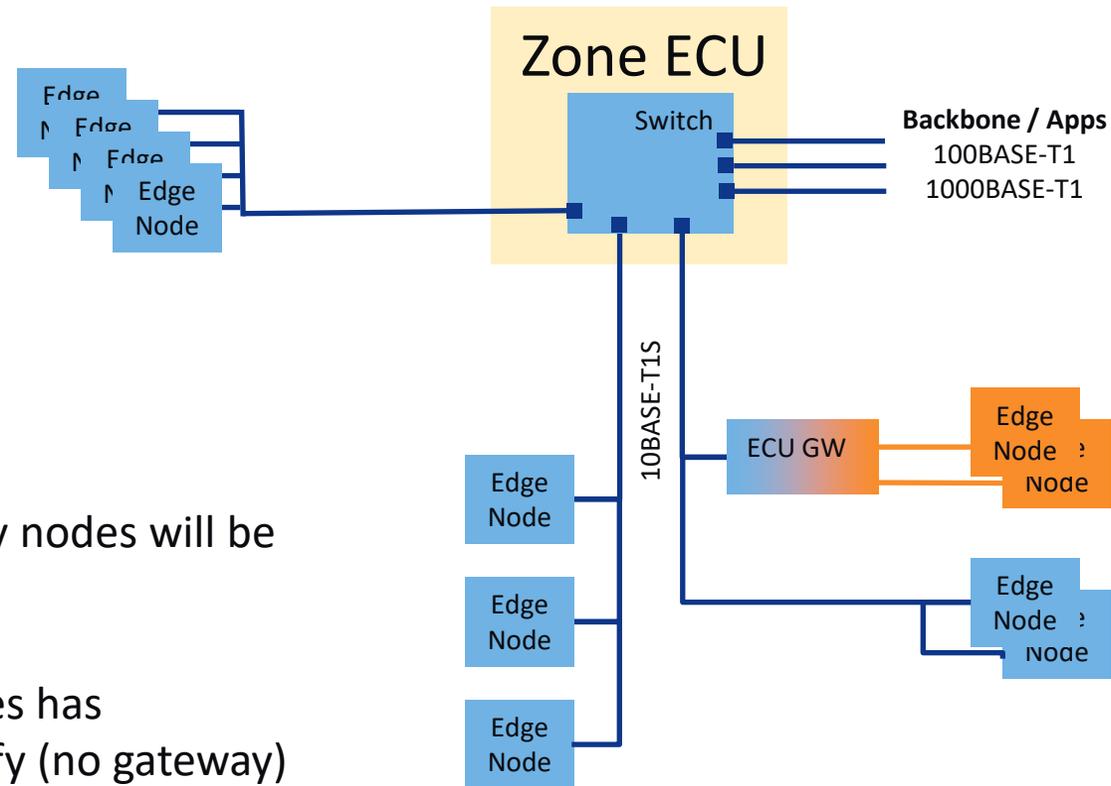
## The Path to an All-Ethernet Vehicle



- CAN/LIN will not disappear immediately
- Initially only new applications will be put on 10BASE-T1S

# 10BASE-T1S in Zone Architecture

## The Path to an All-Ethernet Vehicle



- Over time more and more legacy nodes will be replaced with Ethernet nodes
- Once the number of legacy nodes has decreased Zone ECUs will simplify (no gateway)
- Where legacy is still needed local gateways will be used

# Why hybrid networks combining Ethernet and legacy message transmission won't work well in zonal architecture ...



# System Without Switch

## Two Networks on a Single Physical Layer

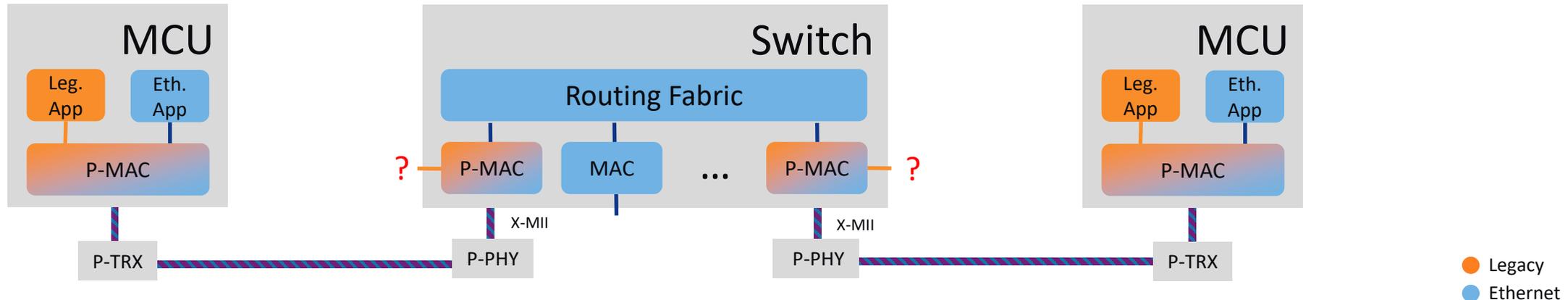
- Use existing control communication
- Keep message catalogs
- Keep infrastructure, tools, etc.
- Experts don't need training
- Keep ECU software
- Works for legacy architecture
- Requires special MAC



P-MAC: Proprietary MAC supporting Ethernet and legacy Data Link Layer

# System with Ethernet Backbone is Problematic

- Requires proprietary MACs in switches → no easy adoption in switches
  - P-MAC could have a gateway function → same as if MCU uses Ethernet
  - No system specifications for clock synchronization, security, safety, prioritization, etc. → needs to be written by OEM
- **Not really suitable for zone architecture**



P-MAC: Proprietary MAC supporting Ethernet and legacy Data Link Layer

# Wake/Sleep

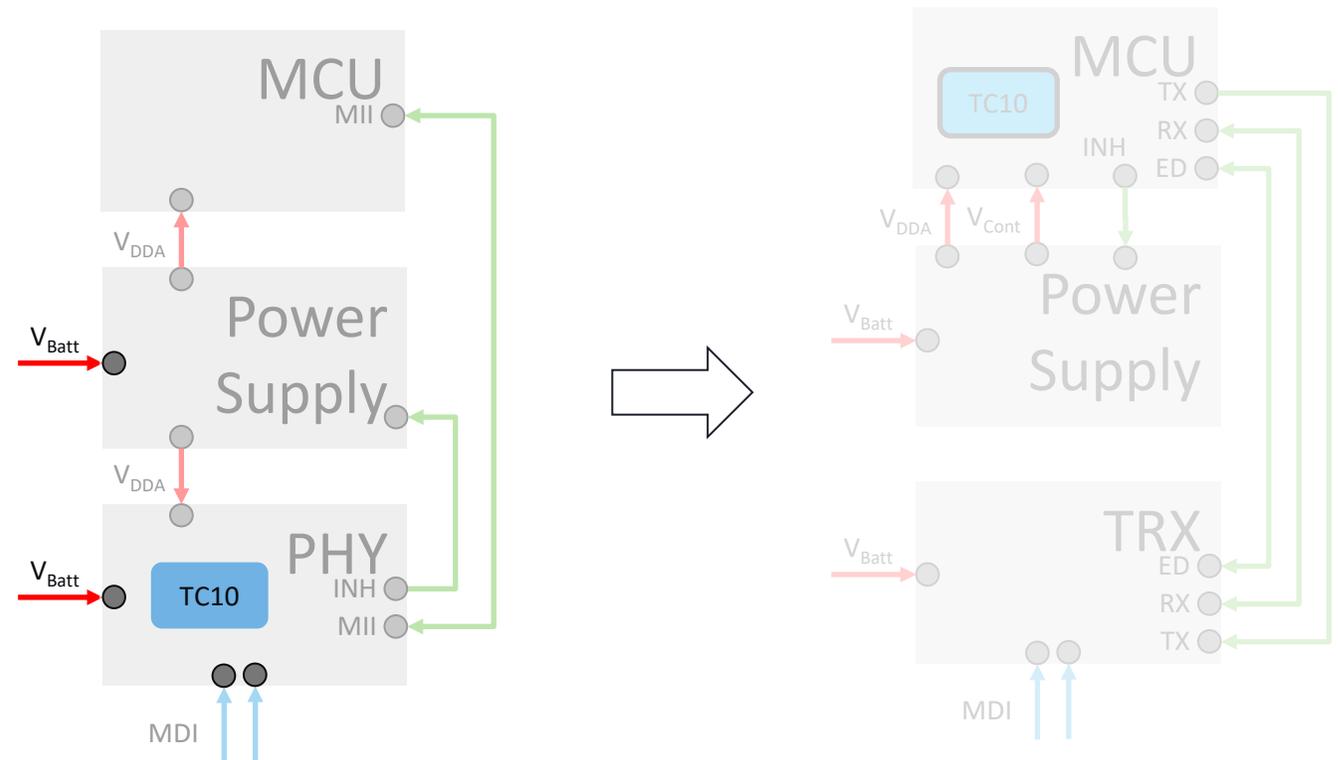
## How the OA3p Affects the Board Design

- **Standby mode defined for TRX**
- **ED pin (Energy Detect) provides line activity indication**
- **There is a significant difference to a PHY-based architecture**

# Wake/Sleep

## Awaking PHY-Based Architecture

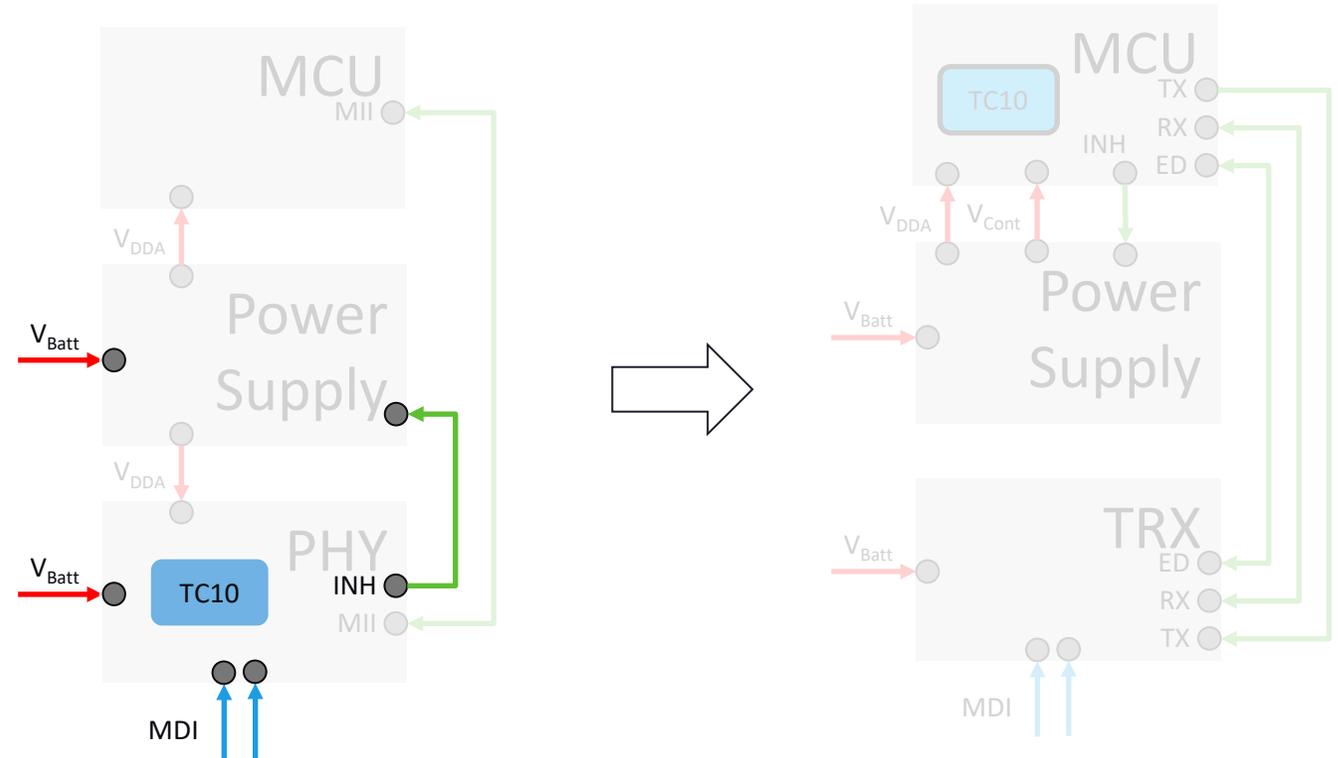
- **During sleep**
  - MCU off
  - Power supply off
  - PHY almost off. Only a block checking for a wake-up-pulse (WUP) on MDI is working.



# Wake/Sleep

## Awaking PHY-Based Architecture

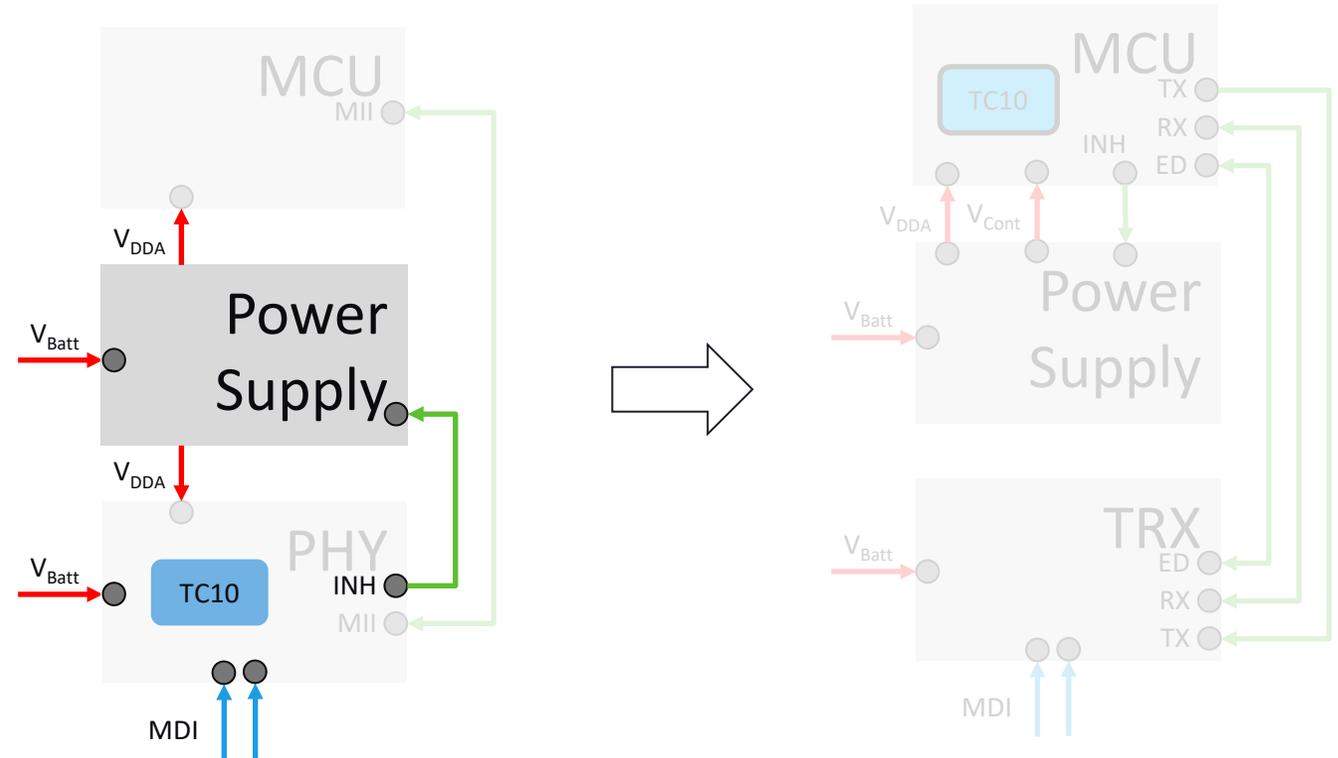
- **PHY detects WUP**
  - PHY toggles inhibit pin to awake power supply



# Wake/Sleep

## Awaking PHY-Based Architecture

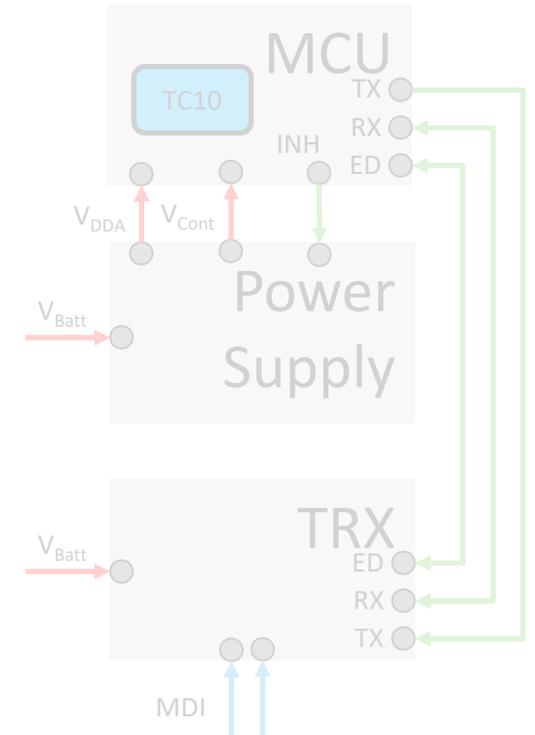
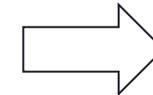
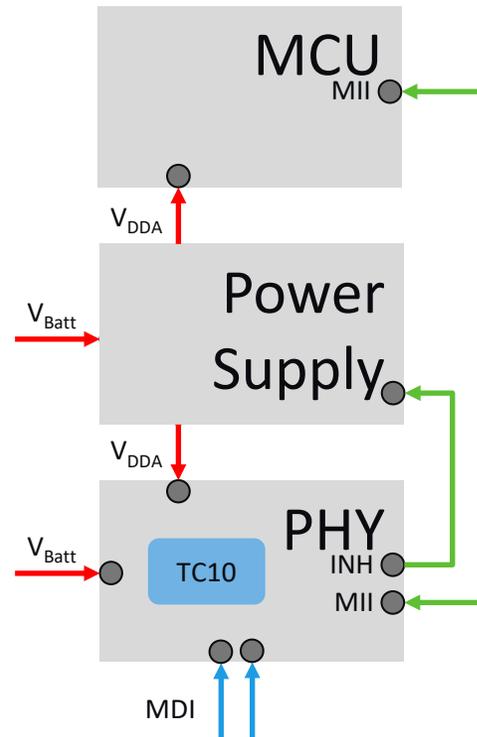
- **Power supply on**
  - Providing regulated power to MCU and PHY



# Wake/Sleep

## Awaking PHY-Based Architecture

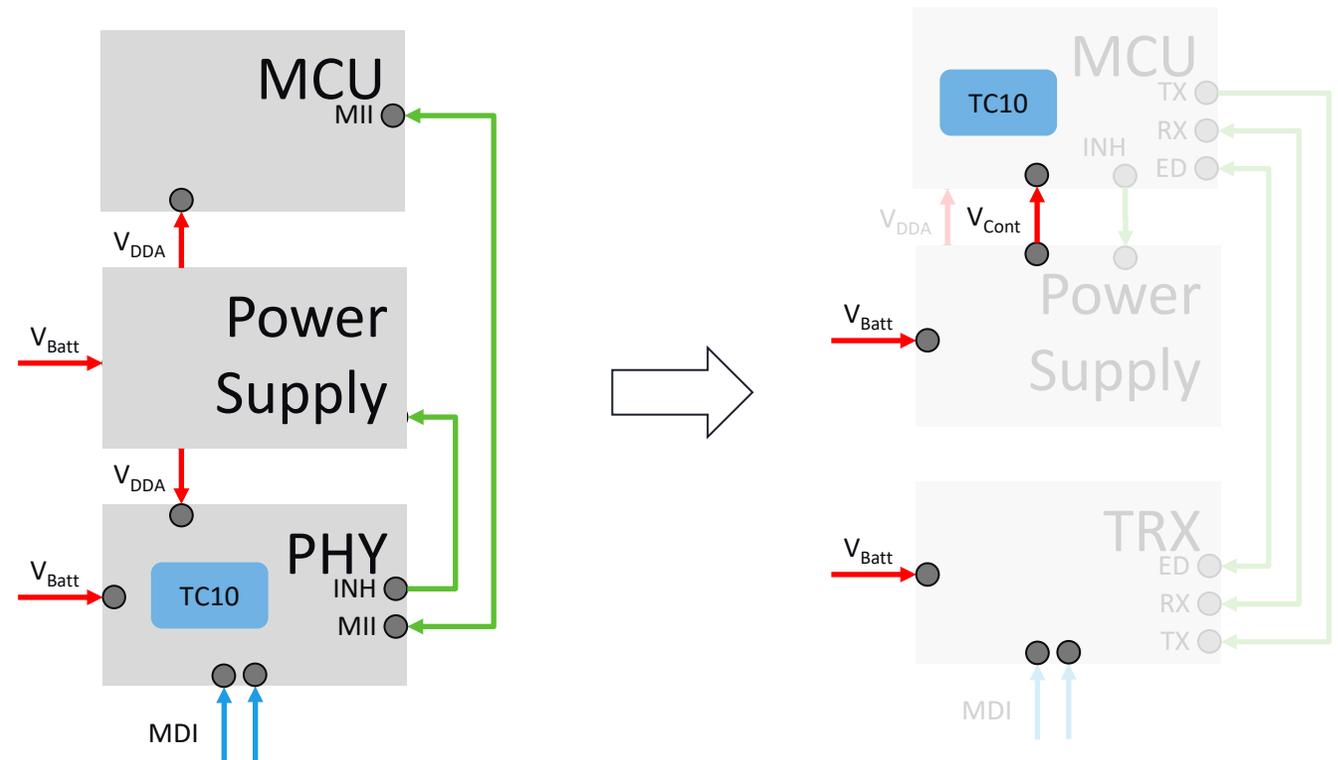
- **System powered**
  - MCU on
  - PHY on
  - Communication via MII



# Wake/Sleep

## Awaking TRX-Based Architecture

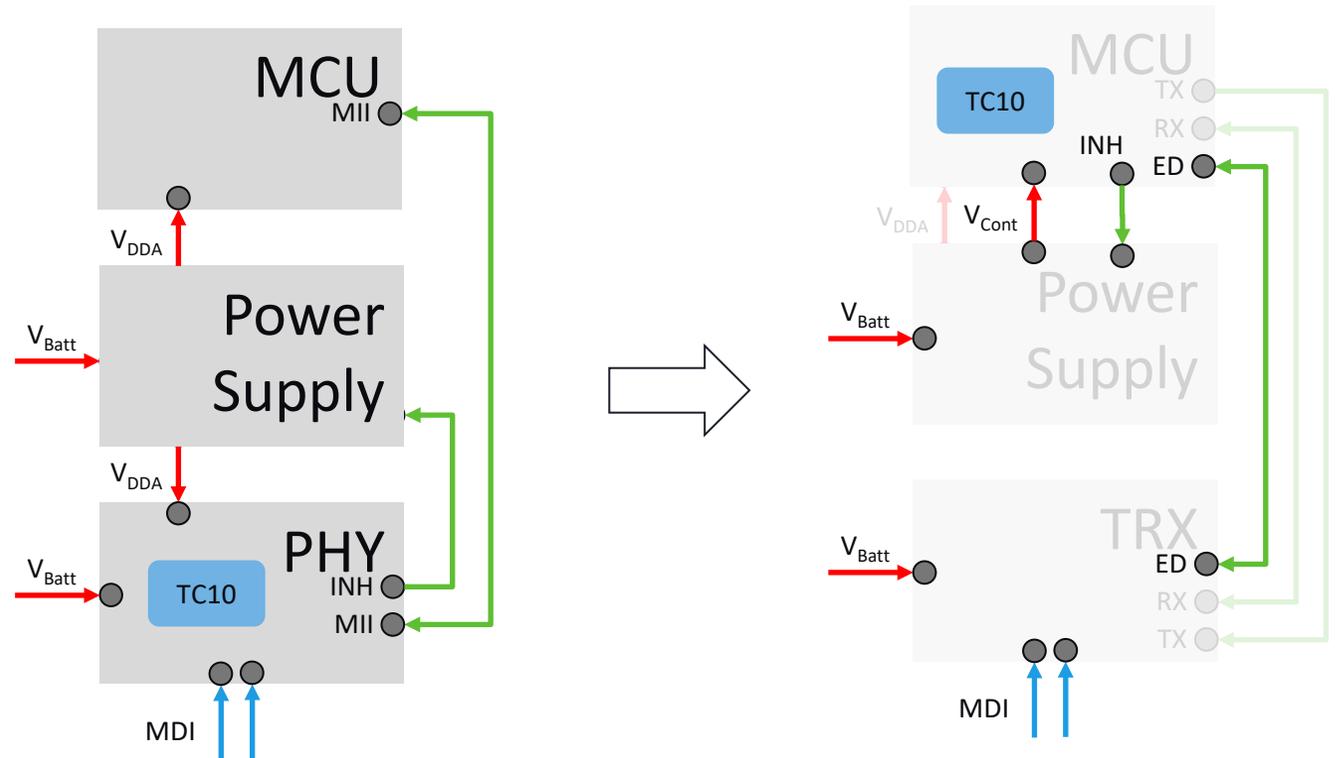
- **During sleep**
  - Power supply provides power to MCU
  - MCU only powers block detecting WUP
  - TRX off except block doing energy detection



# Wake/Sleep

## Awaking TRX-Based Architecture

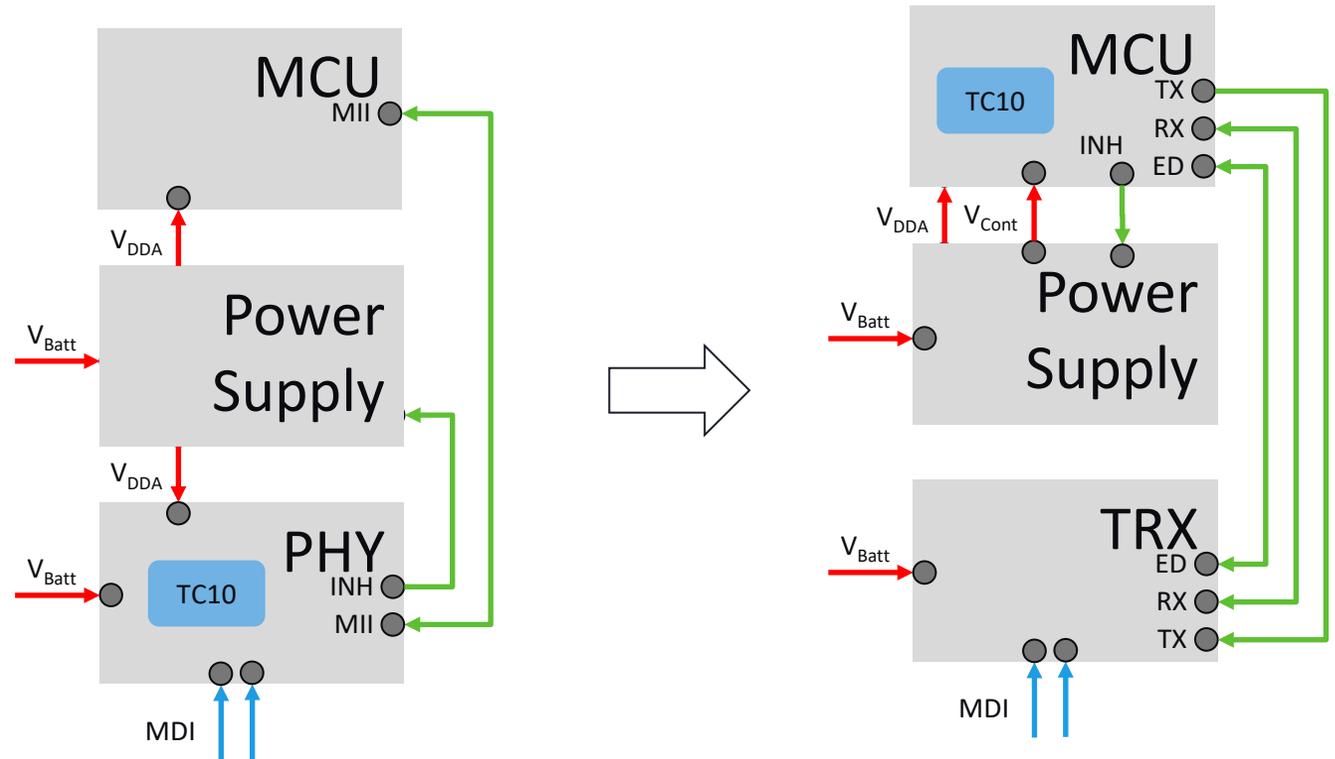
- **TRX detects energy**
  - MCU get ED signal
  - If MCU decides that this is a WUP, it issues INH signal



# Wake/Sleep

## Awaking TRX-Based Architecture

- **System powered**
  - Power supply on
  - MCU on
  - MCU sets TRX from sleep to transmit mode



# Summary

- **OA3p systems**

- Full featured including wake/sleep
- Fully IEEE compliant
- Die size saving >75% for digital part
- Pin saving 75% compared to PHY

- **OA3p is THE enabler for the All-Ethernet Vehicle**

