Zonal Architecture and New Opportunities to Optimize the Cost and Power of Interzonal Links

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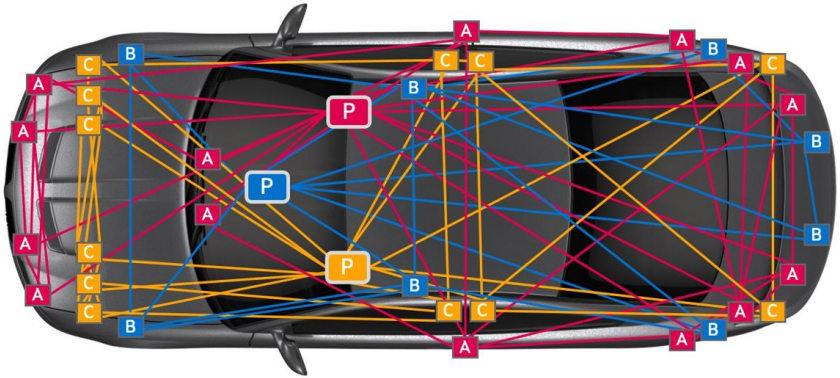
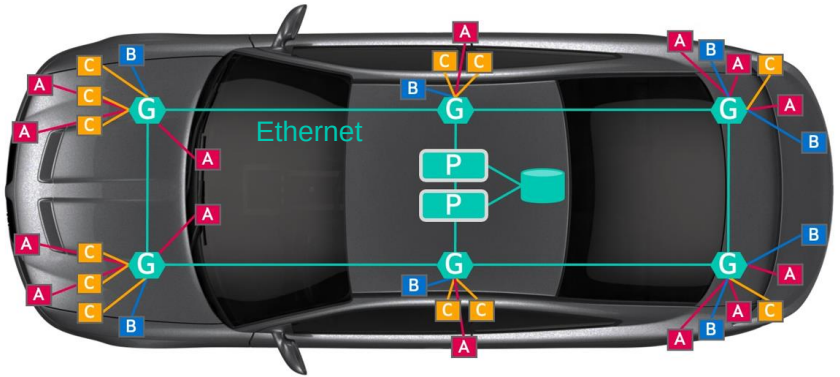
Domain-based vs. zonal architecture

Domains



Point to point, rigid, expensive

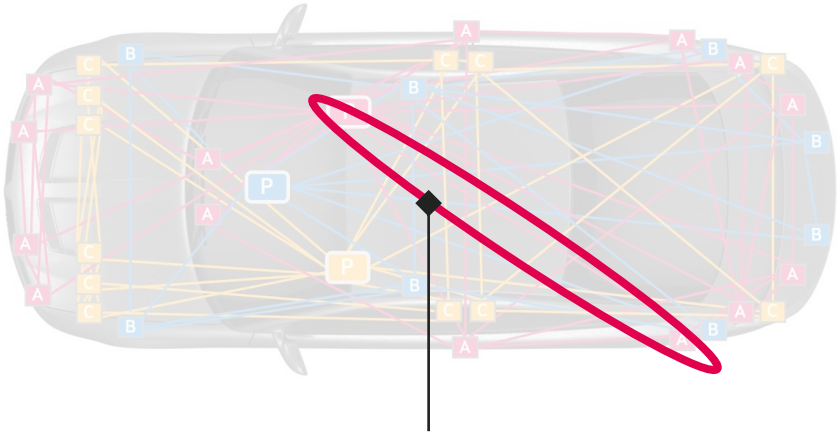
Zones



Networked, secure, scalable, intelligent

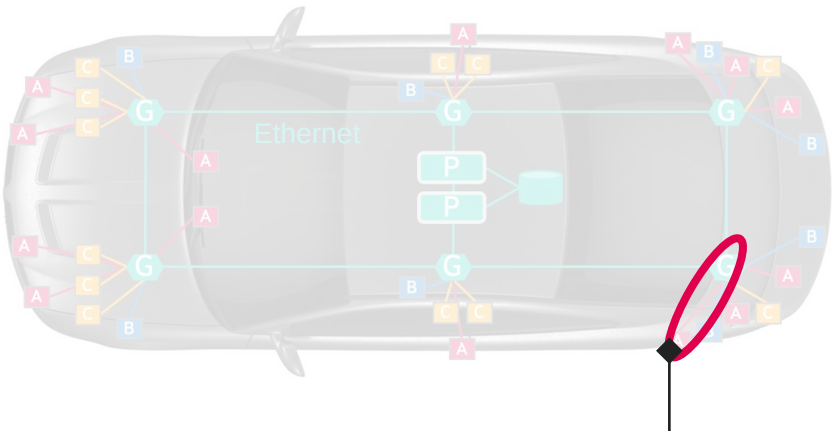
Zonal links are shorter

Domains



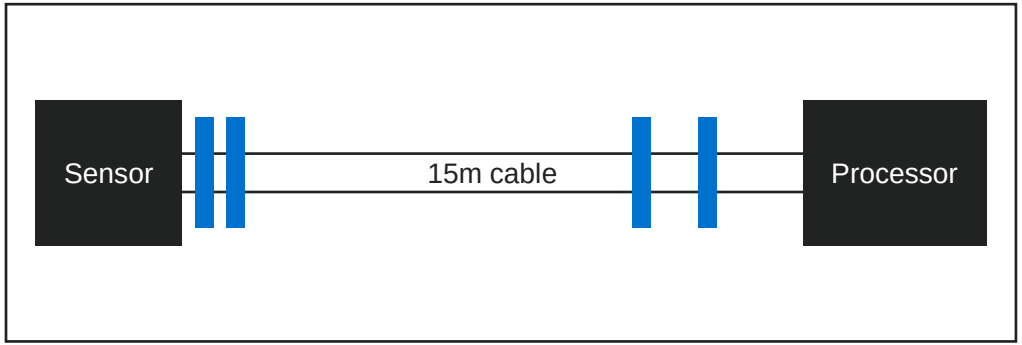
Point-to-point links are long

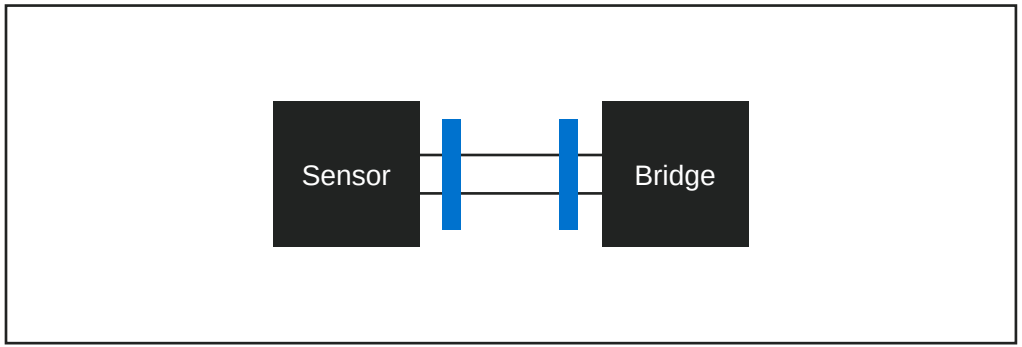
Zones



Interzonal links are short

Point-to-point vs. interzonal link attributes





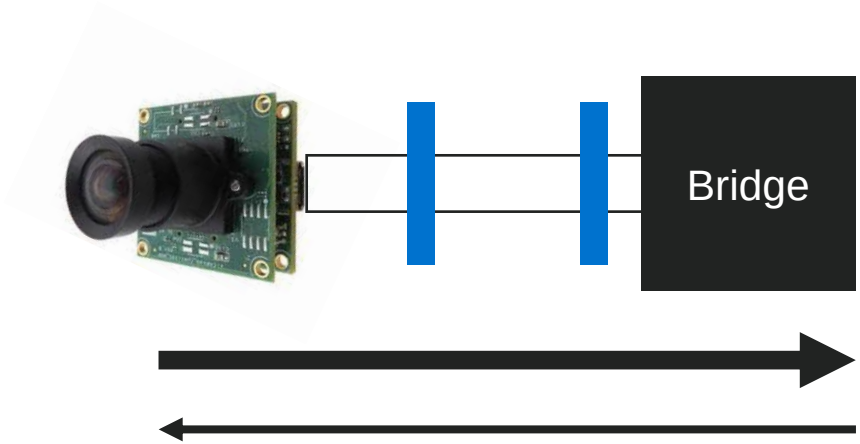
Point-to-point

- 15m:1000/2.5G/5G/10GBASE-T1
- 11m: 25GBASE-T1
- Up to four inline connectors

Interzonal

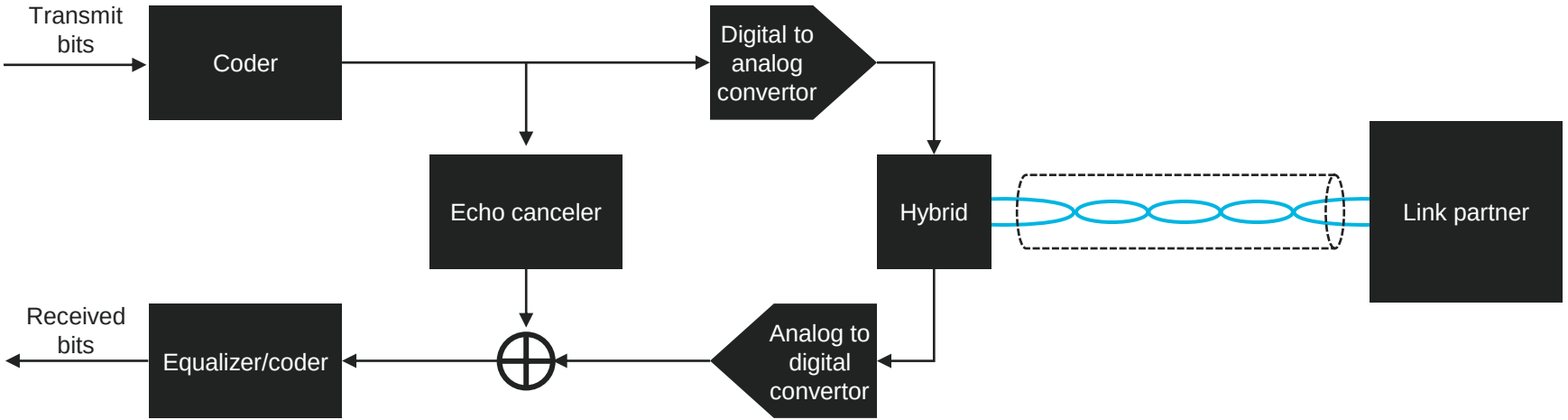
- Much shorter (less than 5m)
- Fewer inline connectors

Short-reach interzonal links ideal for camera-bridge

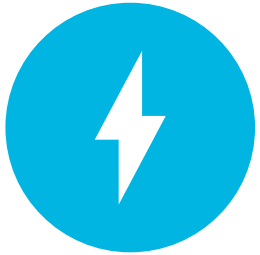


Camera Bridge is subject of recent 802.3 study group

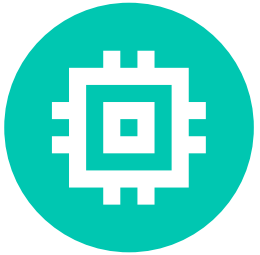
Typical full-duplex link



What we want to optimize



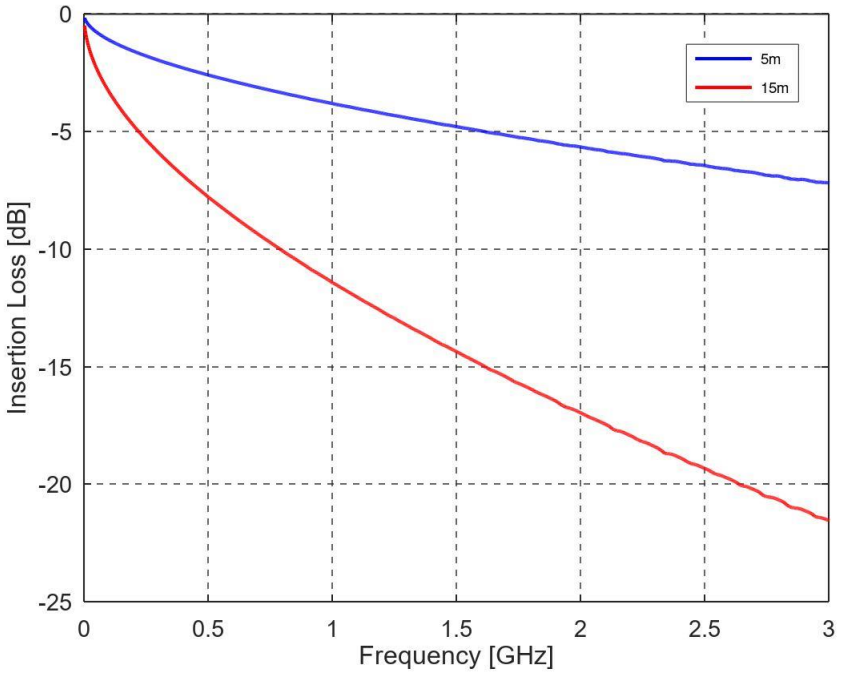
Power consumption



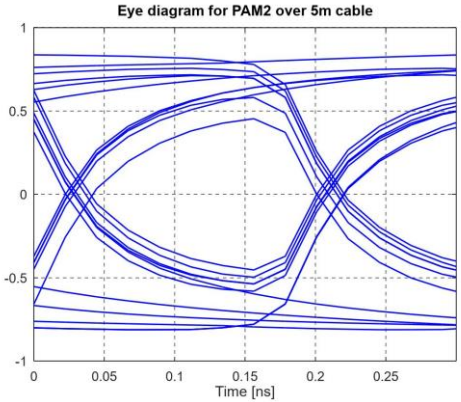
Silicon area (cost)

Lower power and area means lower complexity

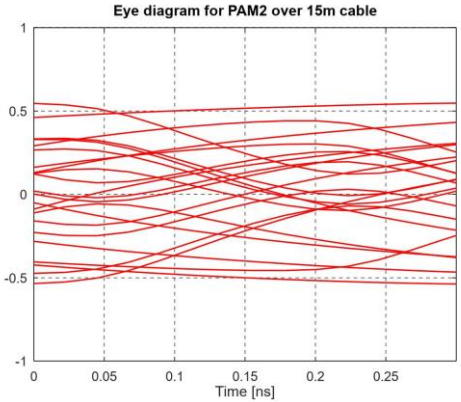
Lower insertion loss = simpler equalization



5m

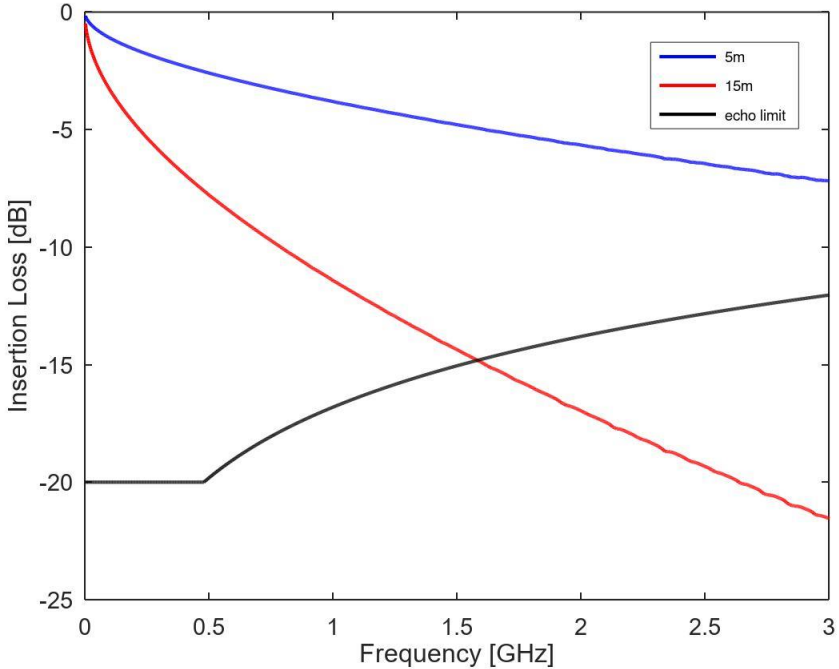


15m



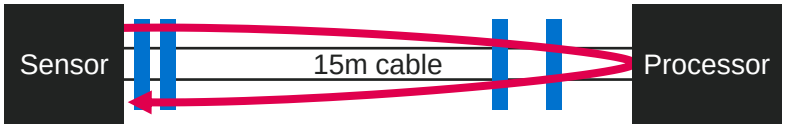
Source: Marvell

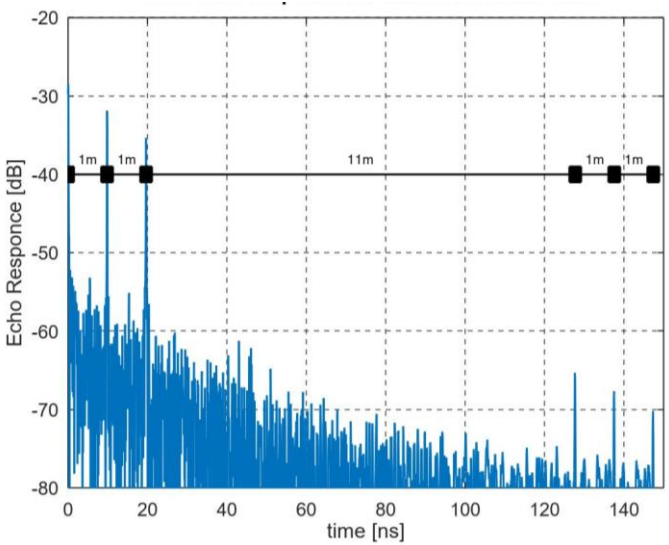
Lower insertion loss = less echo cancelation needed

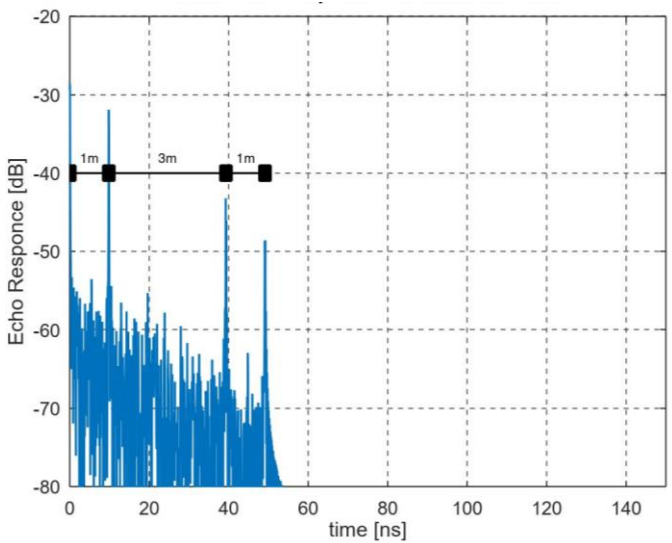


Source: Marvell

Shorter echo duration = simpler echo cancelers



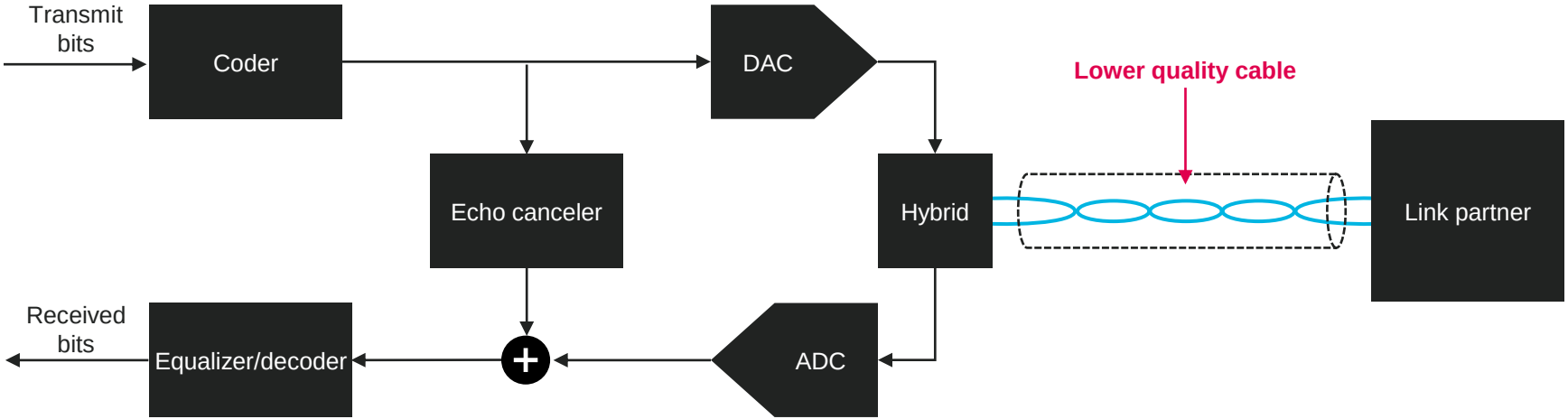




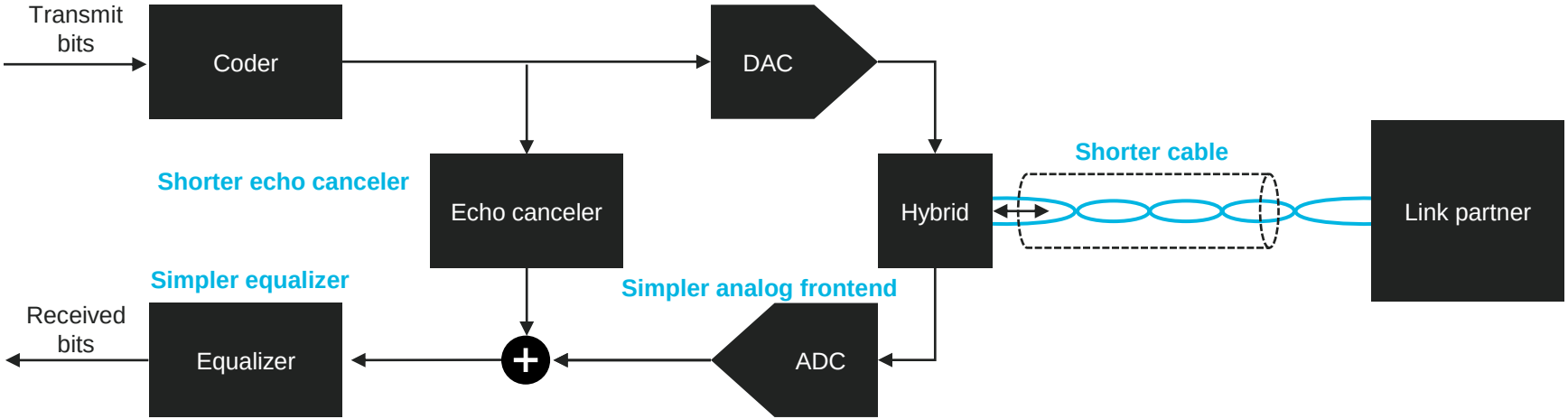
How can we take advantage of the shorter link?

	1	Enjoy higher design margin
OR	2	Use less expensive cable
OR	3	Reduce PHY power and/or area

Use less expensive cable



Power savings possible under current standards



Chip area savings not possible with current standards
Still need to support longer cables

What if…we optimized design for interzonal links?

Optimize equalization and echo cancellation circuits

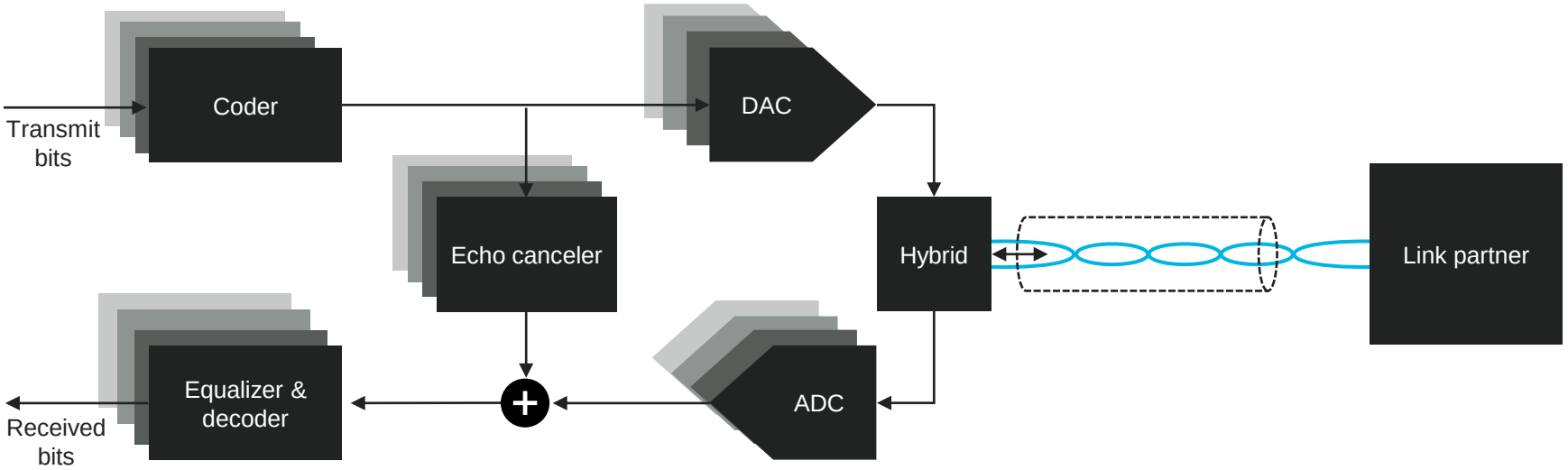
Use lower baud rate, higher-order modulation

Power and area savings

Power savings: *f*(baud rate)

Reduced need for HW parallelism = area savings

Lower baud rate reduces HW requirements



Use 802.3cy tool to compare PAM4 and PAM16

	Upstream	Downstream
Requirements		
Data Rate [Gbps]:	10	10
Target RS-FEC output BER:	1.00E-12	1.00E-12
Cable Length [m]:	**15.000**	**15.000**
Wire u-reflections limit:	jonsson*12_08_	jonsson*12_08_
Number of Connectors:	4	4
Modulation		
PAM Levels:	**4**	**4**
FEC Block Size (n):	360	360
FEC Data Size (k):	326	326
RS-FEC Correction Efficiency:	100%	100%
Bits per FEC Symbol:	10	10
TDD Time Duty-Cycle:	100%	100%
Framing Overhead:	1.875%	1.875%
Transmit Signal		
PSD-mask:	PSD_ZOH	PSD_ZOH
Transmit Power [dBm]:	0	0
Design Tradeoff		
Impulse Error Rate:	1.00E-04	1.00E-04
AFE-noise [dBm/Hz]:	-140	-140
Cable Reflection Echo Cancelation [dB]:	6	6
Connector Echo Cancelation [dB]:	50	50
Implementation Loss [dB]:	5	5
Simulation Parameters		
Cable Model:	mueller_3cy_01_12_01_20_stp	
PCB model:	pcb_kadry_3cy_02_0820	
PCB trace length [m]:	0.0762	
Connector Echo Model:	Hard	
Temperature [°C]:	20	
Max Simulation Frequency:	5.00E+09	

Calculated Values		
	Upstream	Downstream
Theoretical Slicer SNR [dB]:	26.69	26.69
Estimated Slicer SNR [dB]:	21.69	21.69
Required Slicer SNR [dB]:	17.20	17.20
SNR Margin [dB]:	**4.49**	**4.49**
Wire u-reflections [dB]:	-42.79	-42.79
Nyquist Frequency [GHz]:	2.81	2.81
Channel Insertion Loss @ Nyquist [dB]:	28.80	28.80
Cable Insertion Loss @ Nyquist [dB]:	27.79	27.79

	Upstream	Downstream
Requirements		
Data Rate [Gbps]:	10	10
Target RS-FEC output BER:	1.00E-12	1.00E-12
Cable Length [m]:	**5.000**	**5.000**
Wire u-reflections limit:	jonsson*12_08_	jonsson*12_08_
Number of Connectors:	4	4
Modulation		
PAM Levels:	**16**	**16**
FEC Block Size (n):	360	360
FEC Data Size (k):	326	326
RS-FEC Correction Efficiency:	100%	100%
Bits per FEC Symbol:	10	10
TDD Time Duty-Cycle:	100%	100%
Framing Overhead:	1.875%	1.875%
Transmit Signal		
PSD-mask:	PSD_ZOH	PSD_ZOH
Transmit Power [dBm]:	0	0
Design Tradeoff		
Impulse Error Rate:	1.00E-04	1.00E-04
AFE-noise [dBm/Hz]:	-140	-140
Cable Reflection Echo Cancelation [dB]:	6	6
Connector Echo Cancelation [dB]:	50	50
Implementation Loss [dB]:	5	5
Simulation Parameters		
Cable Model:	mueller_3cy_01_12_01_20_stp	
PCB model:	pcb_kadry_3cy_02_0820	
PCB trace length [m]:	0.0762	
Connector Echo Model:	Hard	
Temperature [°C]:	20	
Max Simulation Frequency:	5.00E+09	

Calculated Values		
	Upstream	Downstream
Theoretical Slicer SNR [dB]:	36.39	36.39
Estimated Slicer SNR [dB]:	31.39	31.39
Required Slicer SNR [dB]:	29.09	29.09
SNR Margin [dB]:	**2.30**	**2.30**
Wire u-reflections [dB]:	-35.00	-35.00
Nyquist Frequency [GHz]:	1.41	1.41
Channel Insertion Loss @ Nyquist [dB]:	6.14	6.14
Cable Insertion Loss @ Nyquist [dB]:	5.60	5.60

Use 802.3cy tool to compare PAM4 and PAM16

Areas for further study

- Electromagnetic noise
- Error correction codes/latency
- Jitter sensitivity

Key takeaways

1. Existing standards designed for point-point and backbone network
2. Zonal architecture: most links are between sensors and local switches
3. Current Ethernet PHYs are overdesigned for interzonal links
4. Standards evolution would enable PHY optimization for interzonal links

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Thank You

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Special thanks to Mark Davis for his valuable inputs