POTENTIAL GAPS FOR AUTOMOTIVE ETHERNET A VIEW FROM THE END-USER

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OVERVIEW

From the abstract:

After several year using Automotive Ethernet with a great success some negative topics appear too. In many cases it seems that discussing negative topics, so called undefined "extra features" is not necessary and not really a thing to do this in the public. Differently we would give an impulse with the presentation to the Automotive Ethernet users an impulse actively to cooperate to avoid pitfalls, improve the technology and strengthen the Automotive Ethernet community. The presentation will cover Interop issues at one example, currently under investigation. A second topic shows the MDIO interface for configuration as an potential risk. The last example tries to explain, where the IEEE and OpenAlliance specifications need to improve for higher data rates.

Three examples:

➢ Start-up of 100 and 1000BaseT1 links.

➢ MDIO issues.

➢ Missing parameters for STP link and system.

START UP UNDER NOISE

➢ Why EMC noise seems to be an underestimated problem.

➢ Two test setups for impact on noise.

➢ Summary on test results and conclusion.

START UP UNDER NOISE - INITIAL OBSERVATION

▪ A test report of a device, which performs an extra test with extended parameter:

ETH-Link-Off Observation

Description of Test:

1. Apply disturbance to DUT
2. Switch on DUT and boot up
3. Switch off DUT
4. Switch to next Frequency and continue with 1

Note: dwell time = 15sec boot up + 37sec monitoring = 52sec

Observation:

• During and after boot up sporadically and not frequency depending, ETH-Port has no link established or late established.

Is this a relevant test?
Test error?
Current status of PHY implementation?

Discussion was already started at the beginning of Automotive Ethernet:

▪ PHY designer: The link-up uses a modified signaling, which is more robust than normal traffic.

But it is a critical phase, as the channel parameters are not compensated.

▪ EMC result (~2014) show no significant impact of noise at start-up.

→ was not a topic for further investigation.

→This sequence exceeds current requirements (currently: only established link is tested).

→Test sequence needs longer time between the frequency steps.

→Current EMC test sequence implicitly causes a link-up with no-noise/no-field, as between each frequency step the field is reduced / turned-off.

➜Can the observed behavior be confirmed?

➜Can we define a useful test setup?

SETUP 1 – USE SINE WAVE / NOISE GENERATOR
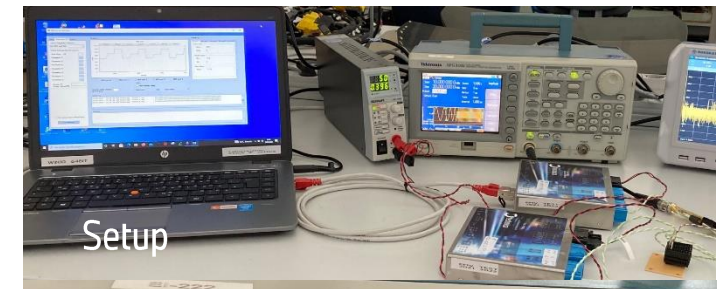
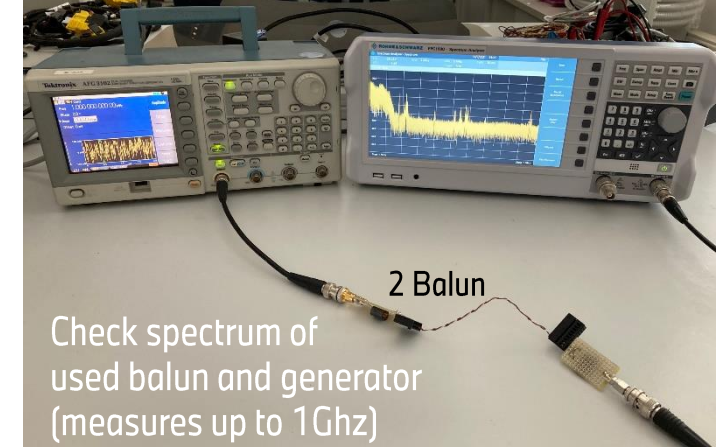Setup is derived from IEEE-receiver test:
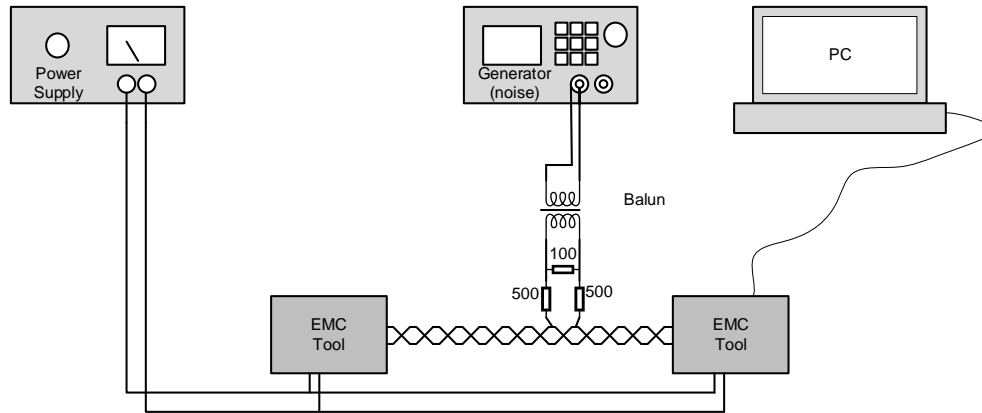
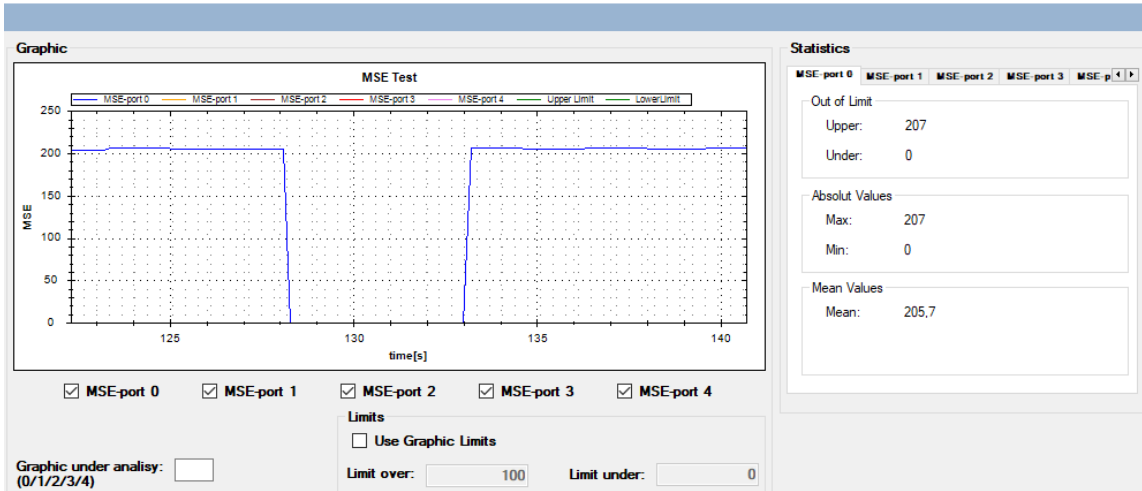Two test signals are used: sine sweep / Gaussian noise.

- Monitoring the MSE value, the impact of noise on active link can be observed.

- Try a link-up with a known noise level:

a)   Either with Power On (Hard Reset).

b)   -Or- with PHY Soft Reset.

Results of this setup:

➔ Sine sweep and Gaussian noise shows impact.

➔ Obviously a difference between Hard Reset and Soft Reset.

Check spectrum of used balun and generator (measures up to 1Ghz)

Setup

Parameter settings at AWG

OBSERVING THE MSE VALUE AND LINK-UP WITH „EMC-TOOLS"

Setup for both: Using the noise generator to get a MSE value of > 200.

- **Power- On Reset** of one link partner for a defined time.

Soft Reset: Use test feature for link-up test.

Indication:
- Link-up behavior change in presence of noise on the line.
- Link-up differs between Hard-Reset / Power-On and Soft-Reset.

But these setups have to many side parameter which impact the behavior.
➔ Define a more direct test setup for detailed test. With different PHYs from different vendor.

SETUP 2 - USE EMC TEST SETUP

- Using the same EMC tools;
- Apply Soft Reset → built-in feature of EMC tool.
- Apply Power-On Reset link partner (1s Power off)

      60s per step; read-out / reset every 5s

Test Setups:
  – Stripline 200V/m
  – BCI 106dBµA
  – Antenna: (Log-Per 0.2-1GHz)
       70V/m; 100V/m; 120V/m; 140V/m

Results using these setups:
➔ EMC has impact on start-up.

Setup Stripline

Observation MSE
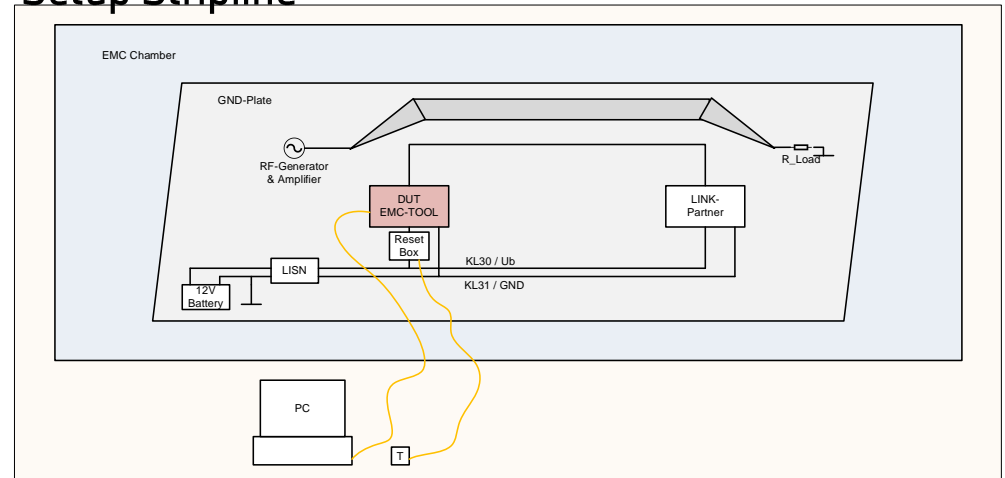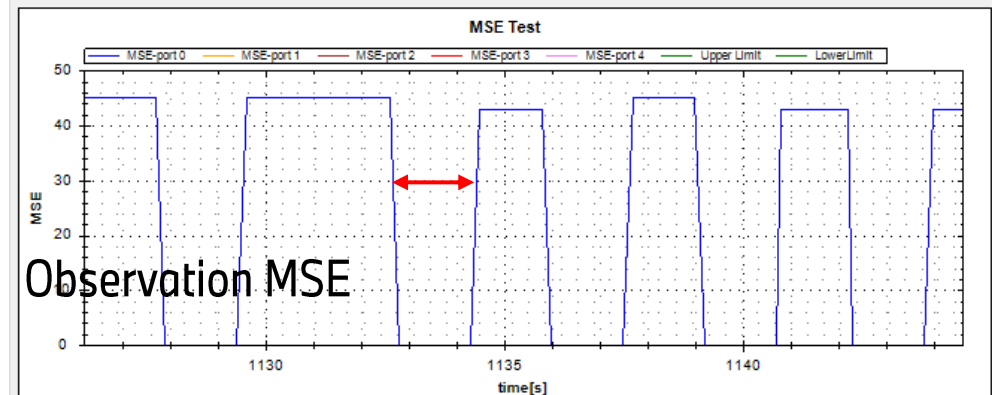
Indication:
- Link-up behavior change in presence of noise .
- Link-up differ between Hard-Reset / Power-On and Soft-Reset.
Note: Here mainly deviation of link–up time at frequencies out-of-band were observed!
These setups have many side parameters which impact the behavior (as stated before).
➔ Define a more direct test setup for detailed test.
➔ With different PHYs from different vendors.

SUMMARY: START-UP UNDER NOISE

- Test setup 1 verified at Ruetz for 1000BaseT1; setup 2 verified at FTZ for 100BaseT1 with DPI setup: ➔ observation confirmed.
  - ➔ deviation of link-up time.
  - ➔ fail at dedicated frequency.
  - ➔ behavior is different for chips from different vendors.

DUT	Link Partner			
A	B	IOP_16_SR_M_S_C1_T1	IOP_16_SR_S_M_C1_T1	LinkUp>100ms
A	C	IOP_16_SR_M_S_C1_T1	IOP_16_SR_S_M_C1_T1	
B	A	IOP_16_SR_M_S_C1_T1	IOP_16_SR_S_M_C1_T1	LinkUp>100ms
C	A	IOP_16_SR_M_S_C1_T1	IOP_16_SR_S_M_C1_T1	

Test Results DPI Link up Test vs. normal Communication Test – Conclusion
Narrowband vs. Broadband Disturbances
Different Transceivers, Optimized BIN

Transceiver type	Maximum test power at broadband power meter without failure / dBm							
	Link up test				Normal communication test			
	min 2.5% unbalanced Narrowband	min 2.5% unbalanced Broadband	min 5% unbalanced Narrowband	min 5% unbalanced Broadband	min 2.5% unbalanced Narrowband	min 2.5% unbalanced Broadband	min 5% unbalanced Narrowband	min 5% unbalanced Broadband
A	≥ 40	≥ 40	≥ 40	38.5	≥ 40	≥ 40	≥ 40	≥ 40
B	≥ 40	≥ 40	≥ 40	≥ 40	≥ 40	≥ 40	≥ 40	≥ 40
C	32.0	36.5	28.0	28.0	≥ 40	≥ 40	35.0	38.0
D	≥ 40	39.5	≥ 40	34.5	≥ 40	≥ 40	≥ 40	36.5

Comment: current limit requirements DPI narrowband for symmetric and +/- 2.5% unbalanced

- The initial observation is correct:
 - ➔ start-up under noisy condition might fail or may be delayed.
  - ➔ depends on vendor implementation.

- For some applications it might be a relevant issue, when link-up is significantly delayed or even fails.
- Potentially a topic for low-power modes, e.g. EEE with sync-sequences in the low power operation.

- The start-up has to be tested independent from a established link.
- Same for low-power modes.

- The test method with the AWG generator and the directional coupler seems a fast and direct method for tests.
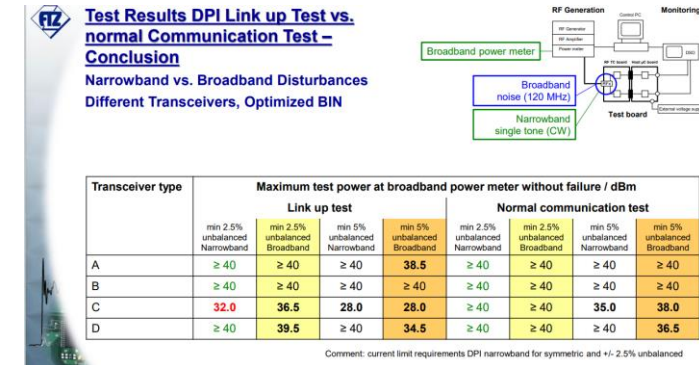
➔ IEEE should define test criteria for the start-up and for the low-power mode with environmental impact.

MDIO ISSUES

➢ MDIO Basic - a short introduction.

➢ Why MDIO is important:

- MDIO use case: Configuration.

- Consequences of wrong or defective configuration.

➢ Experience with using MDIO :

- Example: Impact of timing.

- Approach for analyzing the MDIO traffic.

➢ Summary and proposal for improvement.

MDIO BASICS

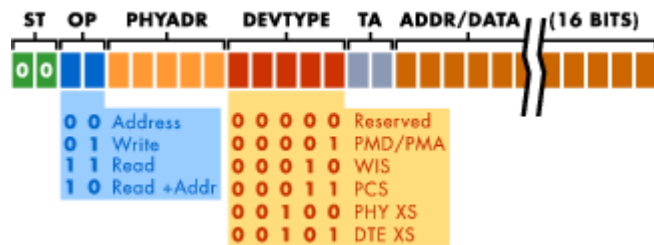A short introduction to MDIO:

Clause 22:*

Original Format; limited address range (5bit).

Clause 45:**

Extended Format; extended address range (16 bit / Devtype).

$V_{I/O}$ 1.2V**….5V*

MDC frequency :   min: kHz … max: 2.5 to 10 MHz.

ST	2 bits	Start of Frame (01 for Clause 22)
OP	2 bits	OP Code
PHYADR	5 bits	PHY Address
REGADR	5 bits	Register Address
TA	2 bits	Turnaround time to change bus ownership from STA to MMD if required
DATA	16 bits	Data Driven by STA during write Driven by MMD during read

ST	2 bits	Start of Frame (00 for Clause 45)
OP	2 bits	OP Code
PHYADR	5 bits	PHY Address
DEVTYPE	5 bits	Device Type
TA	2 bits	Turnaround time to change bus ownership from STA to MMD if required
ADDR/DATA	16 bits	Address or Data Driven by STA for address Driven by STA during write Driven by MMD during read Driven by MMD during read-increment-address

MDIO is for PHY the Interface for configuration, control and monitoring.

MDIO USE CASE: CONFIGURATION AT DIFFERENT PHY GENERATIONS

Configuration of PHYs using the MDIO interface is an important use case:

A comparison of size of configuration script for different PHY generations.

Base is the size of the SW implementation (api.c-file) in kilobyte.

[Source: vendor API / real implementation]

PHY-Generation	HW-Config	MacSec	PTP	EEE
100BaseT1 (2018)	Yes (7Kb)			
100BaseT1 (2021)	Yes (10Kb)			
100BaseT1 (2025)	Yes	Yes	Yes	
1000BaseT1 (2018)*	Yes (39Kb)			
1000BaseT1 (2021)	Yes (30Kb)			
1000BaseT1 (2025)	Yes (30Kb)	Yes (122Kb)	Yes (30Kb)	
MGBaseT1	Yes (150Kb)	Yes	Yes	Yes

* Some adoptions for 1000BT1 operation were made thru scripts during the market introduction

Size of configuration parameter increases over speed grades and feature set.
There is no indication that there is a saturation for necessary configuration data.
Configuration of PHY is done via MDIO Interface.

CONSEQUENCE OF USING A WRONG / DEFECTIVE CONFIGURATION

PHY function will not be according to the requirement of the chipmakers:
      a) no function at all
      b) marginally different function
      c) side effects in specific operation states
      d) non-optimal performance (start-up, EMC, error handling, …)

> Not the worst-case

> Daily business*

- The next example shows the impact of a timing variation

      as not specified by the chip maker.

- What will happen if we get a bit error during transmission?

  - From EMC?

  - Internal ECU noise?

  ➔ currently not a reported fault for Ethernet; known failure for CAN devices and ASICs.

*Feedback from chipmakers during test in development   (not caused by environmental events, but indicating that wrong data are not seen easily)

Script is not the latest one that has been used in your tests as well as the chip version.

I strongly recommend to start your tests with xxx version of the ABCXYZ and latest script.

> **Use of a wrong or a defective script will not be indicated always immediately as failure/mal-function!**

> **➔ MDIO needs some improvement e.g. a defined method for guaranteed data integrity.**
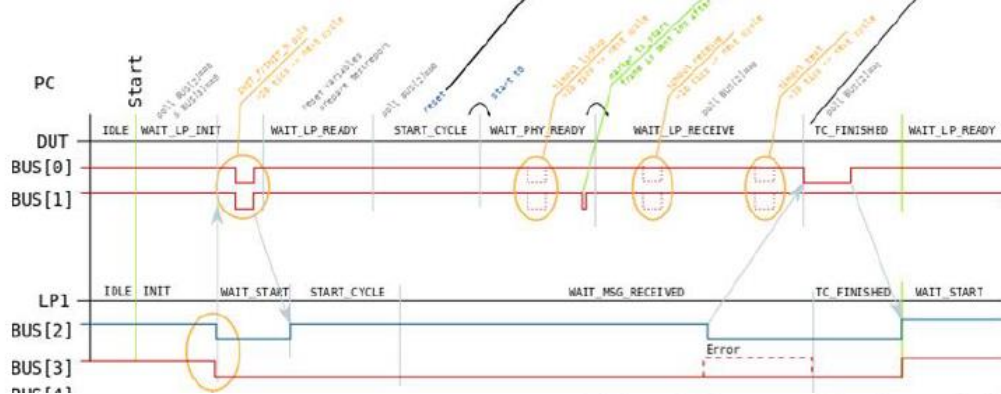
EXAMPLE: IMPACT OF TIMING IN MDIO ACCESS

At extended IOP tests we observed an issue about timing at the MDIO bus:

Following setup / procedure is used:

Variable SW/HW Reset timing
+ konfigurierbar sw/hw Reset
+ variable Wartezeit nach Reset

Control of timing
+ zusätzliche überwachung des Links
für einen konfigurierbaren Zeitraum

This wait time was implemented as a modifiable parameter to increase the pause after a reset "Reset time"

```
device->wait(device, 2);
device->writeReg(device, device->phyAddr, 1, 0x0, 0x840);
device->writeReg(device, device->phyAddr, 3, 0xFE1B,
0x48);
device->writeReg(device, device->phyAddr, 3, 0xFFE4,
0x6B6);
device->writeReg(device, device->phyAddr, 1, 0x0000,
0x0000);
device->writeReg(device, device->phyAddr, 3, 0x0000,
```

Tests made by In-tech / Ruetz-System-Solutions on behalf of BMW

Linkup deviation between HW and SW Reset.
Link-up behavior dependent from timing parameter in configuration file
AND accordingly execution of the code (in complex SW–system…).

3.1 Reset time= 2ms (default)

IOP_16_SR_S_M				
Parameter	Min	Max	Value	Unit
maximum linkup time		100	93,3	ms
minimum linkup time	0		12,8	ms
Standard deviation linkup time		50	7,99	ms

IOP_16_HR_S_M				
Parameter	Min	Max	Value	Unit
maximum linkup time		100	12,8	ms
minimum linkup time	0		11	ms
Standard deviation linkup time		50	0,90	ms

3.2 Reset Time=7ms

IOP_16_SR_S_M				
Parameter	Min	Max	Value	Unit
maximum linkup time		100	88	ms
minimum linkup time	0		12,8	ms
Standard deviation linkup time		50	7,49	ms

IOP_16_HR_S_M				
Parameter	Min	Max	Value	Unit
maximum linkup time		100	12,8	ms
minimum linkup time	0		11	ms
Standard deviation linkup time		50	0,90	ms

3.3 Reset time= 14ms

IOP_16_SR_S_M				
Parameter	Min	Max	Value	Unit
maximum linkup time		100	12,8	ms
minimum linkup time	0		11	ms
Standard deviation linkup time		50	0,90	ms

IOP_16_HR_S_M				
Parameter	Min	Max	Value	Unit
maximum linkup time		100	12,8	ms
minimum linkup time	0		11	ms
Standard deviation linkup time		50	0,90	ms

APPROACH TO ANALYZE FOR CORRECT MDIO-ACCESS

We have observed that it might be useful to check for correct configuration.
Does a verification of data written to the PHY help?

Example shows a commercial SOHO switch:
Behavior can be found at almost any Automotive PHY, too.

Read-Back of register provides different data than written.
- It depends on the according function.
- Not useful for a simple control for correct settings.

Current status: The user can only follow the guidelines of the chip vendor
and has no guarantee that configuration was received correctly.

SUMMARY: MDIO

- MDIO gains importance for PHY / Switch operation:

  - Improvement for data integrity is needed.

  - Improvement on definition of data handling is needed:

        - timings

        - structure

- MDIO is the access of the user to internal information for controlling, monitoring, debugging.

- A short list for new requirements / potential improvements:

        - establish a robust communication, with:

              - Checksum / bit error detection / Check for correct data transmission.
              - Check for data consistency.
              - Definition of timing of data transfer.
        - high speed: allow fast access for monitoring.

        - allow access in low power mode of PHY.

        - security feature for MDIO access.

        - test modes (e.g. defined test sequence).

        - adjustable I/O characteristics / driver strength.

        ... -tbc-

MISSING PARAMETERS FOR STP LINK AND SYSTEM

➤ Overview IEEE specification for the link channel.

➤ Understanding the IEEE specification.

➤ The channel under the view of EMC.
- A different view from the end user.

➤ Summary on missing parameters.

IEEE SPECIFICATION FOR THE CHANNEL (EXAMPLE: 802.3CH)

149.5.1   Test Modes: (@MDI):

    - Jitter, PreCoder, TX linearity, normal PSD, TX droop; Normal Mode.

149.5.2   TX electrical specification:

       - assume either test mode –or- normal operation.

149.5.3   RX electrical specification:

       - BER, Alien crosstalk noise rejection.

149.7   Link segment:

       - IL, RL Coupling/Screening Attenuation; PSANEXT, PSAACRF.
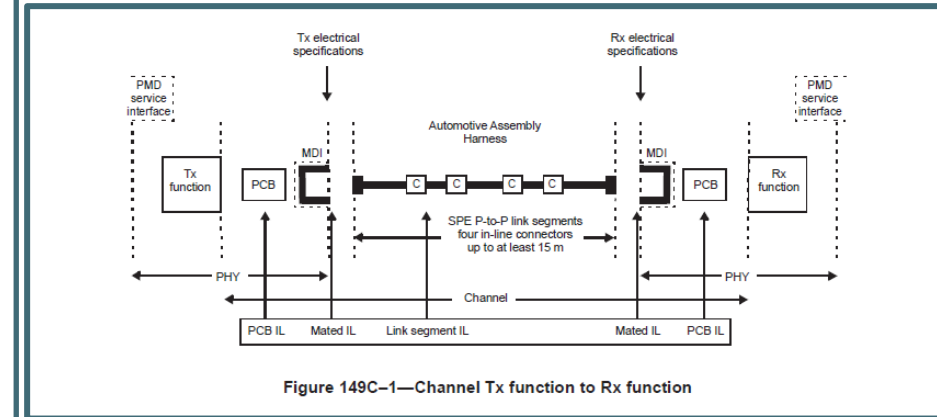
149.8   MDI specification:

   - RL.

149.9   Environment:

       - Safety, EMC.

149 C   TX function to RX function channel characteristic:

       - PCB, IL, RL, Coupling between multiport.

Figure 149C–1—Channel Tx function to Rx function

UNDERSTANDING THE IEEE SPECIFICATION

- IEEE 802.3 defines a standard   -not the implementation- :
    - Definition of the protocol.
    - TX characteristic.
    - Definition of the link segment.
- RX characteristic is implementers choice.
- Standard conformant implementations are the essence of the IEEE community.
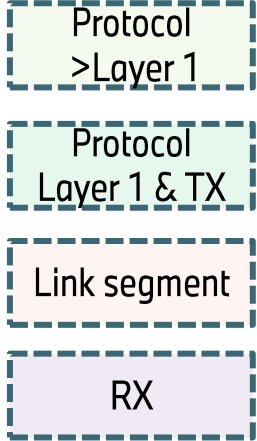
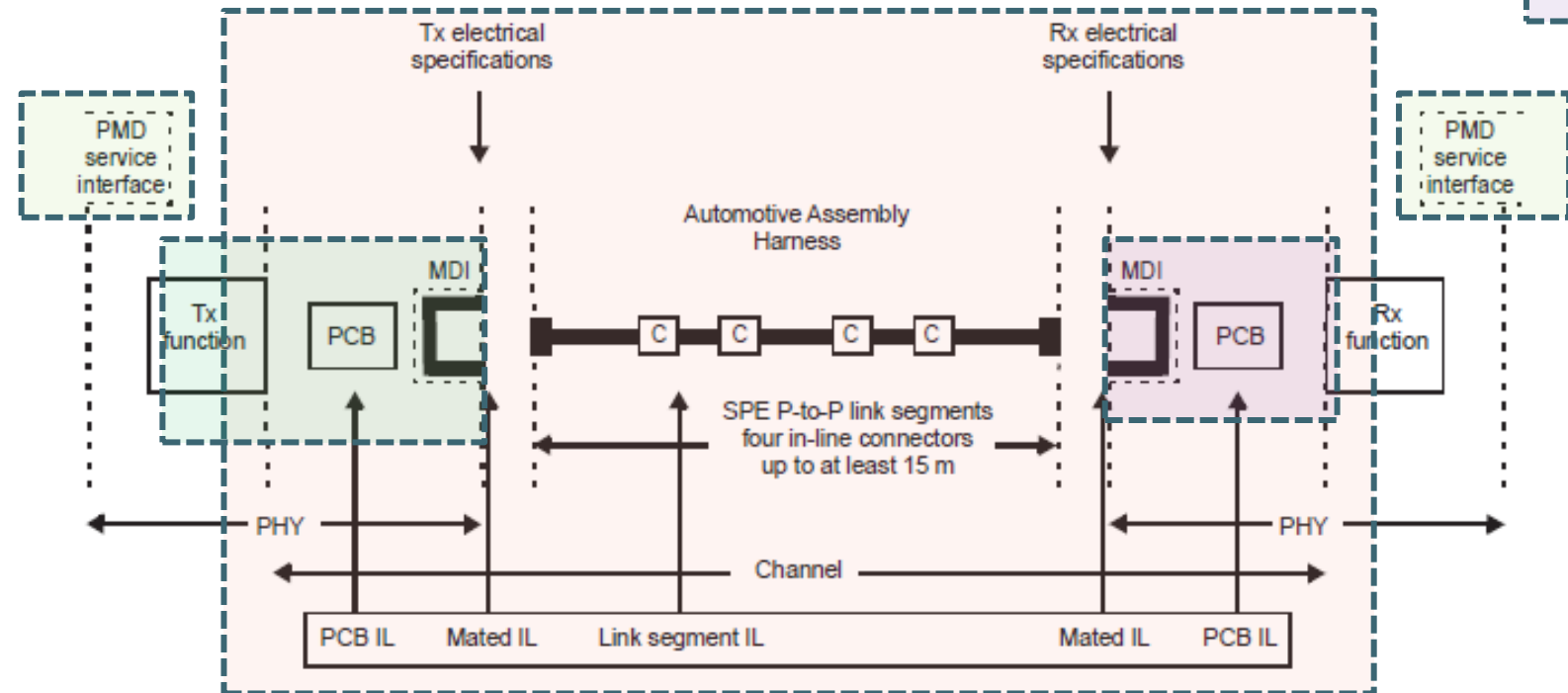The figure summarizes the scope of the IEEE Spec about the channel:

Protocol
>Layer 1

Protocol
Layer 1 & TX

Link segment

RX

Figure 149C–1—Channel Tx function to Rx function

THE CHANNEL UNDER THE VIEW OF EMC

Definitions are made towards :
➢ Signal behavior.
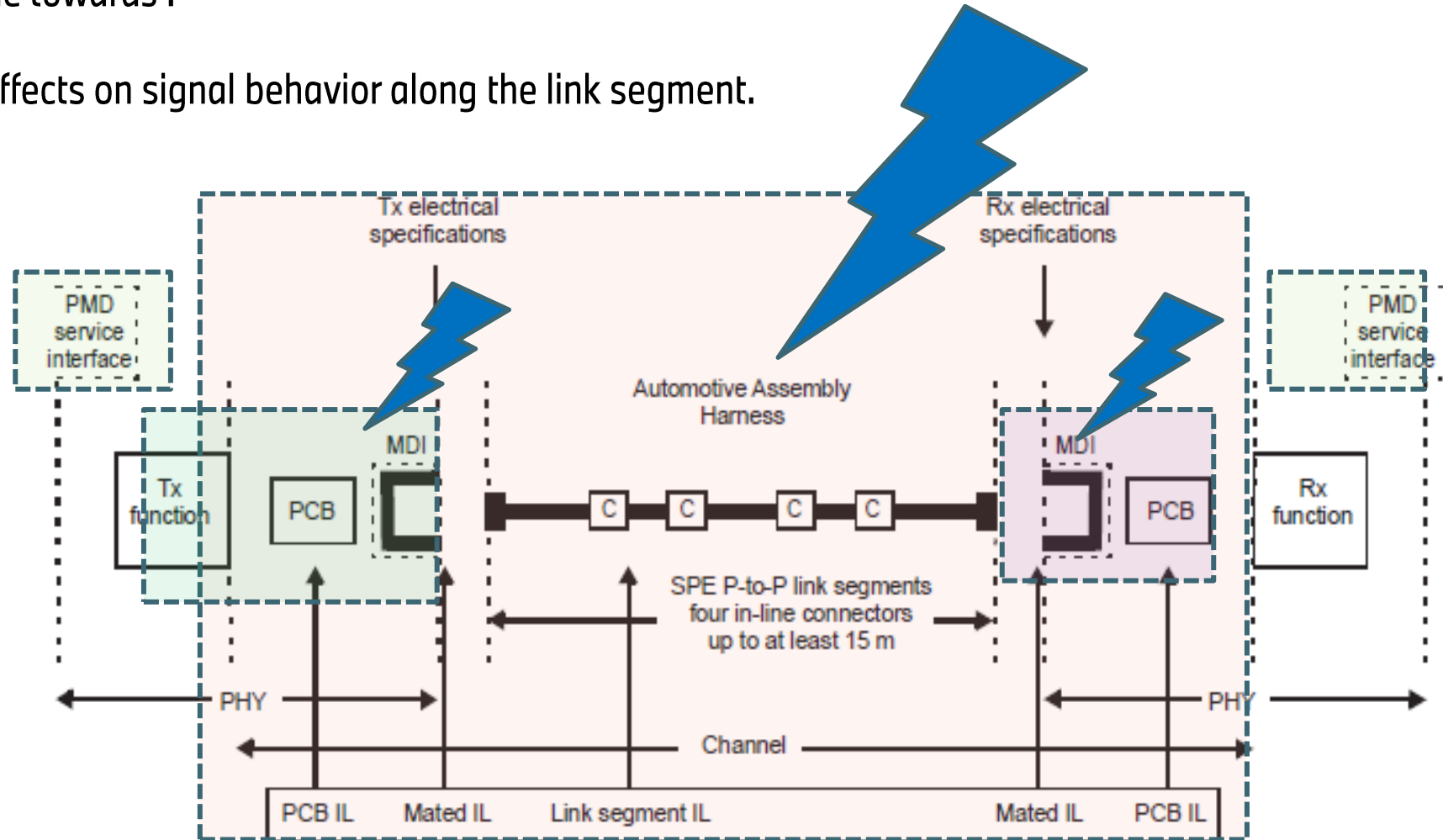➢ Impact of EMC effects on signal behavior along the link segment.

Figure 149C–1—Channel Tx function to Rx function

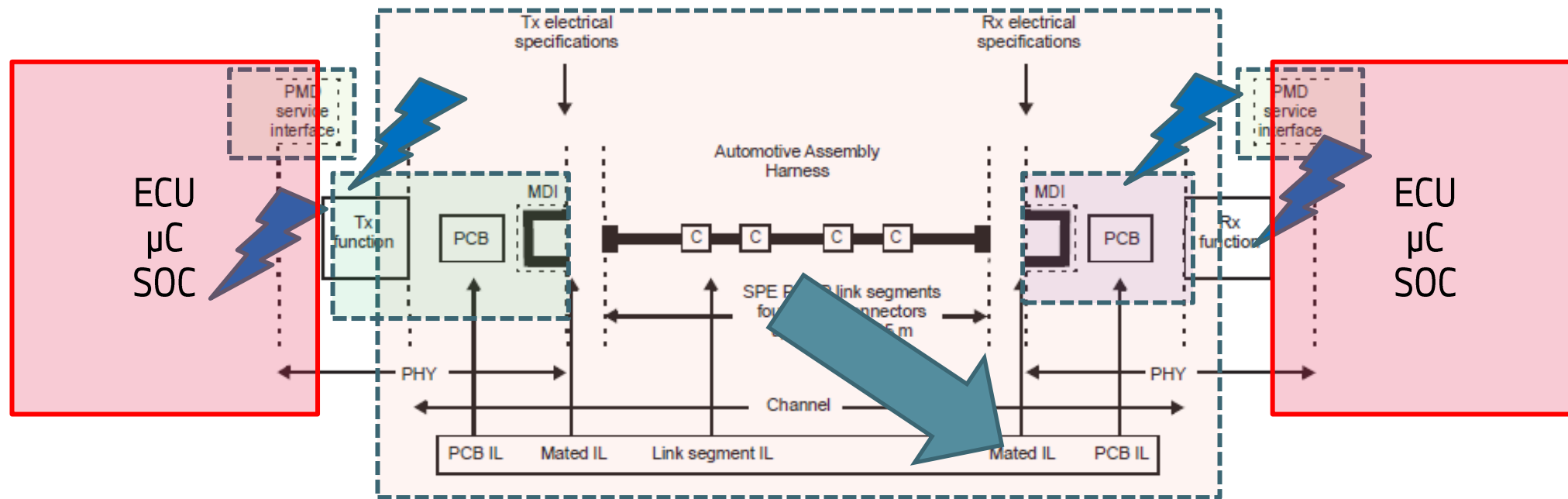# A DIFFERENT VIEW FROM DAILY LIFE OF END-USER

Figure 149C–1—Channel Tx function to Rx function

Almost no definitions are made towards:

➤ A real channel with the additional parameters:
  — Mode conversion.
  — Rules for use of shield.
➤ EMC emission.
➤ Other interfaces of the chip ("implementers responsibility / choice").

149.9.2.2 Electromagnetic compatibility

A system integrating a PHY intended for automotive applications is expected to comply with all applicable local and national codes. In addition, the system may need to comply with more stringent requirements for the limitation of electromagnetic interference. When used in an automotive environment, the PHY is expected to meet the following motor vehicle EMC requirements:

  a) Radiated/conducted emissions: CISPR 25, IEC 61967–1, IEC 61967–4, and IEC 61000–4–21
  b) Radiated/conducted immunity: ISO 11452, IEC 62132–1, IEC 62132–4, and IEC 61000–4–21
  c) Electrostatic discharge: ISO 10605, IEC 61000–4–2, and IEC 61000–4–3
  d) Electrical disturbances: IEC 62215–3, ISO 7637–2, and ISO 7637–3

Exact test setup and test limit values may be adapted to each specific application.

SUMMARY ON MISSING PARAMETER FOR STP

➢ Mode conversion currently not defined in IEEE specification.

   ➔ IEEE spec should define requirement on mode conversion:

      of the Channel.

      of the MDI at PCB level.

➢ EMC is covered in a short statement –   proposal for further improvements:

       - Even they might be potentially out-of-scope of IEEE –

  - Generic concept for shielding.

      Shield as a method to handle EMC at the use of high-speed data links.

  - Include other interfaces of Ethernet devices:

      - Configuration / control interfaces: MDIO, SPI.

      - Interface to µC /SoC: *MII, PCIe …

  - Include GND and power supply concept into EMC topic.

EMC topics are not uni-directional:
Signal integrity and electro-magnetic-compatibility are the two sides of the same coin.

OVERALL SUMMARY

There are gaps in the IEEE specifications....

There are potential improvements for specifications.

There is no real hard border between essential definitions and implementation topics.

> Currently missing topics / finalization for automotive is done at Open Alliance.
> When chips are available: ➔ time, costs, and requirement to change an existing device.
>
> Some topics are today out of the traditional scope of an IEEE 802.3 specification...
> ...an automotive EMC guideline as part of the specification collection could help to establish a clean standard.
>
> Additional, generic requirements for all interfaces and pins of an Ethernet device could help to avoid pitfalls and will reduce the effort of testing.

Any item not addressed is a potential interoperability issue,
with the consequence of a non-standard conformant market approach, sub-de-facto standard implementations,
at extra cost and time.

Automotive industry needs IEEE as strong standardization body.

IEEE needs a wide and in-depth contribution, continuously from the automotive industry, the OEMs, the 1st &
2nd tier suppliers.