Self Healing Nano-Electronics for Nano-Spacecraft in Deep Space Missions

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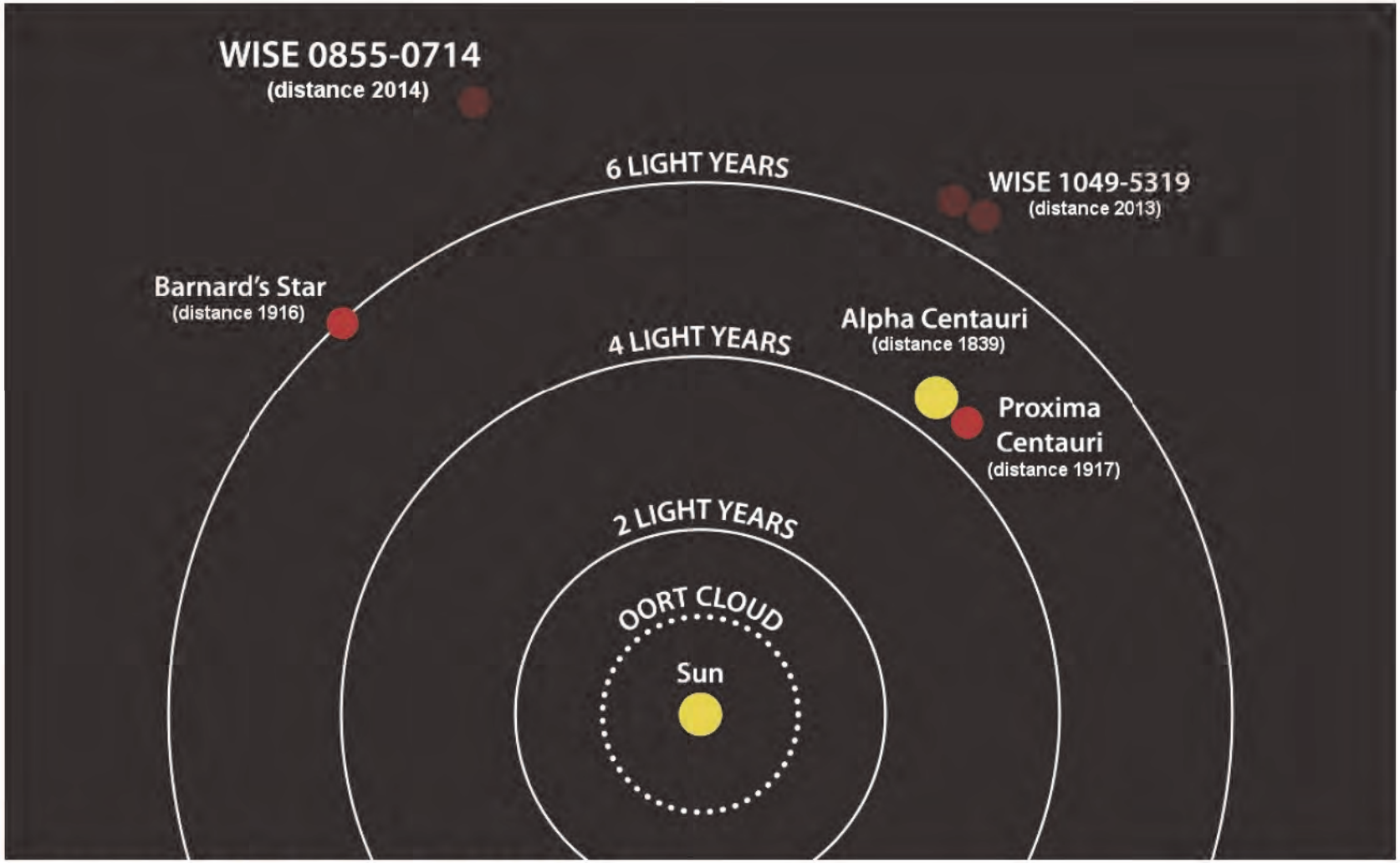
Outline

- Introduction
- Design of Sustainable Electronics
- Pristine Device
- Damage and Recovery
- Applications
- Conclusions

Space Exploration

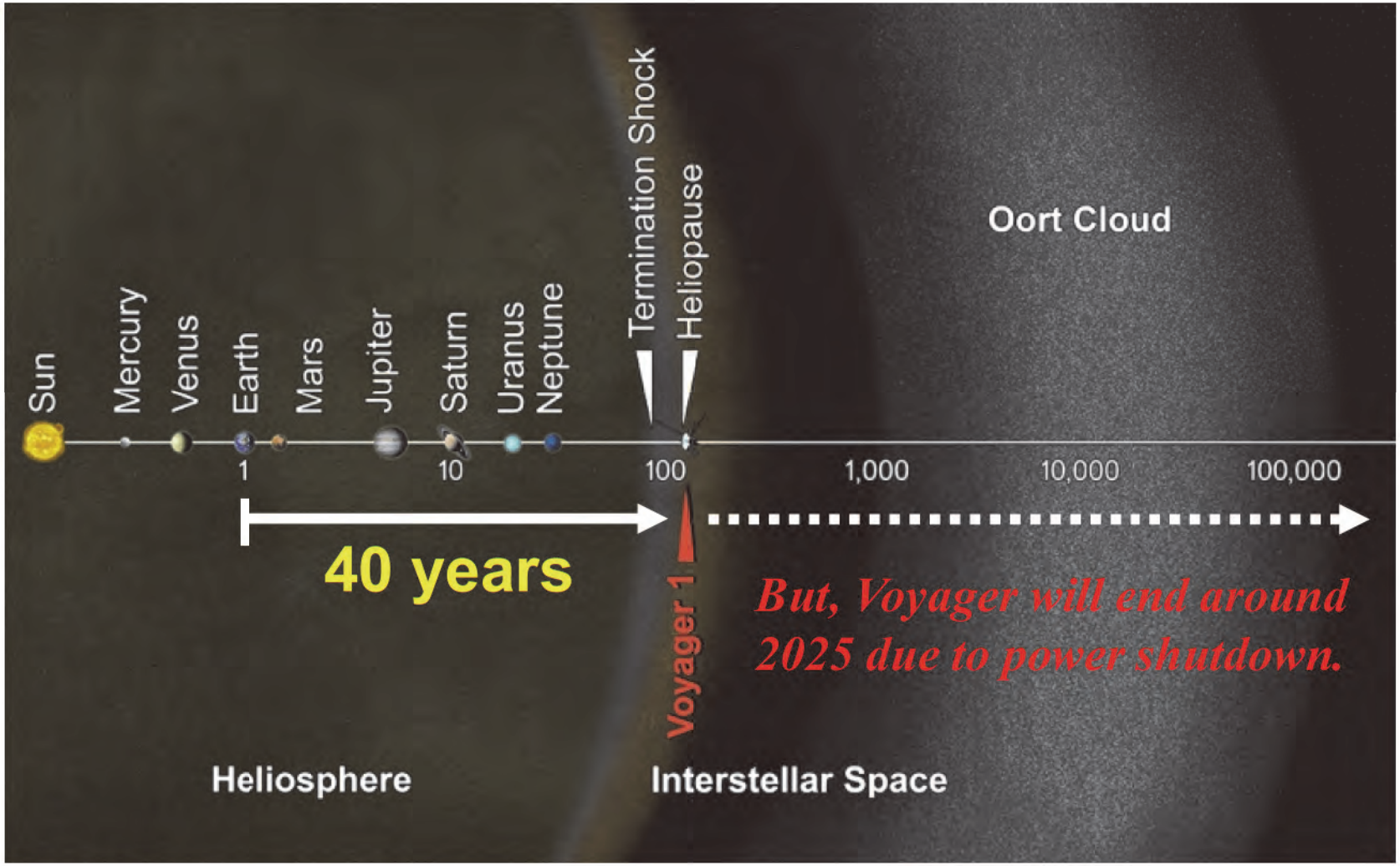


Source: NASA / Penn State Univ.

Voyager into Interstellar Space

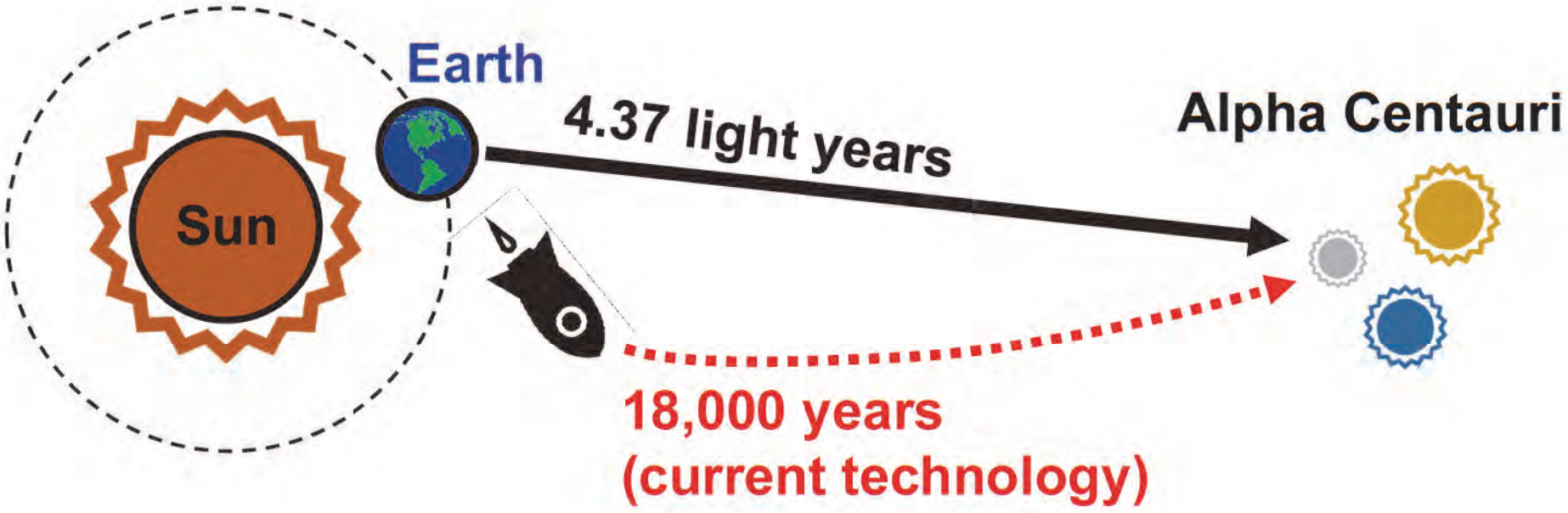
Source: www.nasa.gov

Interstellar Missions



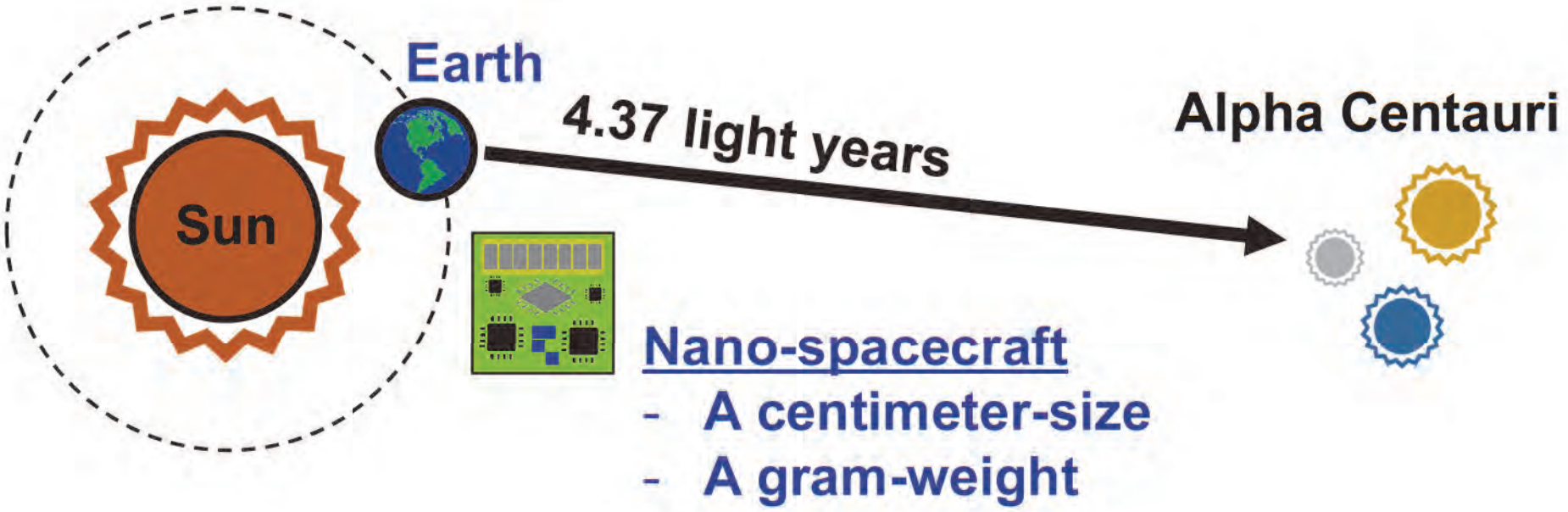
Source: www.nasa.gov

Journey to Alpha Centauri



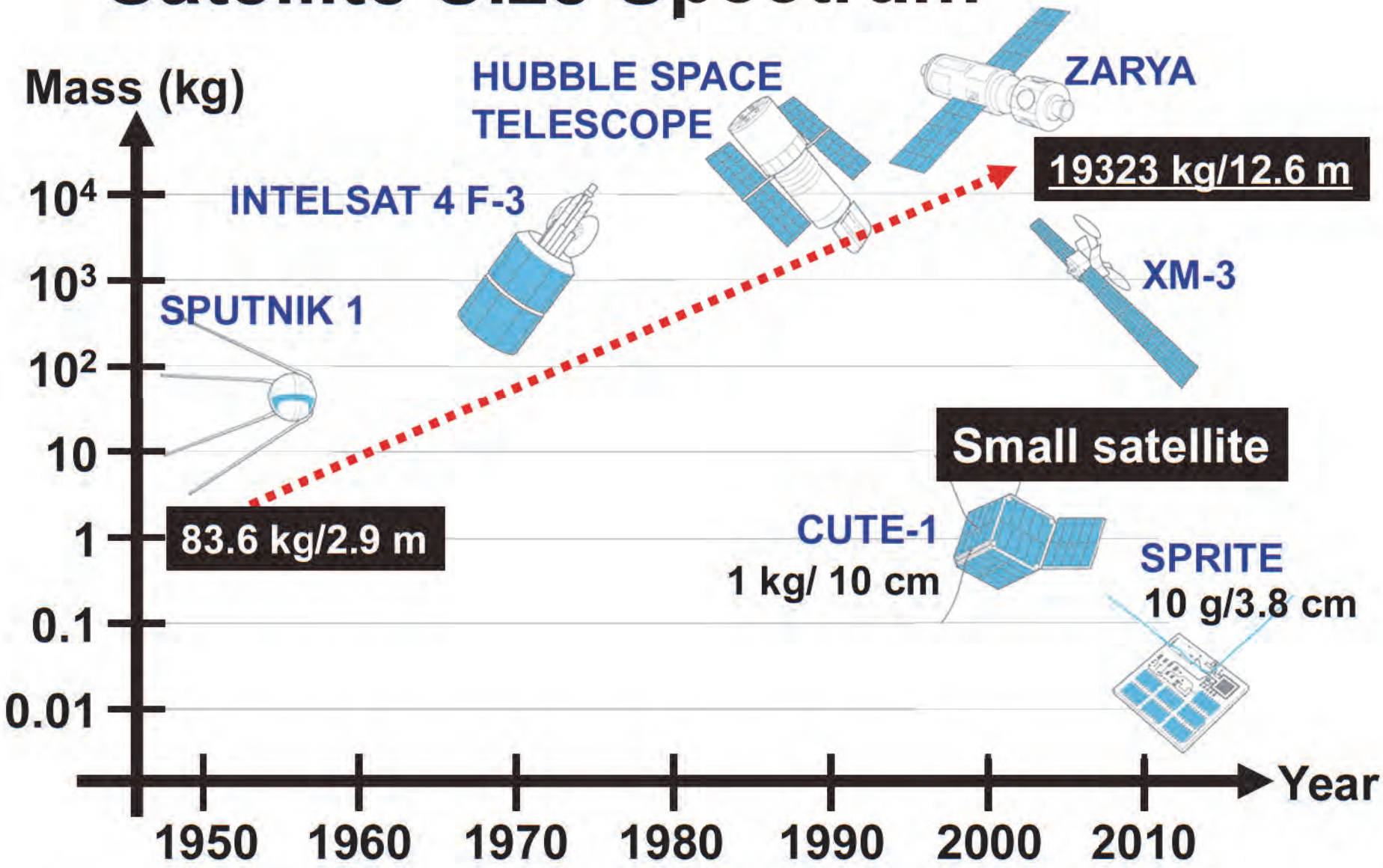
- **Alpha Centauri**
  - The nearest star from Sun (4.37 light years)
  - The fastest spaceship takes 18,000 years.

Spacecraft-on-a-Chip



- **Spacecraft-on-a-Chip: nano-spacecraft**
  - **Theoretical speed is one-fifth of light speed.**
  - **Interstellar mission can be possible in 20 years.**

Satellite Size Spectrum



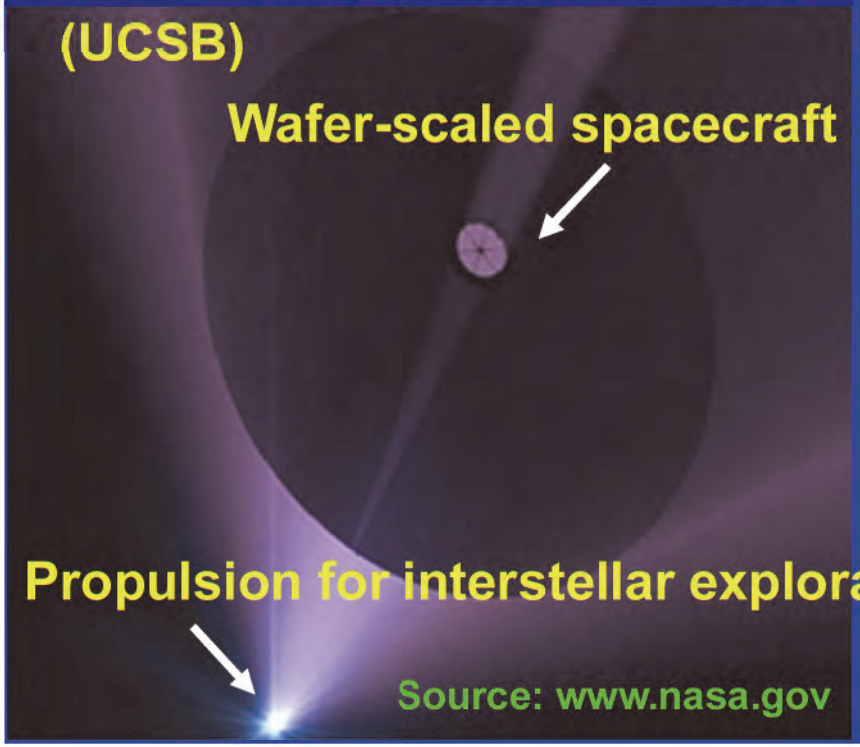
Source: IEEE Spectrum

Nano-Spacecraft Technology

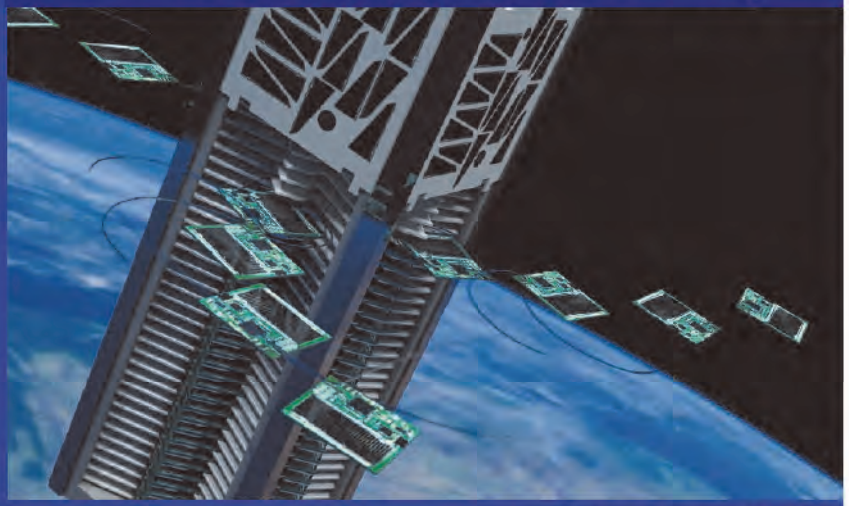
CubeSat (Cal Poly, Stanford Univ.)

Source: www.nasa.gov

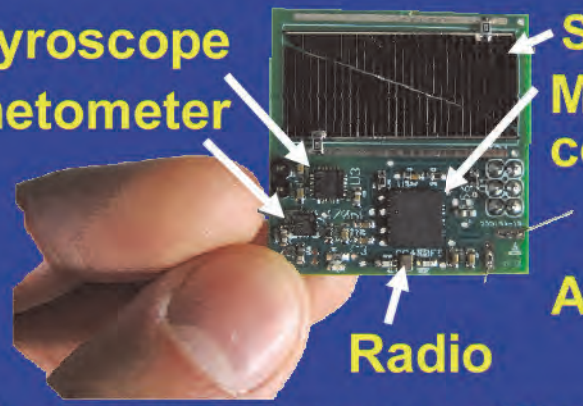
Directed energy interstellar study (UCSB)



KickSat (Cornell Univ.)

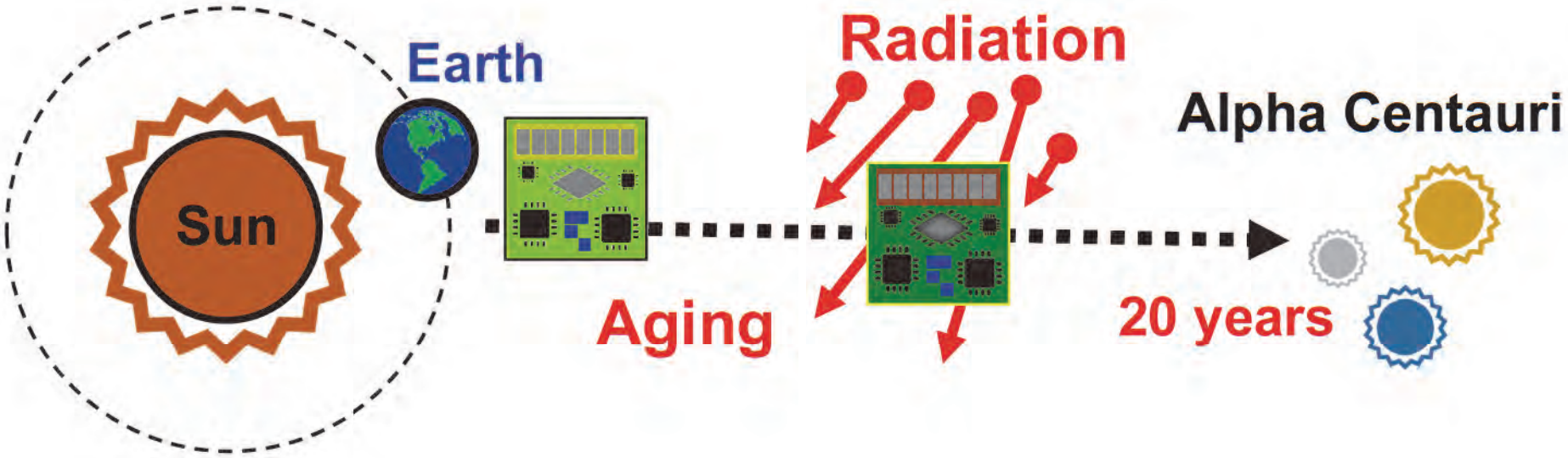


Source: N. Jones, Nature, vol. 534, p.15, 2016.



Source: https://commons.wikimedia.org

Technological Issues

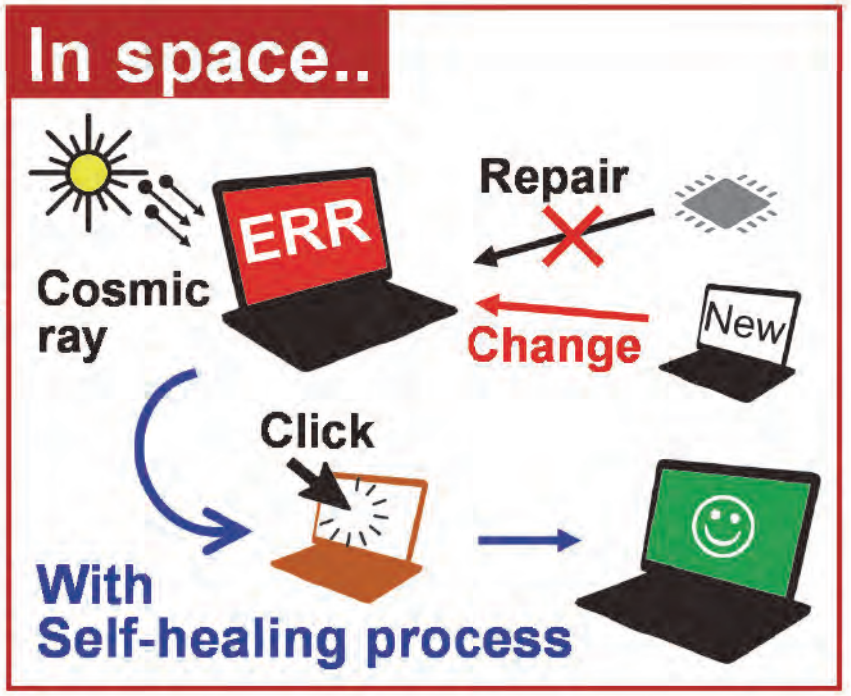


- Lifetime of COTS* chips ~ 10 years
  - ➔ Deep space mission > 20 years
- Limited radiation hardening strategy
  - ➔ No flight path control and radiation shielding

*COTS: commercial off-the-shelf

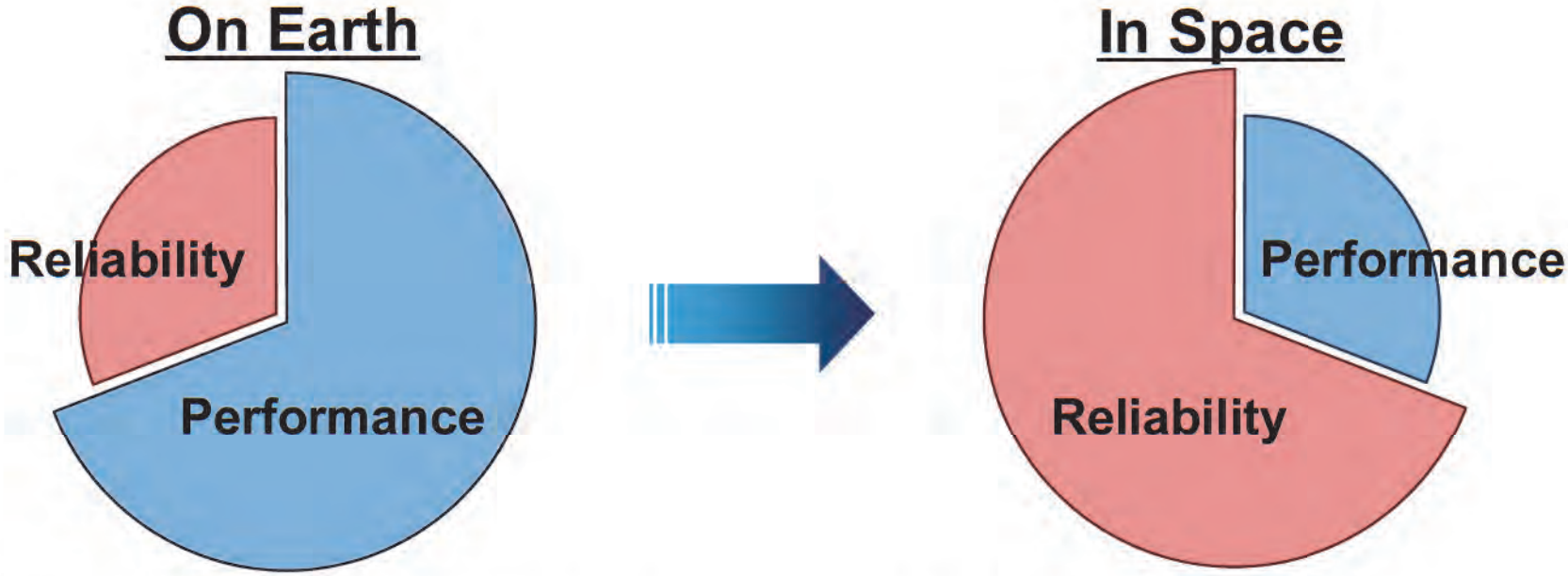
Current Status

On earth,
repairing or replacing components
is available with low cost and short time.



In space,
a service center is not available.
Therefore, new technology
such as self-healing process is required,
which greatly saves cost and time
for deep space exploration.

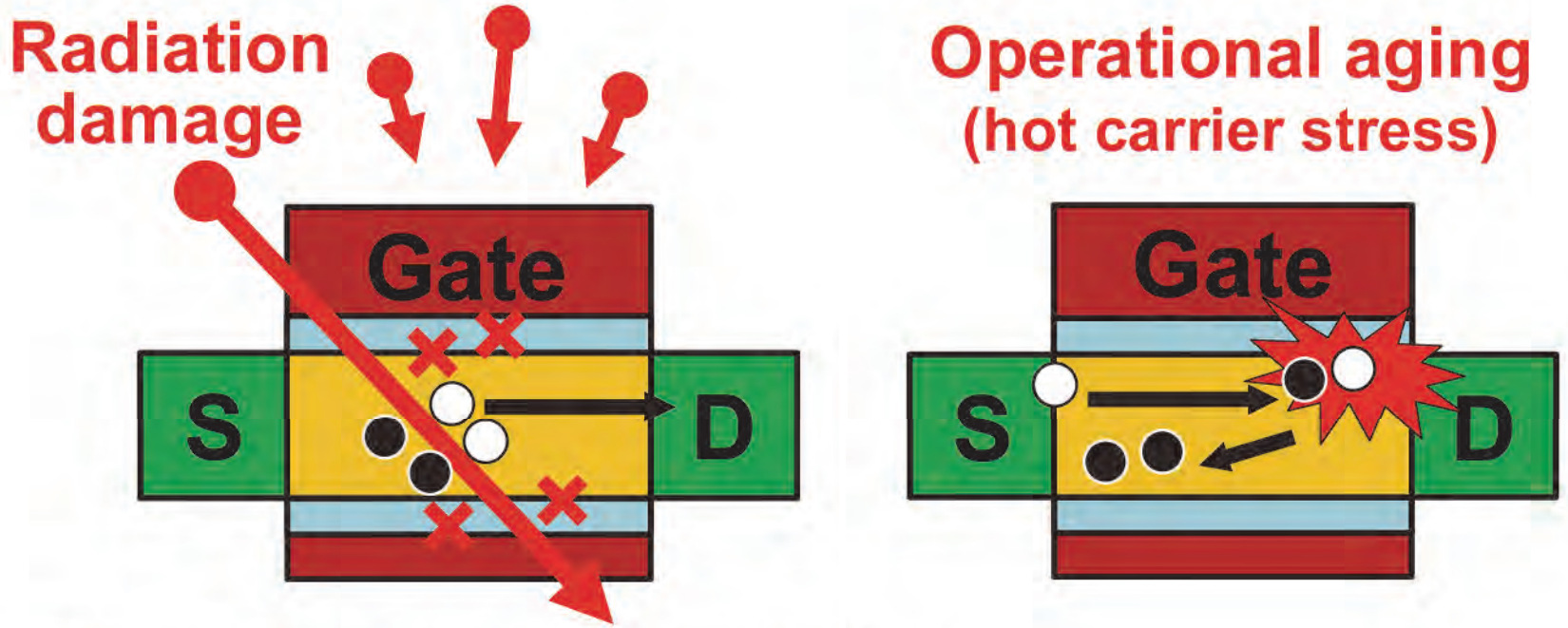
Important Features of CMOS



- **Focus on performance**
  - ✓ High performance (HP)
  - ✓ Low operating power (LOP)
  - ✓ Low standby power (LSTP)
- **Focus on reliability**
  - ✓ Single-event effect (SEE)
  - ✓ Total ionizing dose (TID)
  - ✓ Displacement damage

Source: ITRS roadmap (2012) and R.C. Lacoe, IEEE Trans. Nucl. Sci. (2008)

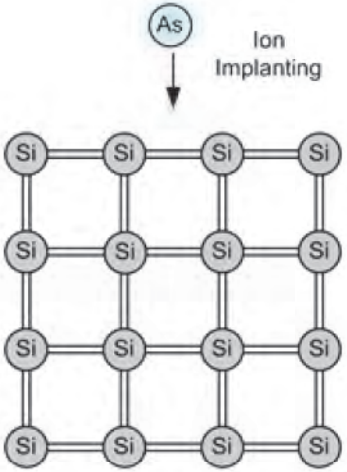
Degradation Mechanisms

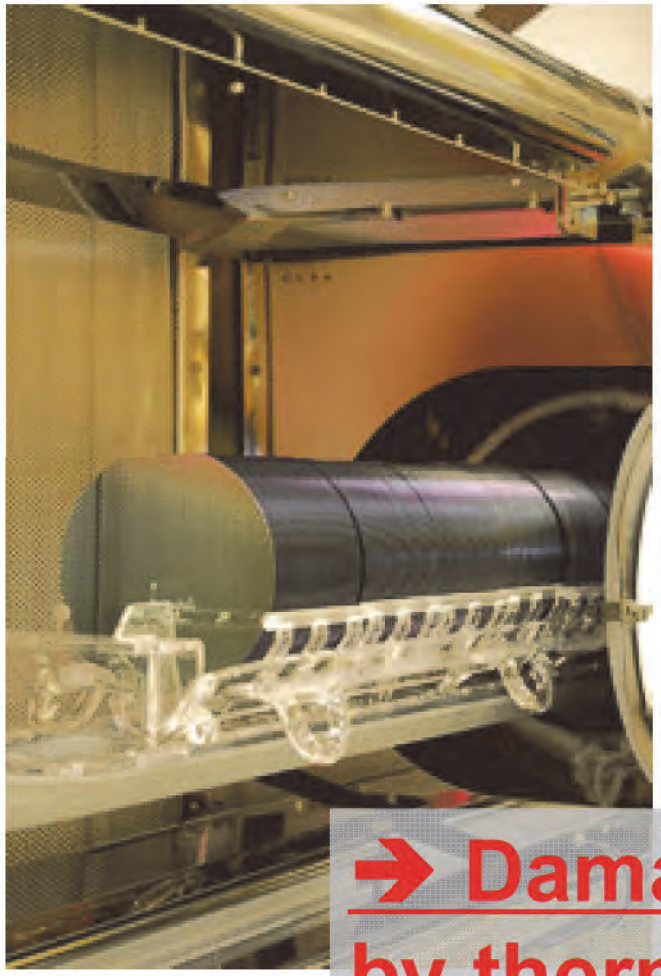


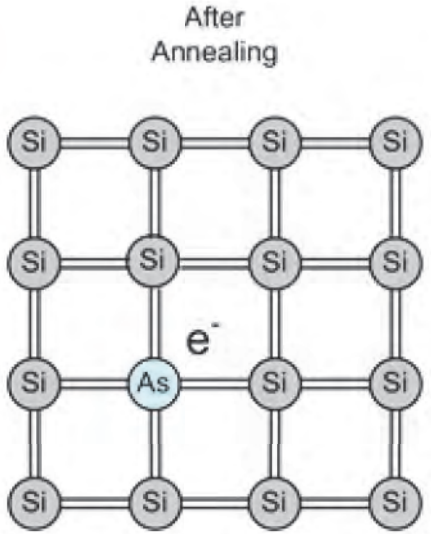
- Sources of device degradation
  - Radiation: high energy particle
  - Operation: electric field

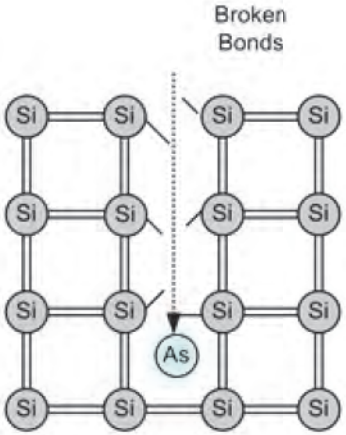
} Trapped charges / Interface states

Example of Annealing/Baking









➔ Damage recovery by thermal annealing

On-Chip High Temperature Annealing of PMOS Dosimeter

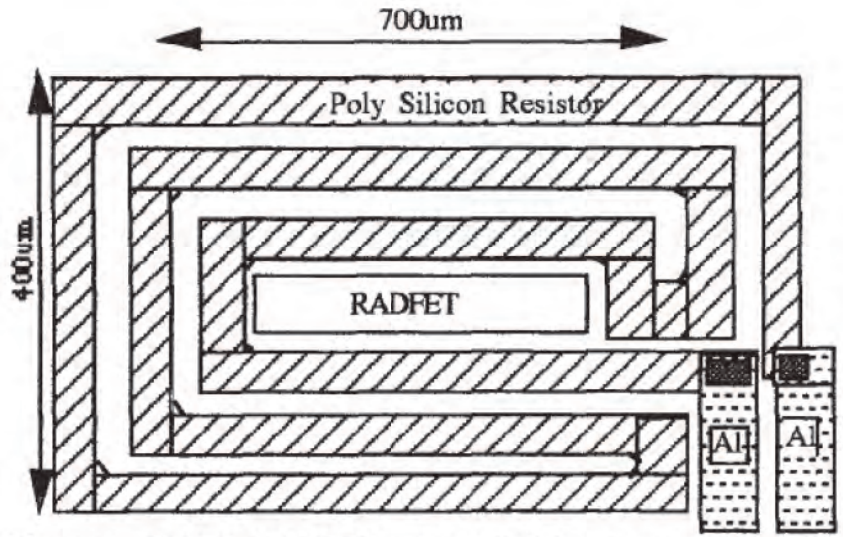
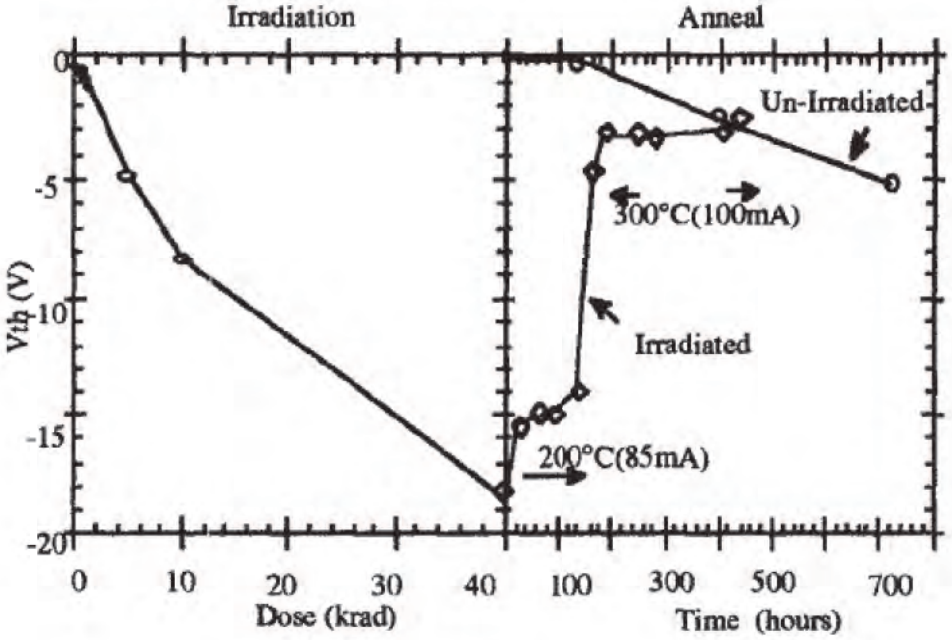
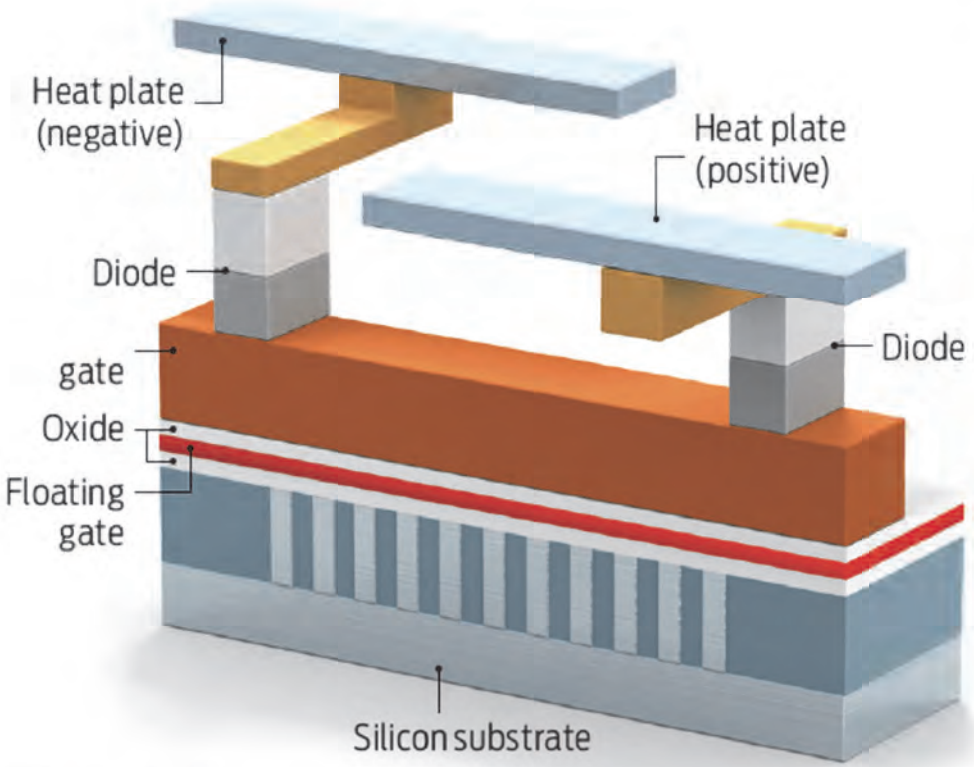


Figure 1. PMOS RADFET surrounded by a serpentine poly-silicon resistor, R=200Ω.

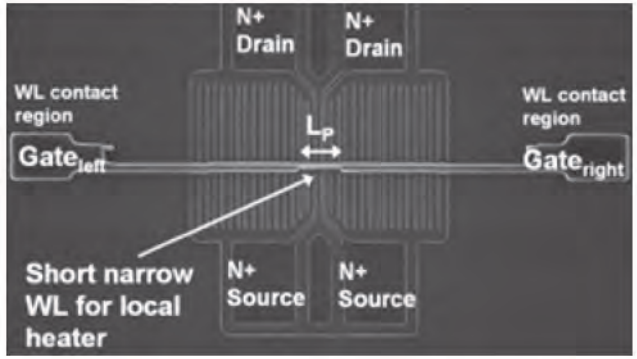


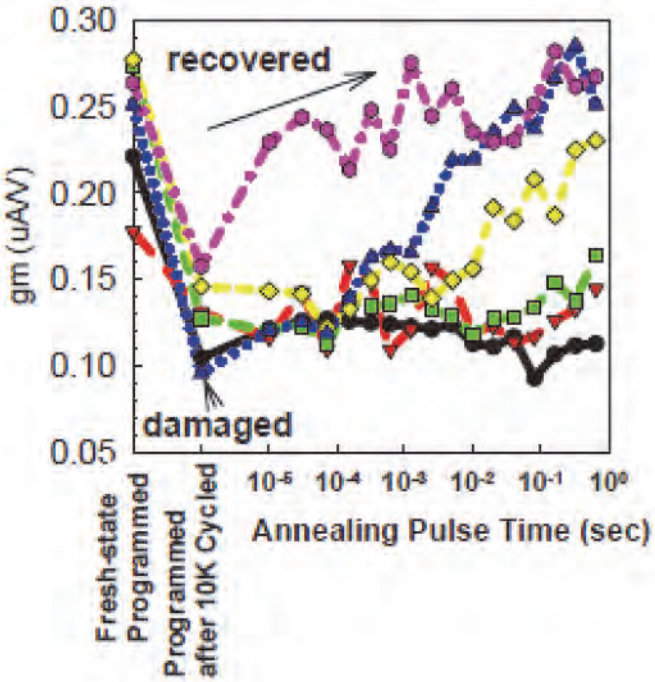
A. Kelleher et al., RADECS 95

Radically Extending the Cycling Endurance of Flash Memory



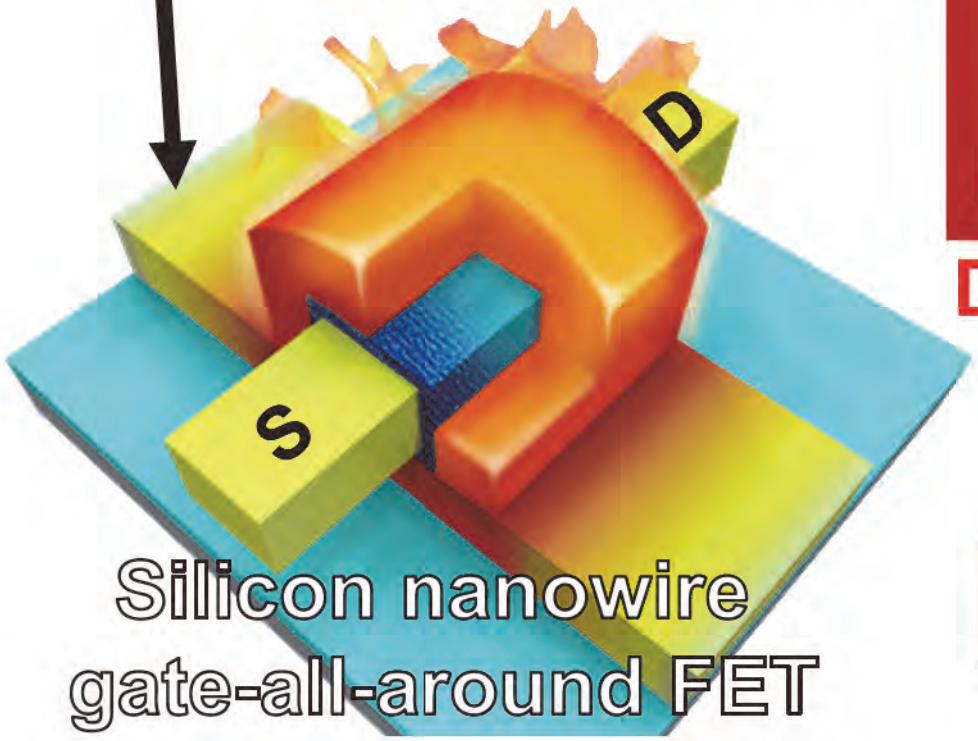
H.-T. Lue et al., IEDM 2012



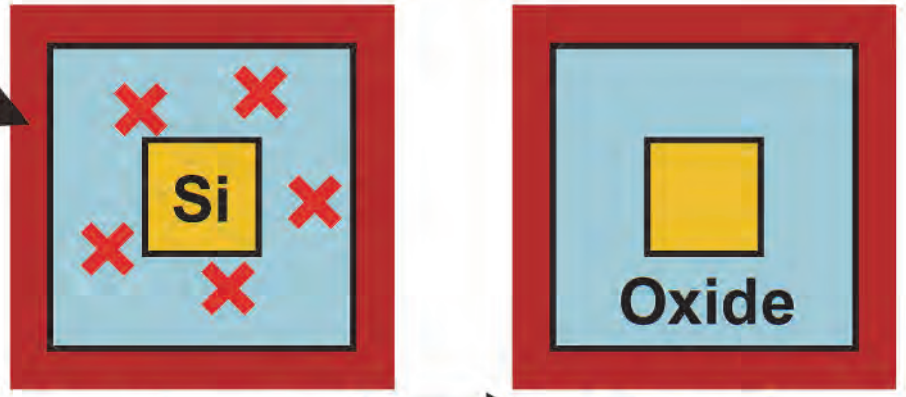


Sustainable Space Electronics

Nano-heater (gate)



Silicon nanowire
gate-all-around FET



Damaged → Fresh

Trapped charges

Interface states

Thermal annealing

Demonstration of highly reliable logic transistor, high-speed DRAM, and Flash memory

Outline

- Introduction
- **Design of Sustainable Electronics**
  - **Silicon Nanowire Gate-All-Around FET**
  - **Built-in Nano-Heater**
- Pristine Device
- Damage and Recovery
- Applications
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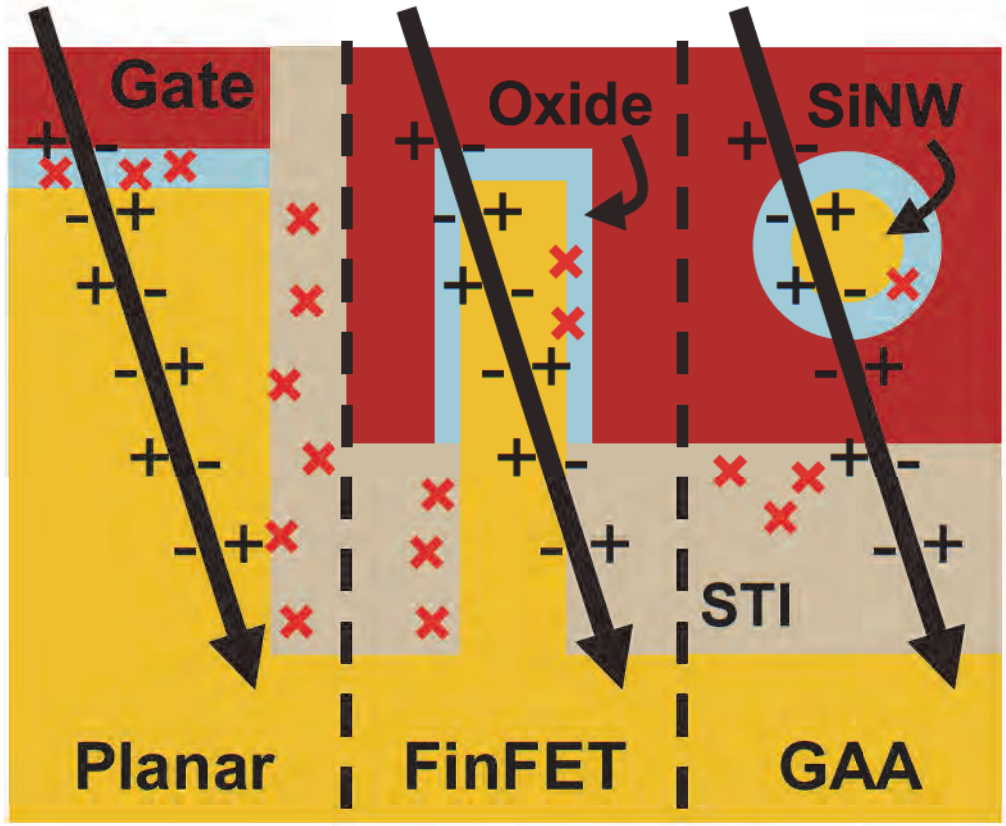
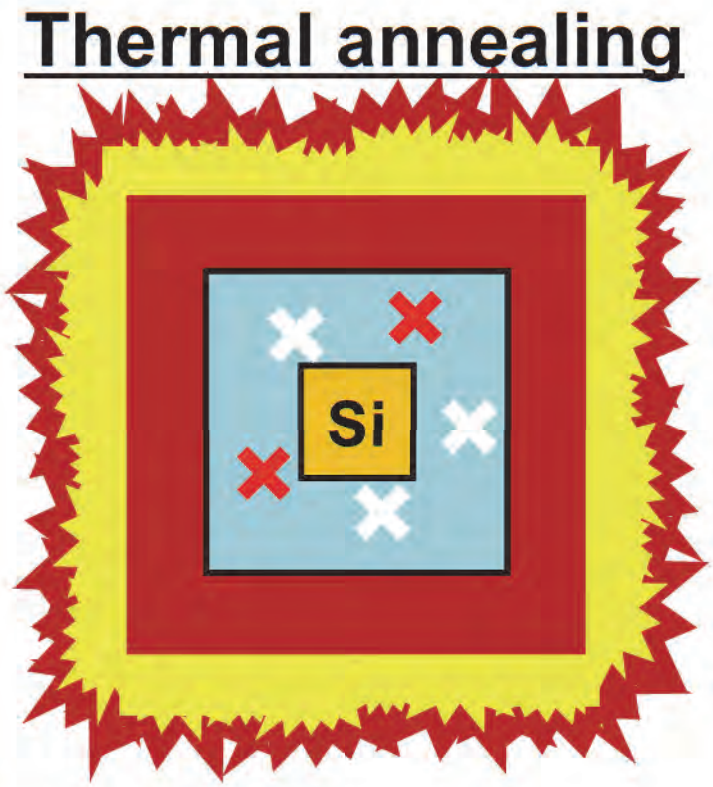
Gate-All-Around (GAA) FET

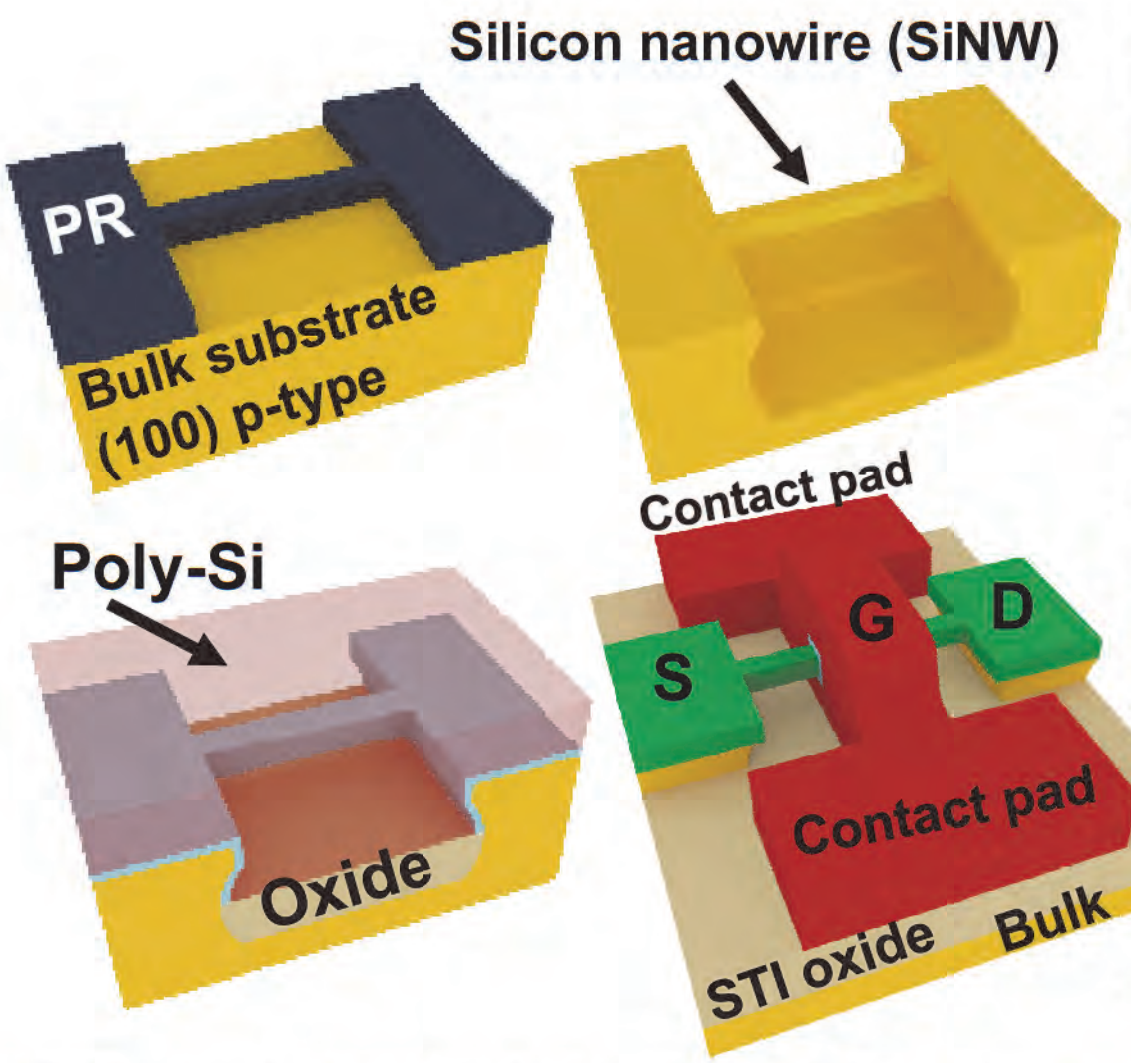




Inherent structural advantages

for radiation and self-healing process

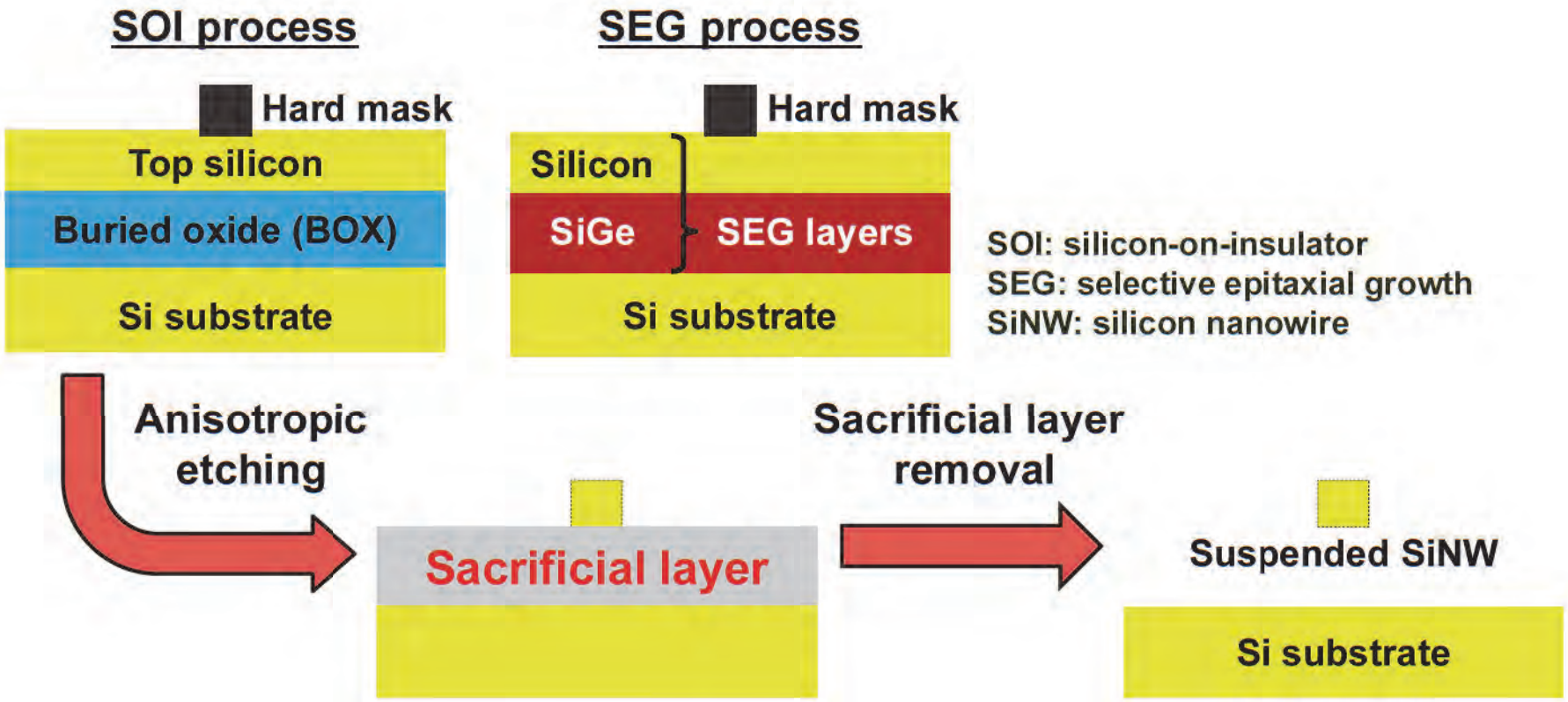
Process Flow



- Bulk substrate
- **Suspended SiNW by one-step etching route**
- Sacrificial oxidation
- Oxide dep. and CMP*
- Partial oxide etching (STI**)
- Thermal oxidation
- *in-situ* n^+ poly-Si dep.
- Poly-Si CMP and HM*** dep.
- **Dual pads gate patterning**
- Spacer formation
- S/D implantation
- RTA**** and H_2 annealing

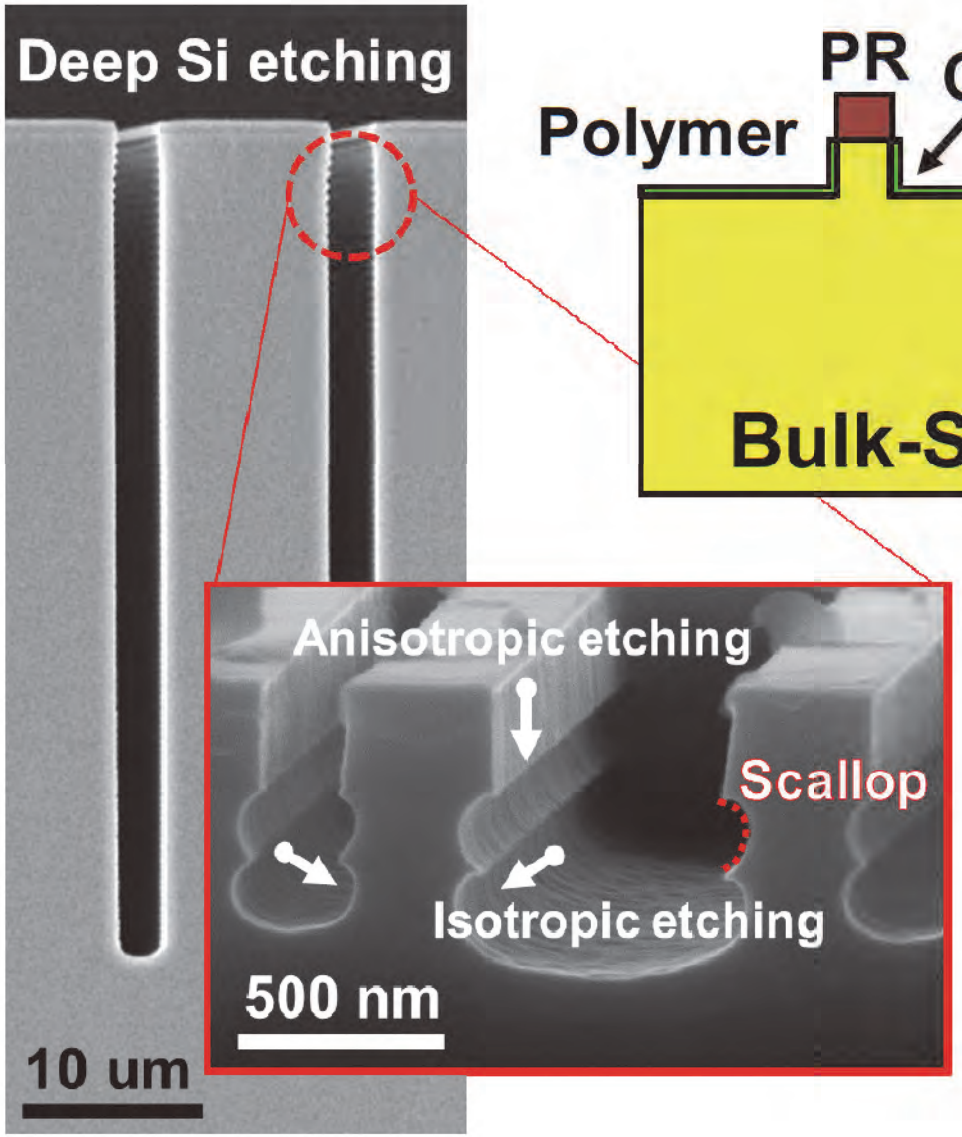
*CMP: chemical mechanical polishing, **STI: shallow trench isolation,
***HM: hard mask, ****RTA: rapid thermal annealing

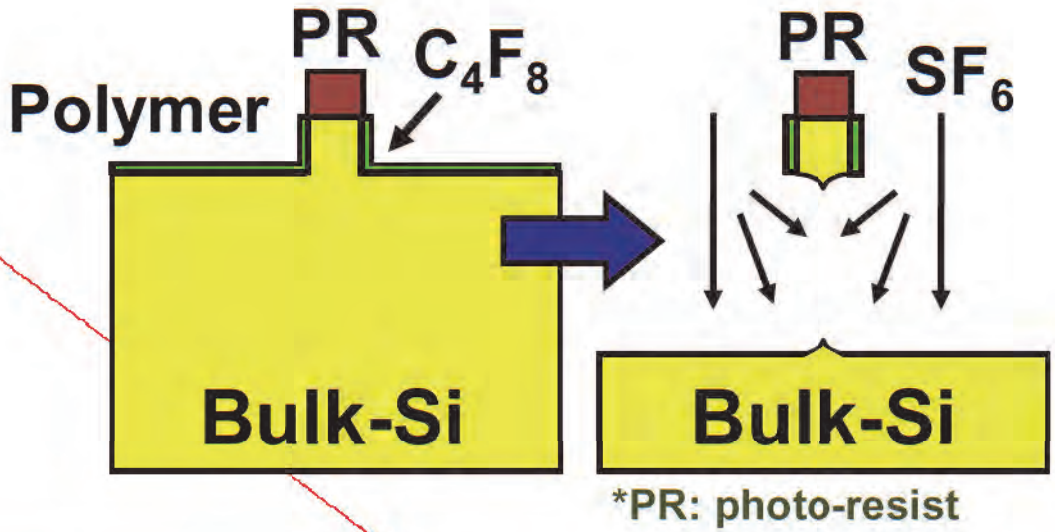
Formation of Suspended SiNWs



- **Suspended SiNW: basic building block for GAA FETs**
- **Previous approaches: SOI substrate and epitaxial growth**
  - CMOS low-compatible, high cost, and low throughput

SiNW by One-Step Etching Route





Anisotropic etching

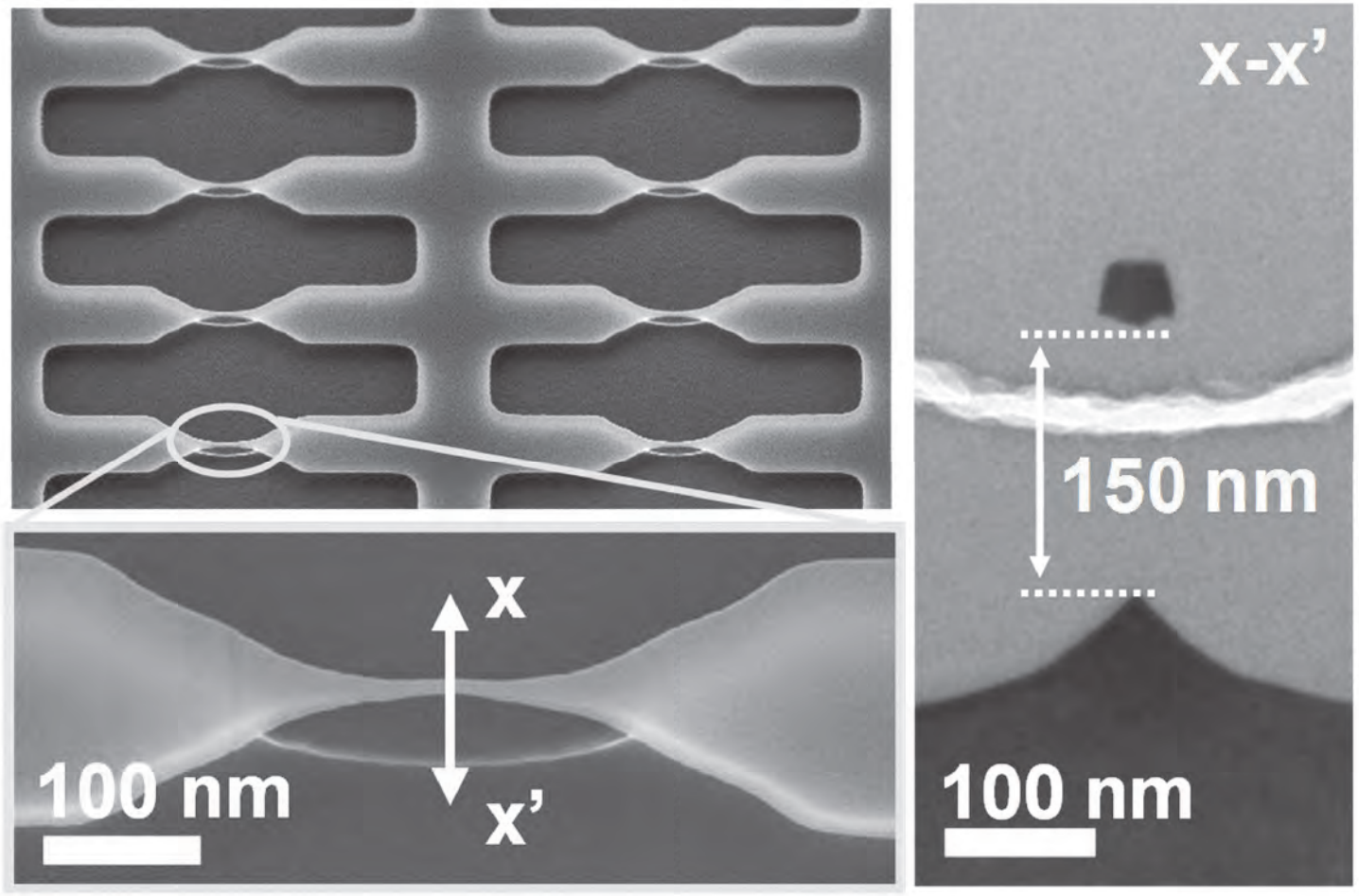
↓

Polymerization (passivation: C_4F_8)

↓

Isotropic etching (SF_6)

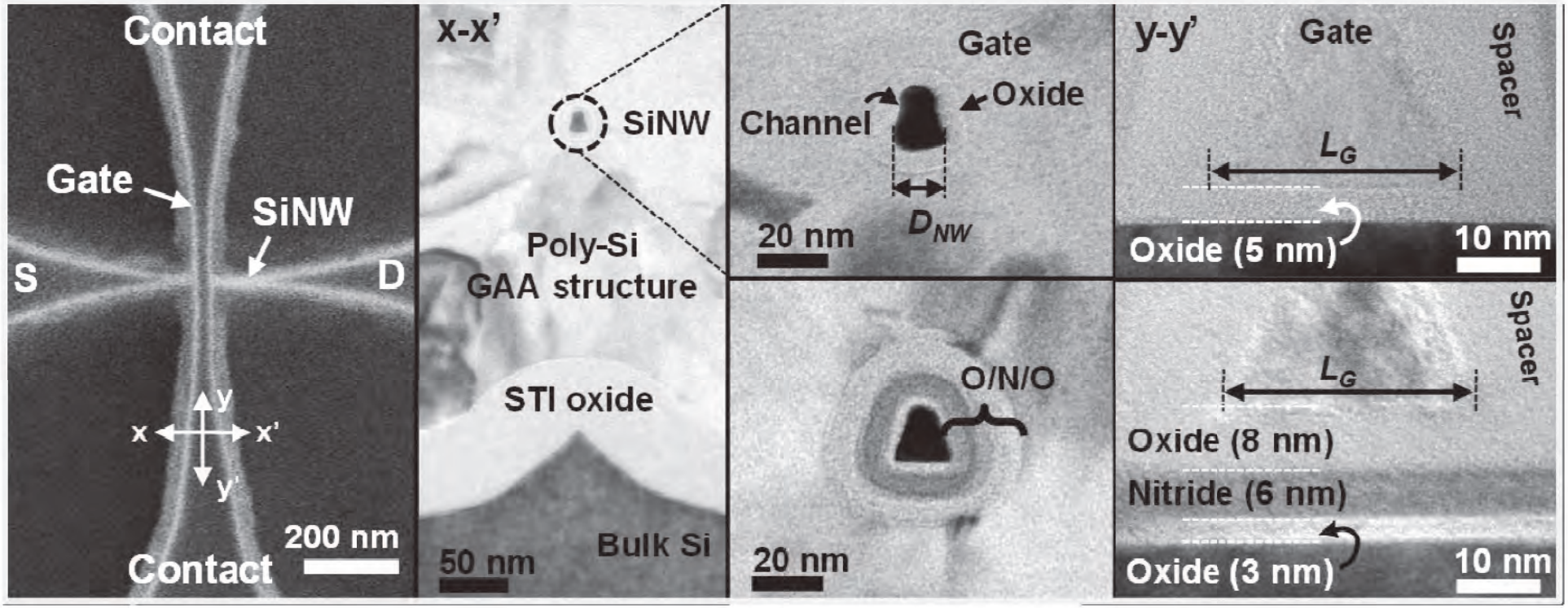
SiNWs from a Bulk Substrate



CMOS compatible one-step etching route

D.-I. Moon et al., IEEE EDL 32 (4)

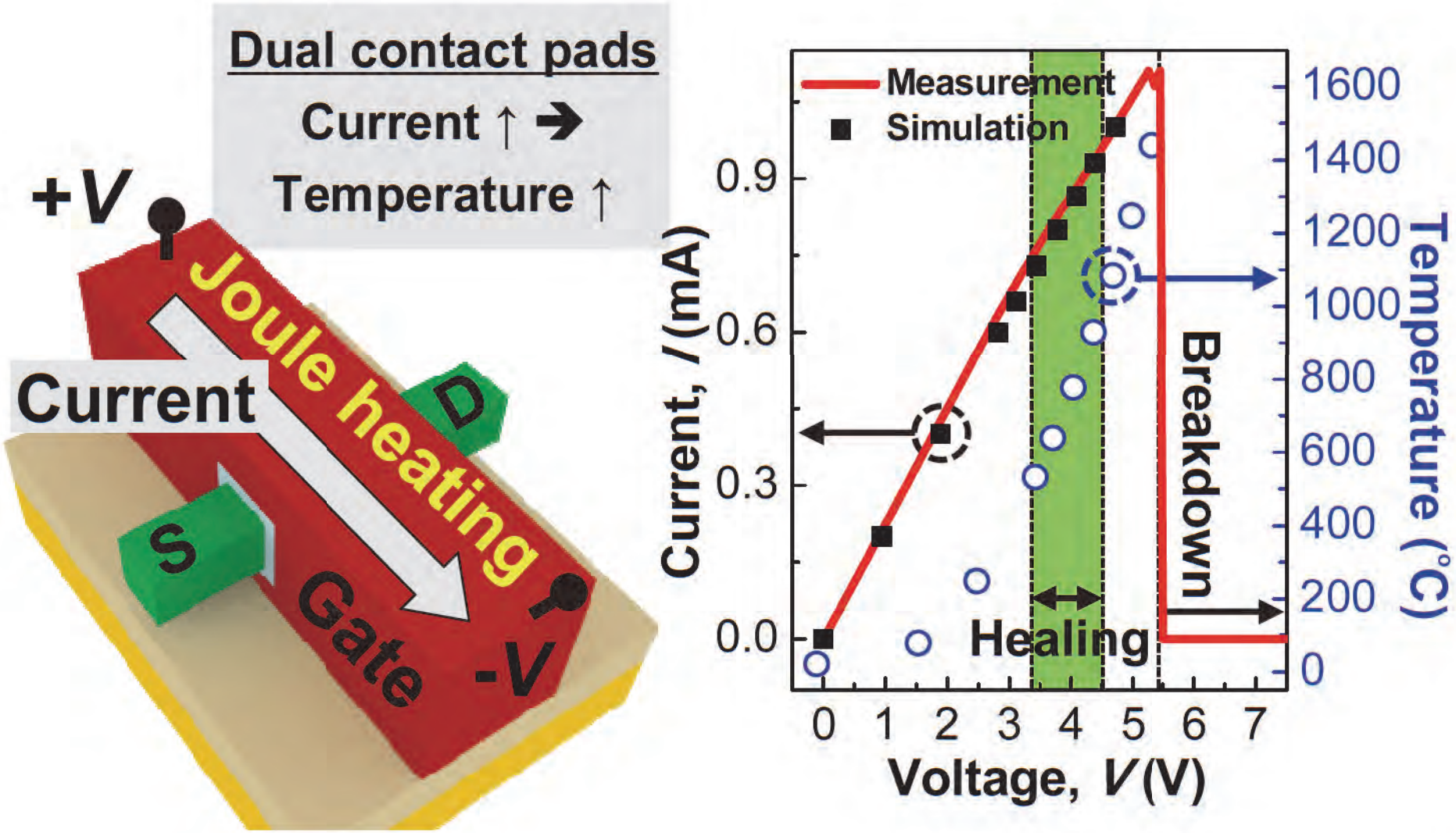
Fabricated Devices



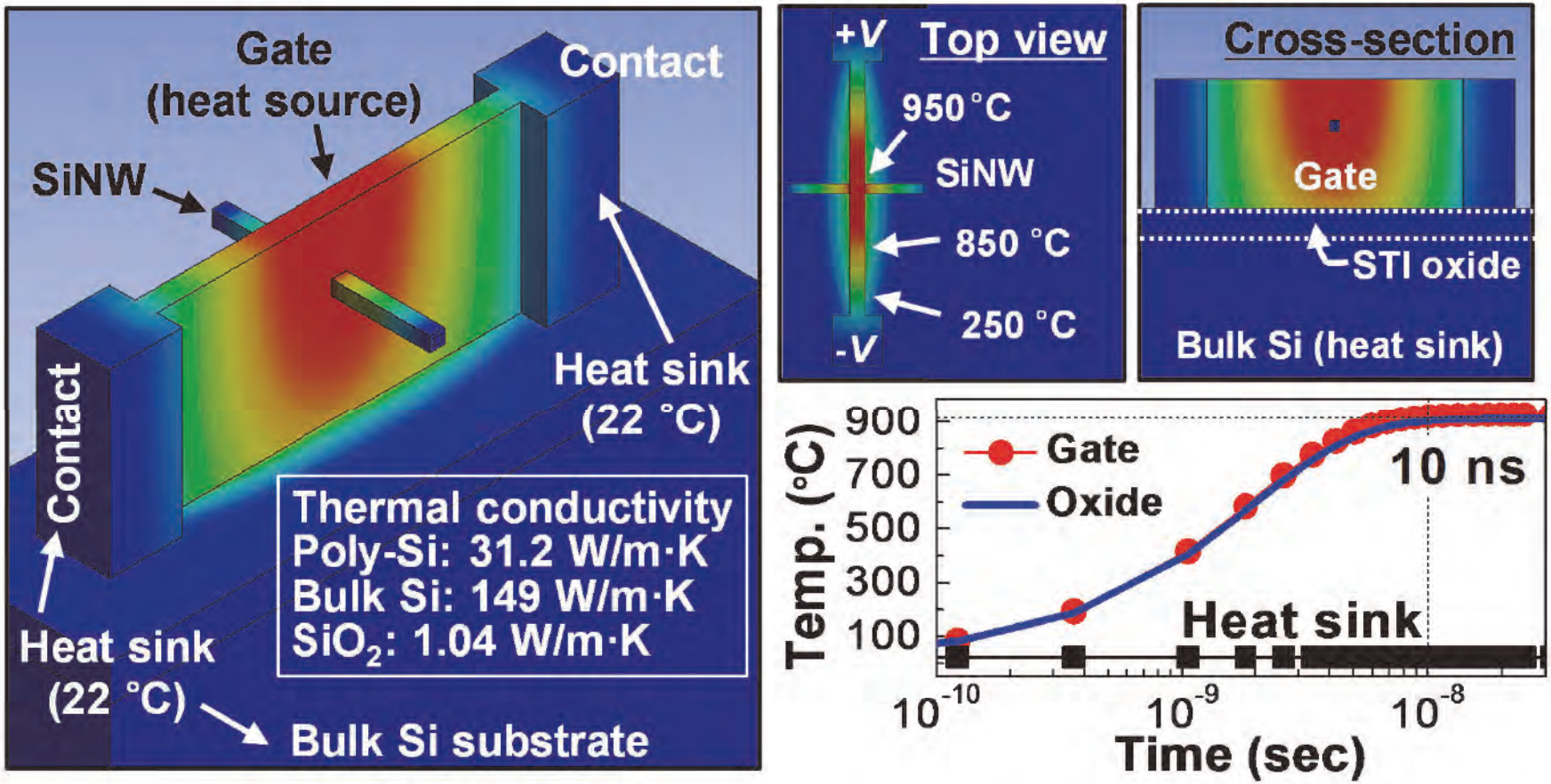
Highly scaled SiNW GAA FET on a bulk substrate

- Gate length (L_G) = 30 nm, SiNW diameter (D_{NW}) = 15 nm
- Gate dielectric: thermal oxide, O/N/O stacks

Built-in Nano-Heater



Electro-Thermal Simulation



Temperature by the nano-heater > 900 °C, 10 ns

Heat transfer from the gate to the dielectric

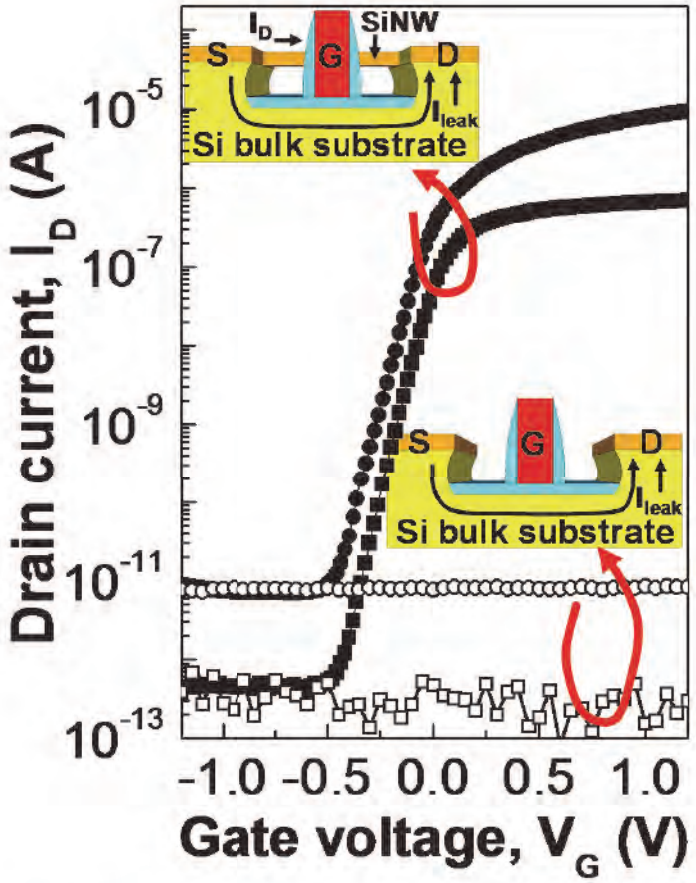
Outline

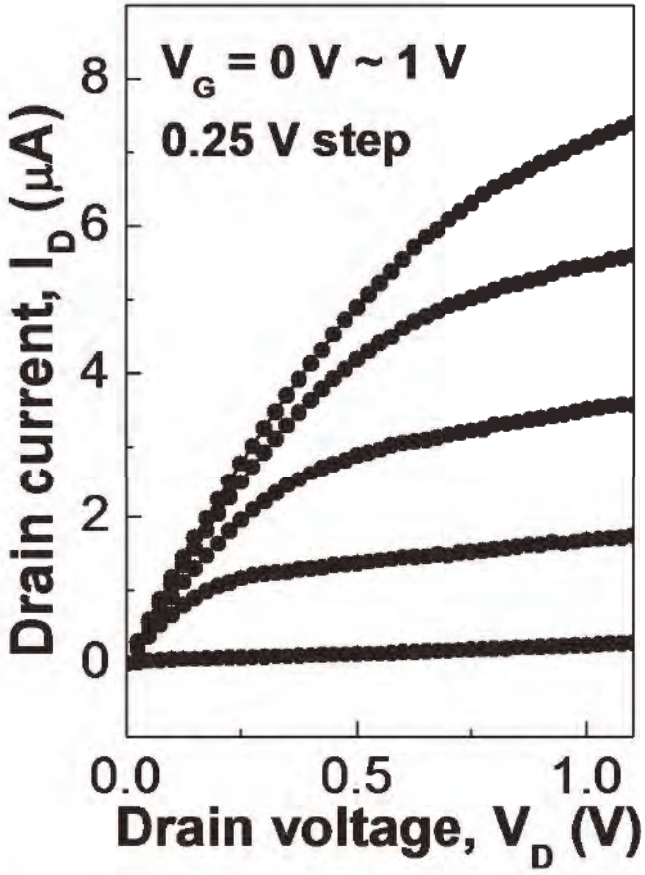
- Introduction
- Design of Sustainable Electronics

- **Pristine Device**
  - **Electrical Characteristics**
  - **Short-Channel Effects**

- Damage and Recovery
- Applications
- Conclusions

Electrical Characteristics



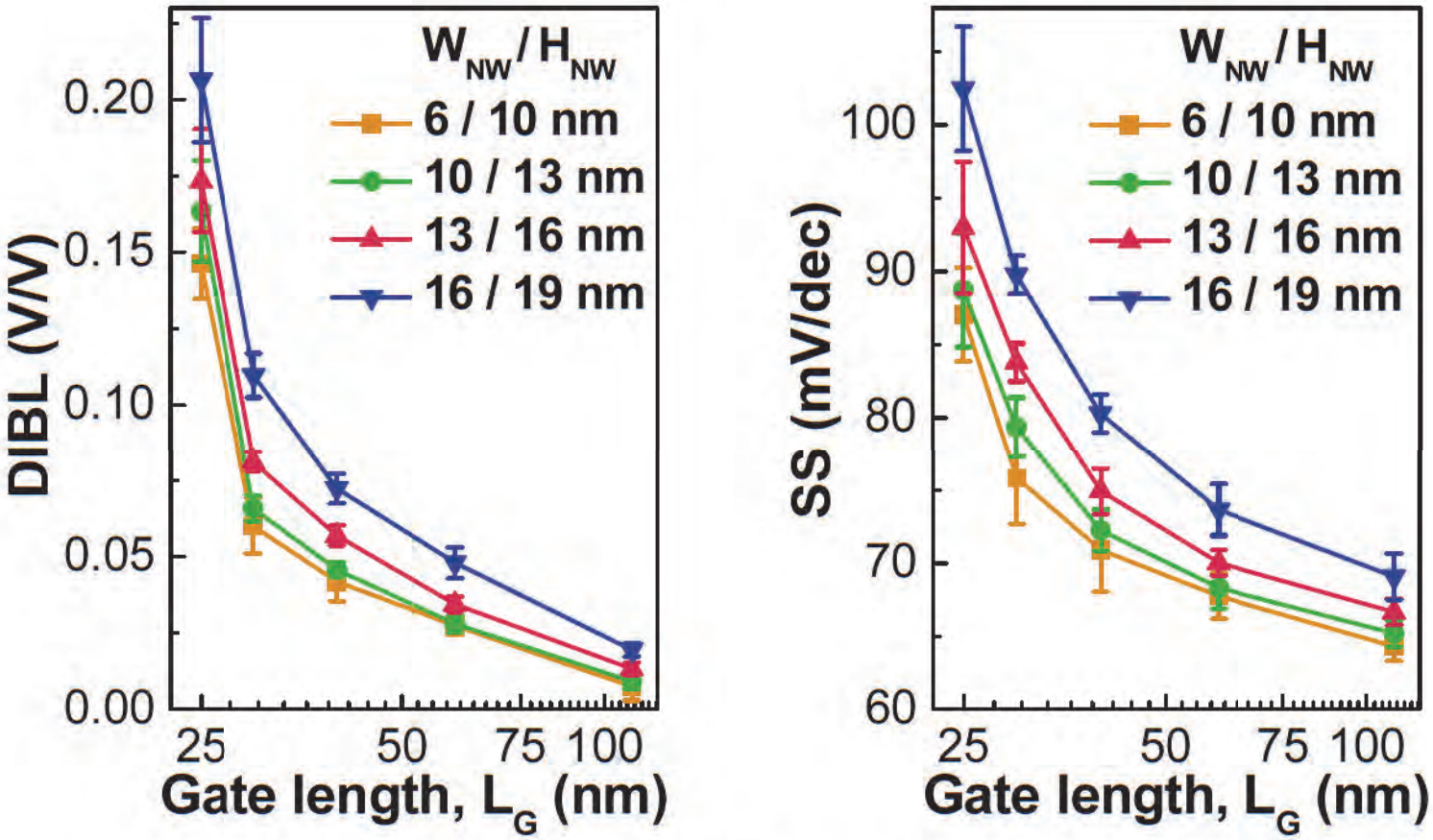


- **Silicon nanowire gate-all-around FET on a bulk substrate**

DIBL: 150 mV/V, SS: 87 mV/dec, $I_{ON}/I_{OFF} > 10^6$

D.-I. Moon et al., IEEE EDL 32 (4)

Short-Channel Effects (SCEs)



Excellent immunity against SCEs despite the device built on a bulk substrate ➔ GAA structure with SiNW channel

D.-I. Moon et al., IEEE EDL 32 (4)

Outline

- Introduction
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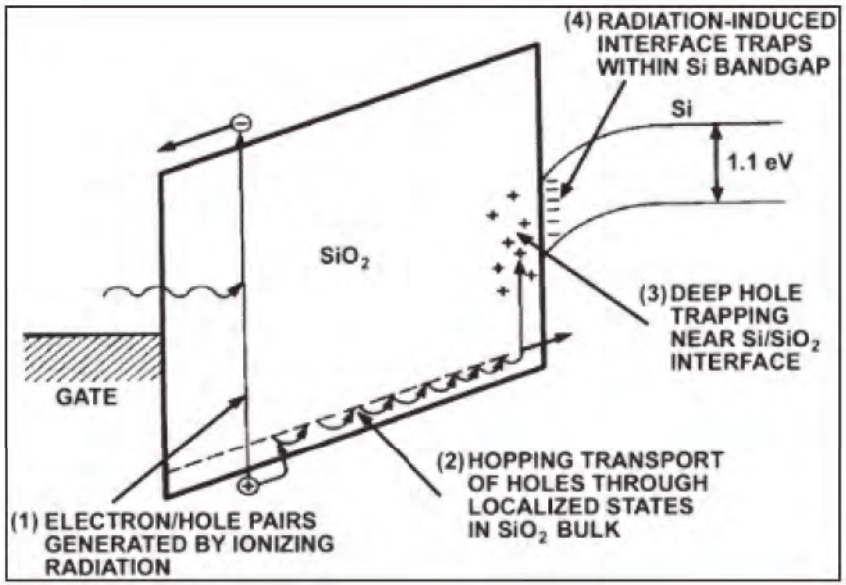
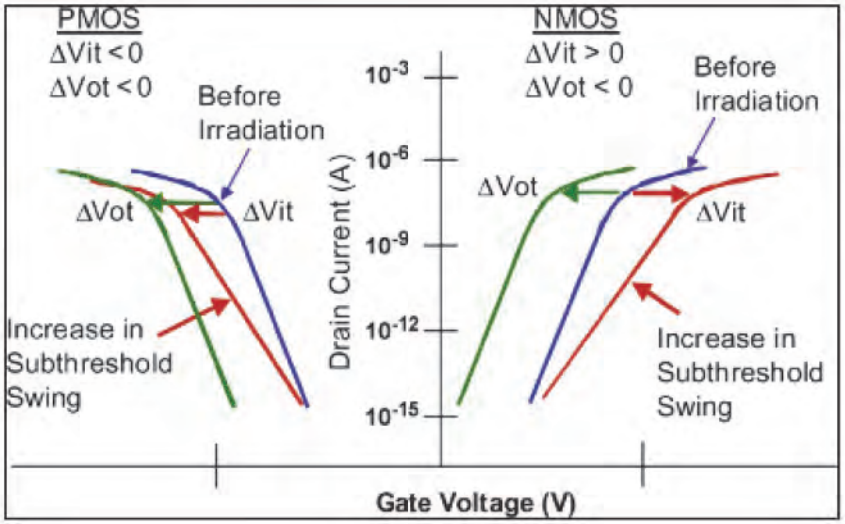
- Pristine Device

- **Damage and Recovery**
  - **Radiation Aspect**
  - Operation Aspect

- Applications
- Conclusions

Total Ionizing Dose (TID)

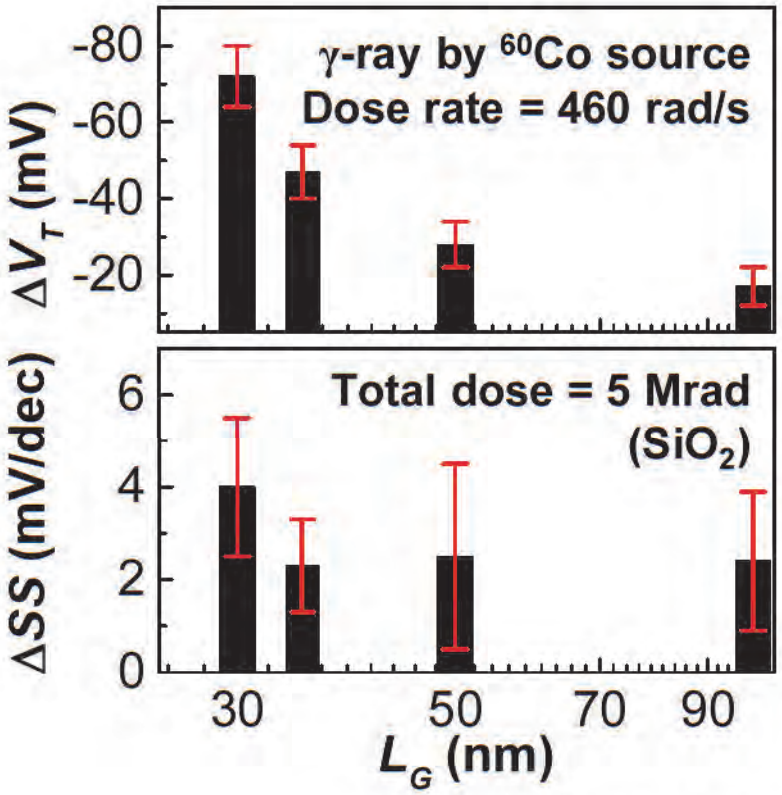


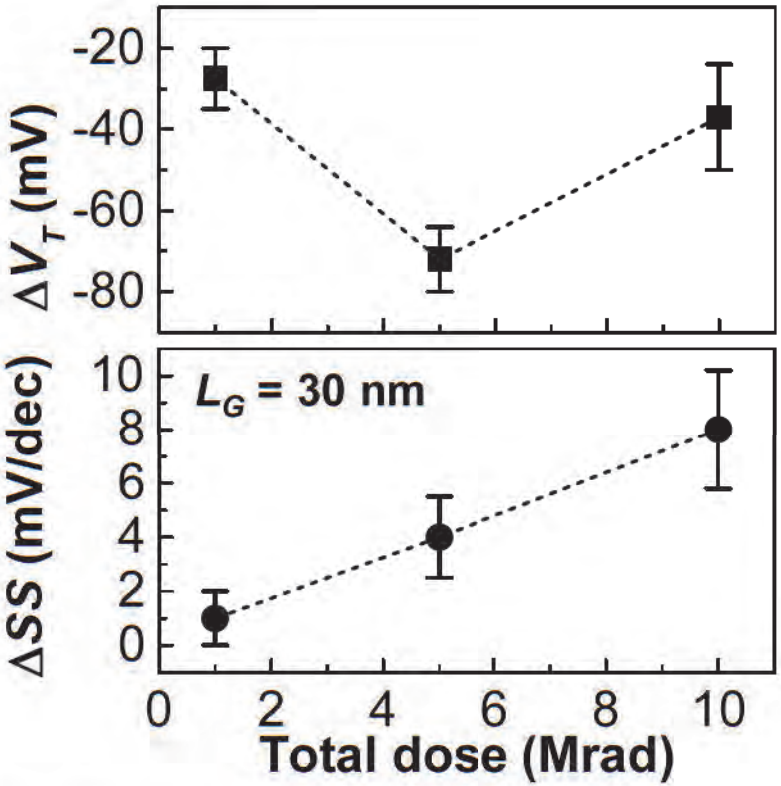


- **<u>Semi-permanent device degradation</u> caused by radiation-induced fixed charge and interface trap**
- **Representative phenomena**
  - Threshold voltage shift
  - Increment of subthreshold swing
  - Reduction in on/off current ratio
- **<u>Accumulated damage</u> according to cumulative radiation dose**

T.R. Oldham et al., IEEE Trans. Nucl. Sci. (2003)
R.C. Lacoe, IEEE Trans. Nucl. Sci. (2008)

TID in SiNW GAA FETs

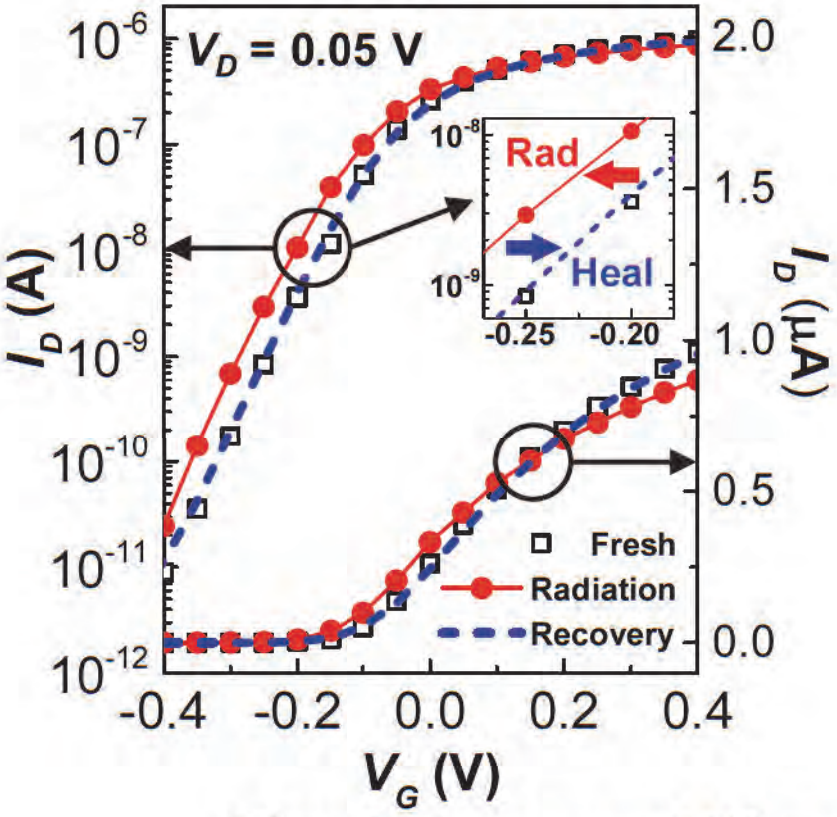


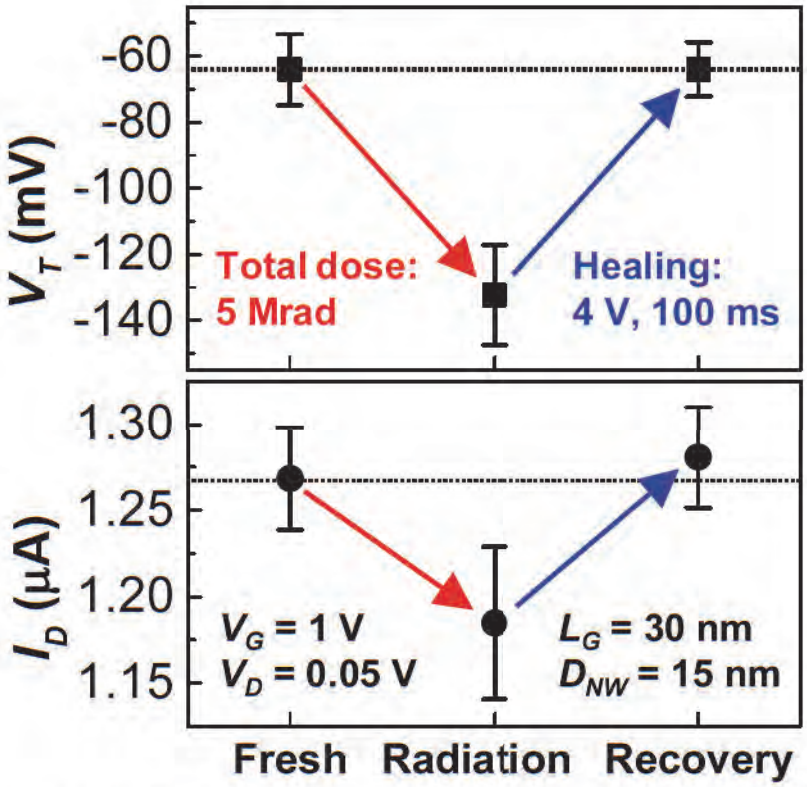


L_G ↓ ➔ TID effect ↑

Total dose ↑ ➔ V_T, *SS*, and I_D degradation

Recovery of TID Damages

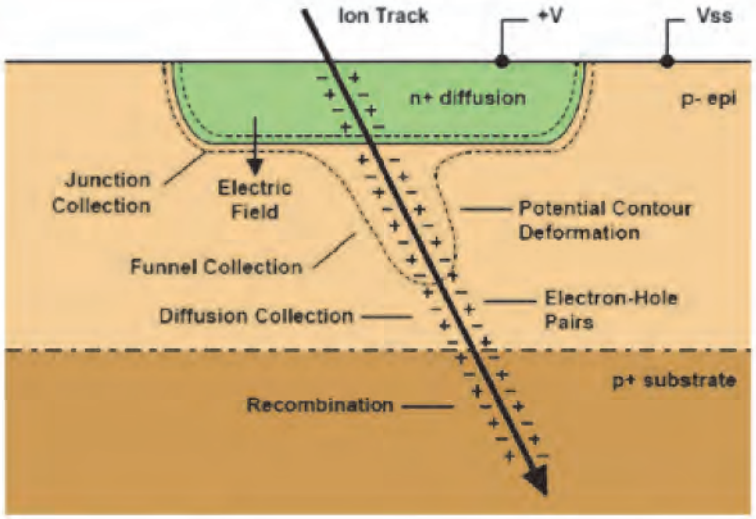


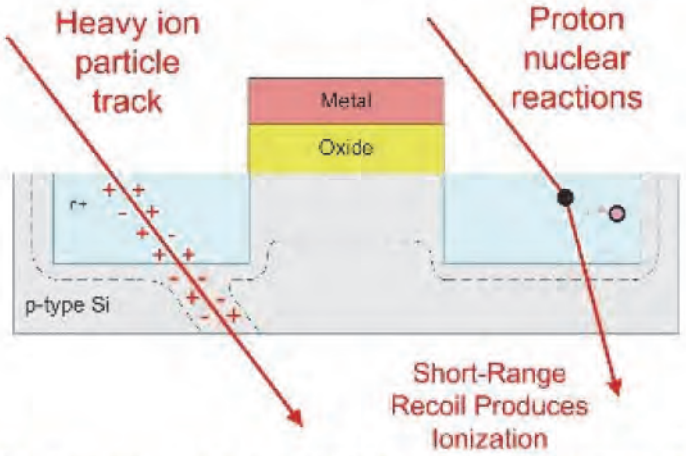


Healing conditions: ± 2 V for 200 ms

Complete recovery of V_T, *SS*, and I_D

Single Event Effect (SEE)

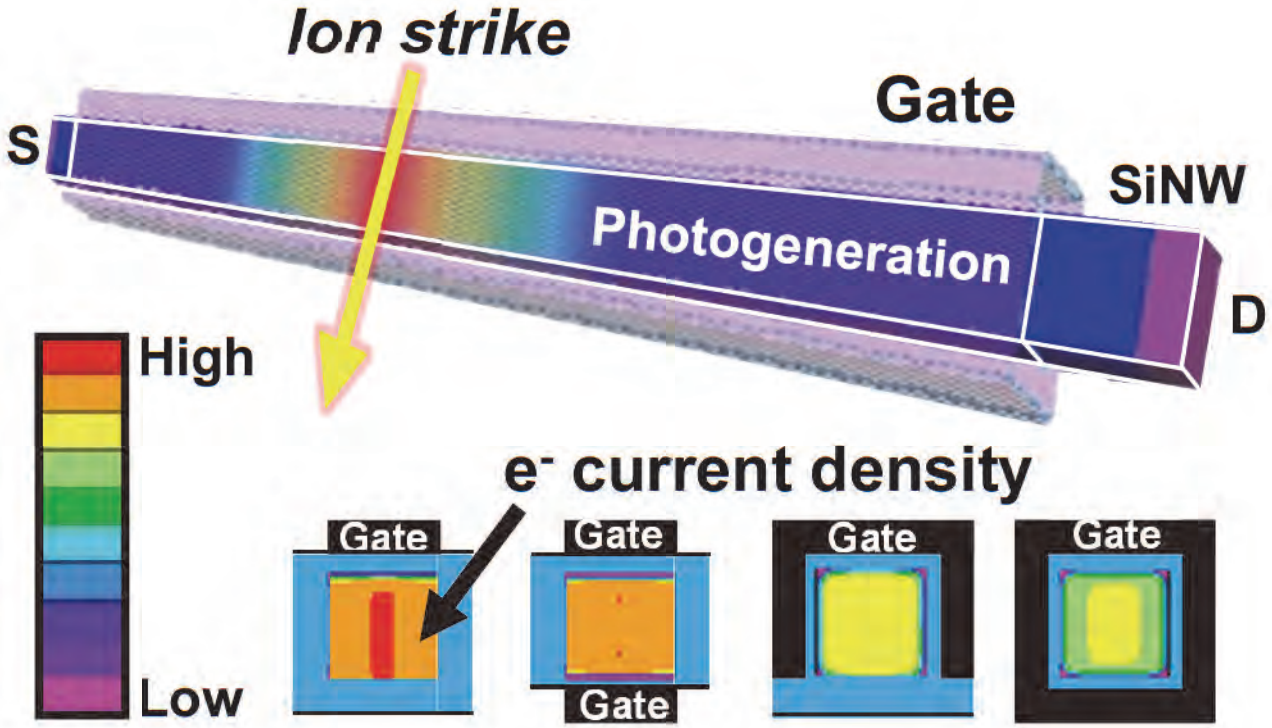




- **<u>Non-destructive malfunction (transient):</u> soft faults**
  - Single-event upset (SEU)
  - Single-event transient (SET)
  - Single/multiple Bit Upsets (S/MBU)
  - Single-event functional interrupt (SEFI)
- **<u>Destructive malfunction</u>: hard faults**
  - Single-event upset (SEU)
  - Single-event burnout (SEB)
  - Single-event gate rupture (SEGR)
- **Hardening techniques**
  - Dual interlocked storage cell (circuit-level)
  - Error detection and correction (system-level)

R.C. Lacoe et al., IEEE Trans. Nucl. Sci. (2008), P.E. Dodd et al., IEEE Trans. Nucl. Sci. (2004), P.E. Dodd et al., IEEE Trans. Nucl. Sci. (2010)

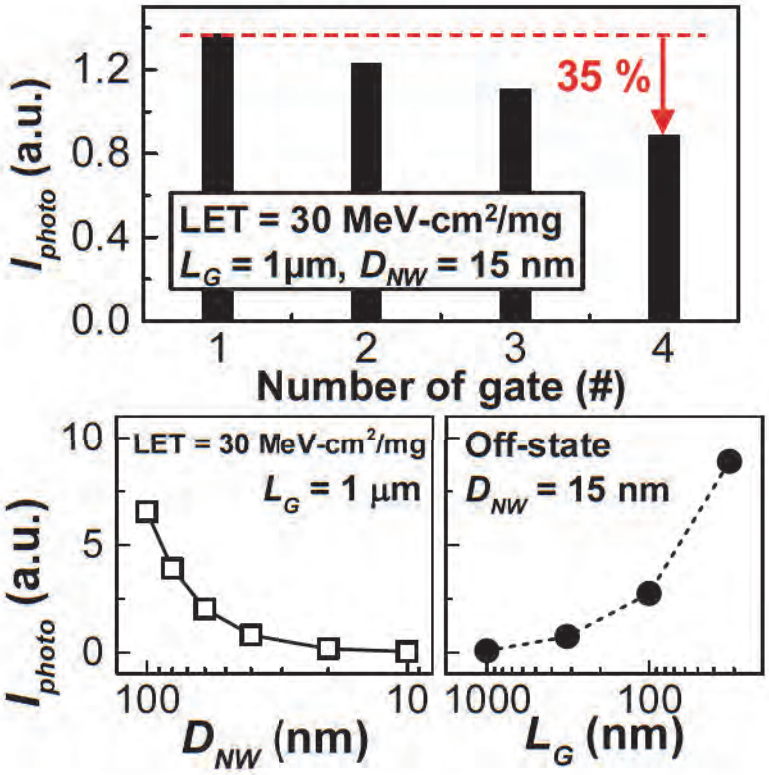
Structural Dependence

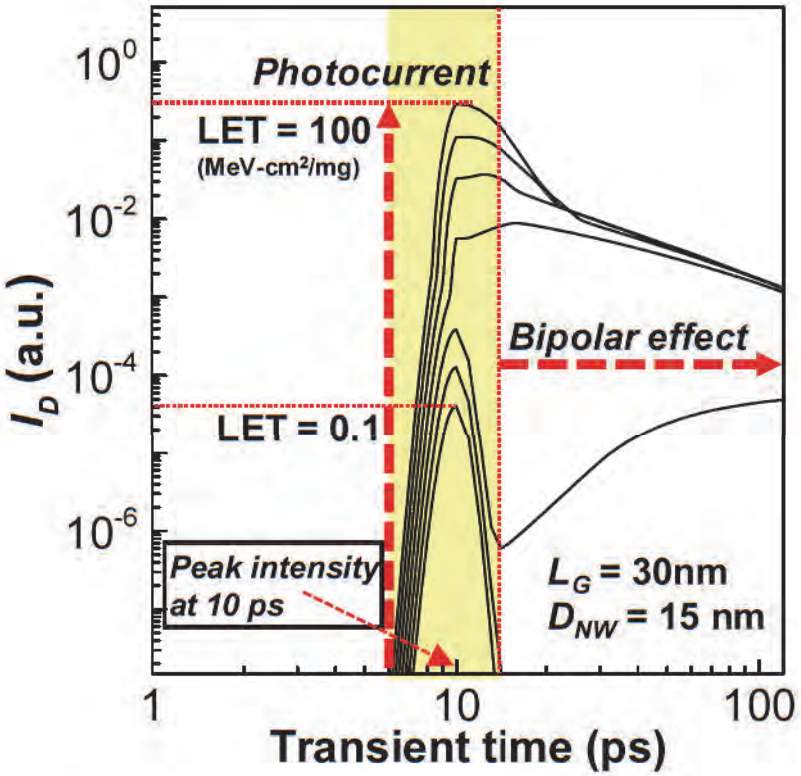


Electron-hole pair generation by radiation

Number of gates ↑ ➔ Leakage current ↓

SEE of SiNW GAA FET



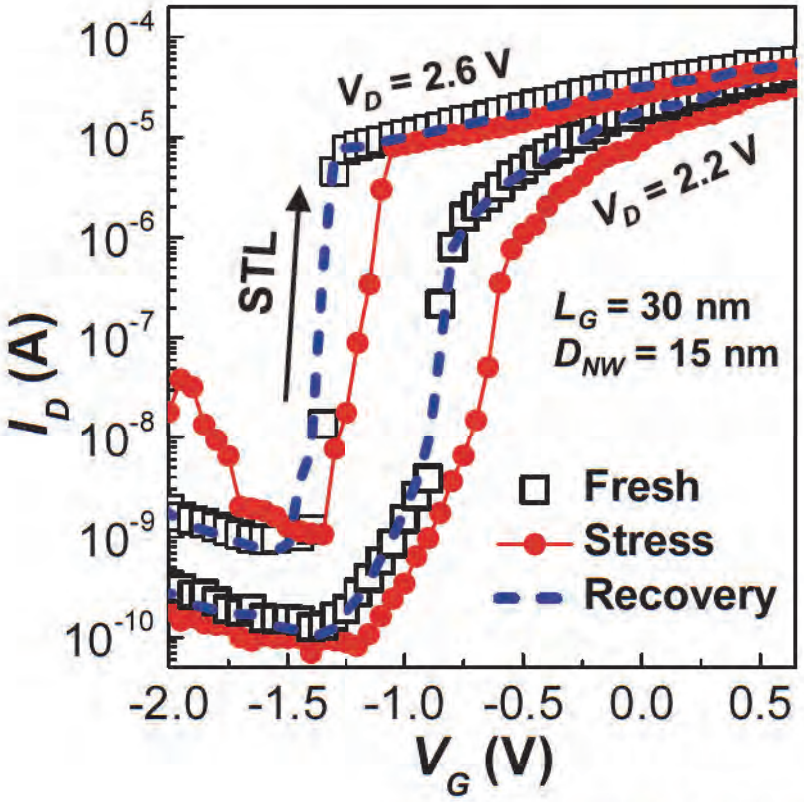


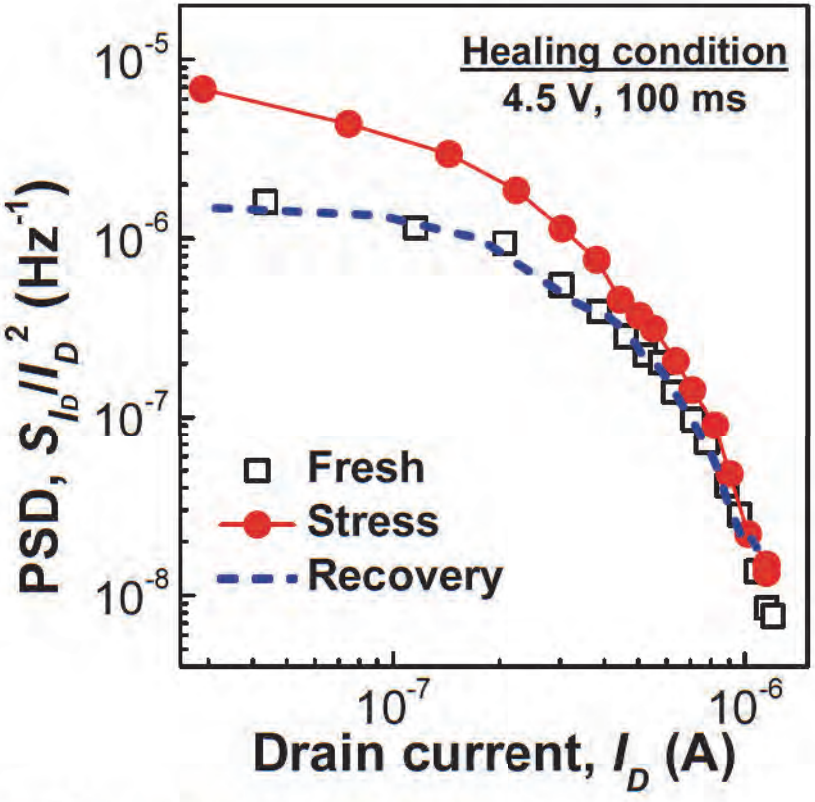
Scaling: D_{NW} ↓ ➔ SEE ↓ vs. L_G ↓ ➔ SEE ↑

Floating body of GAA ➔ bipolar effect

*LET: linear energy transfer

Single Transistor Latch (STL)





Device degradation by latch

Removal of hot carrier stress by Joule heating

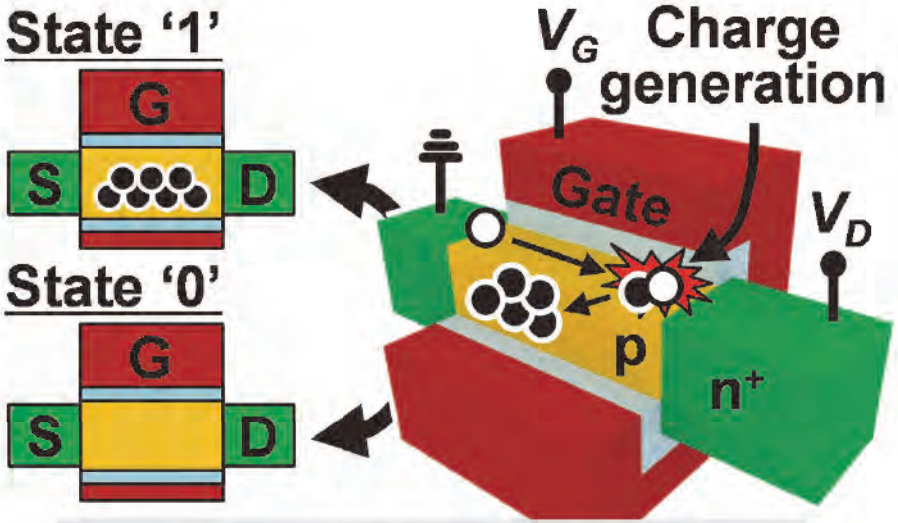
Outline

- Introduction
- Design of Sustainable Electronics
- Pristine Device

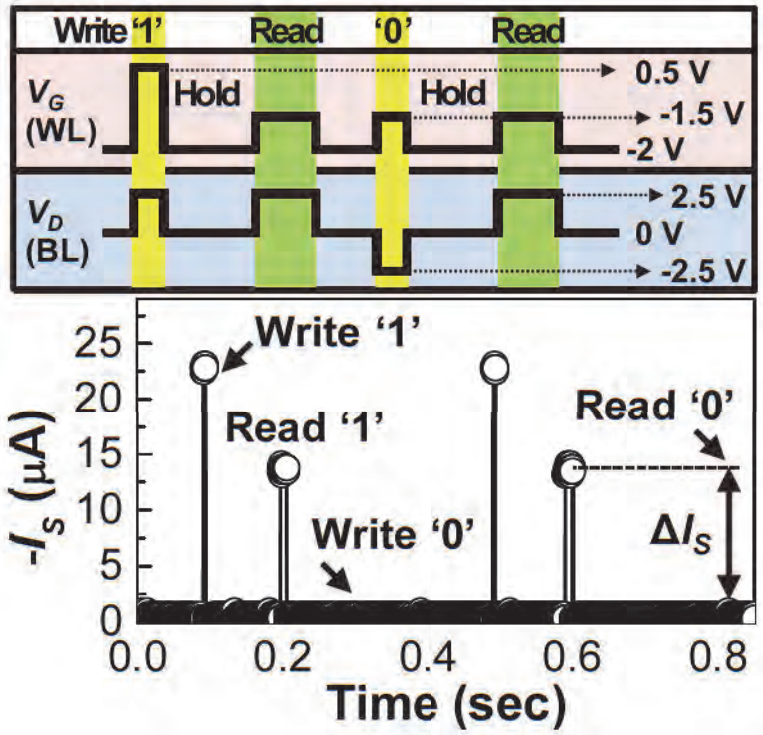
- **Damage and Recovery**
  - Radiation Aspect
  - **Operation Aspect**

- Applications
- Conclusions

Floating Body Cell (FBC)



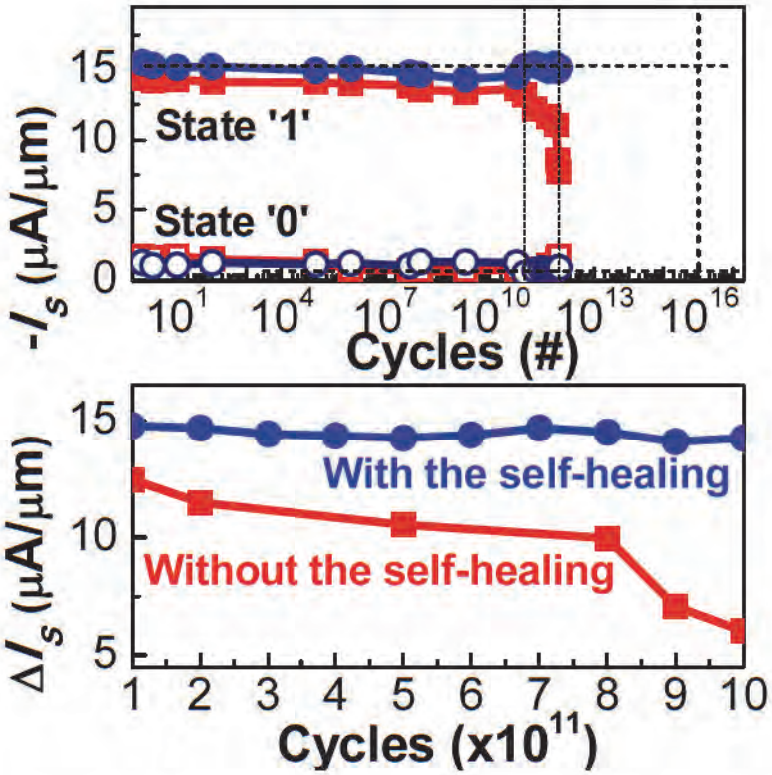
Floating body as a charge storage

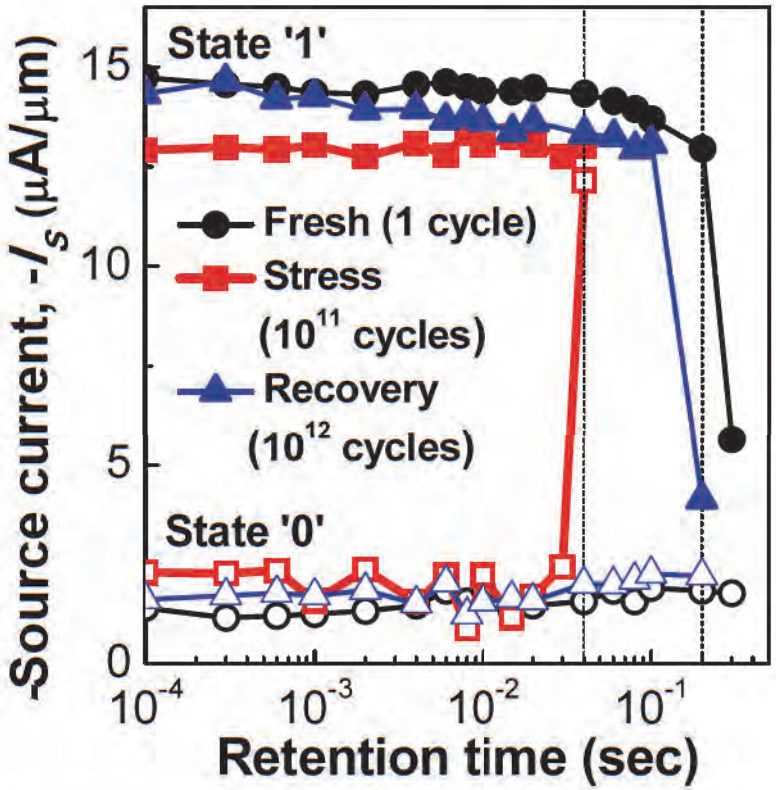


High-speed volatile memory (DRAM)

Reliability issue from the charge generation

Self-Healing in FBC



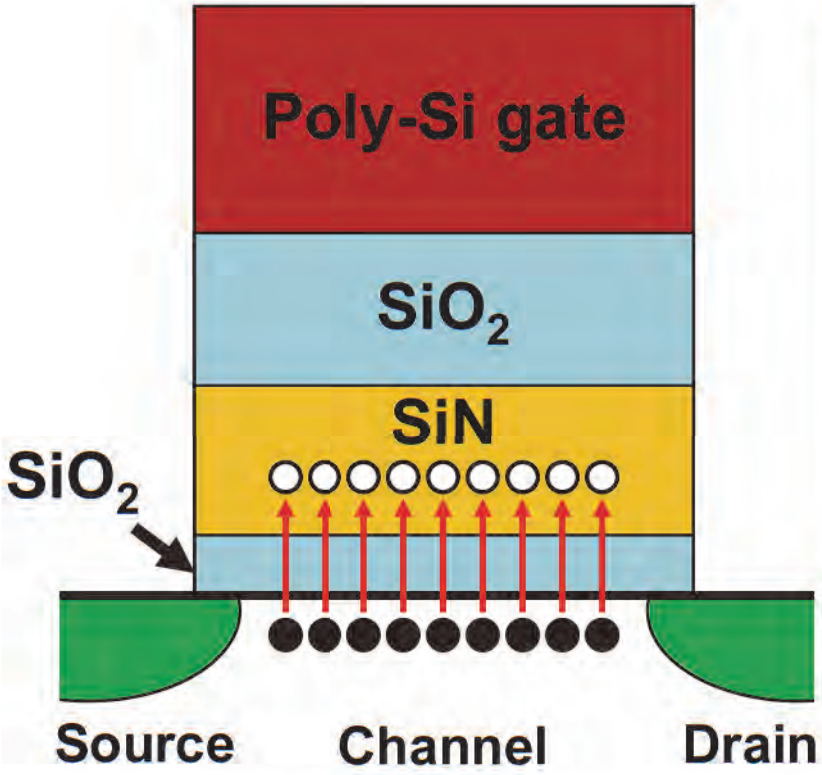


<u>Iterative self-healing process</u>:

10^{11} operations → degradation → annealing

- ✓ **Endurance > 10^{12} cycles & retention > 100 ms**

Flash Memory



Electrons are trapped in SiN through tunneling oxide.

Tunneling oxide can be damaged by program and erase operations.

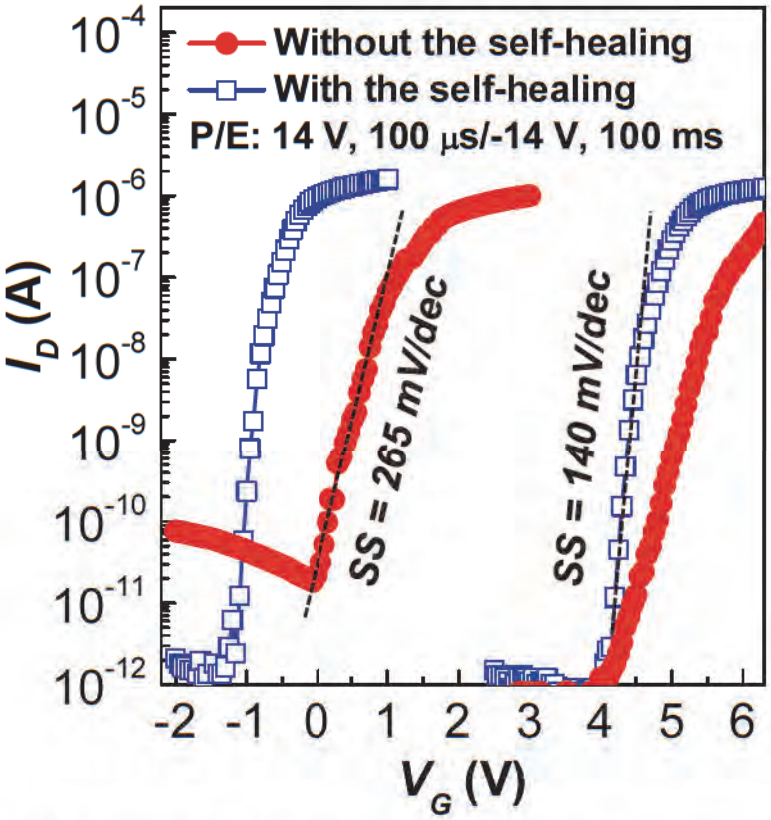
Memory window can be changed and retention can be degraded.

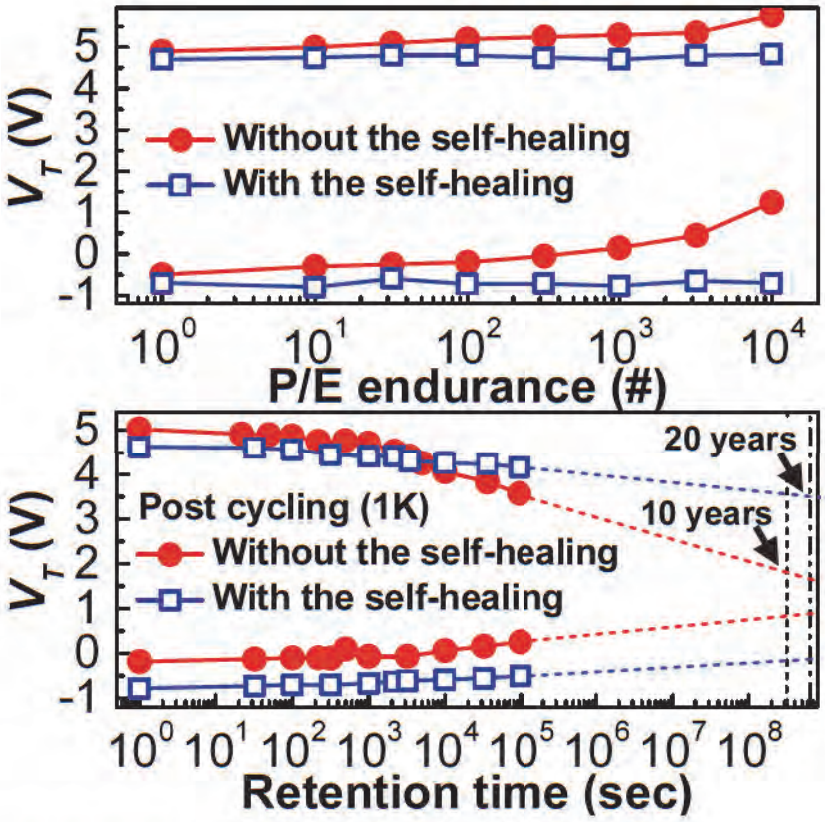
Lifetime of Flash memory can be limited. ➔ Endurance issue

Program/erase stress on a tunneling layer

Increment of trapped charge/interface state

Self-Healing in Flash Memory



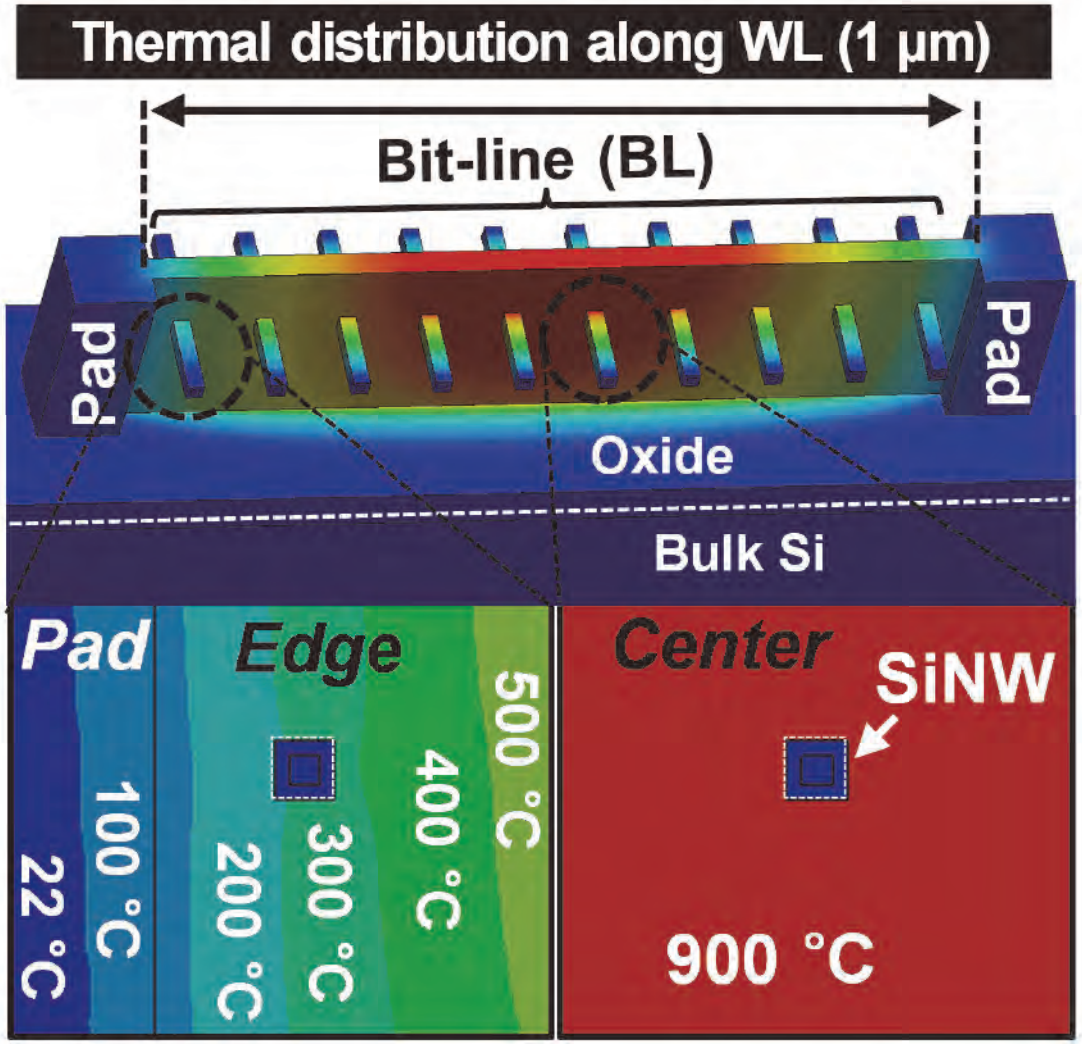


Iterative self-healing process:

1 P/E operation → annealing → no degradation

- ✓ **Endurance > 10^4 cycles & retention > 10 years**

Word-Line Design

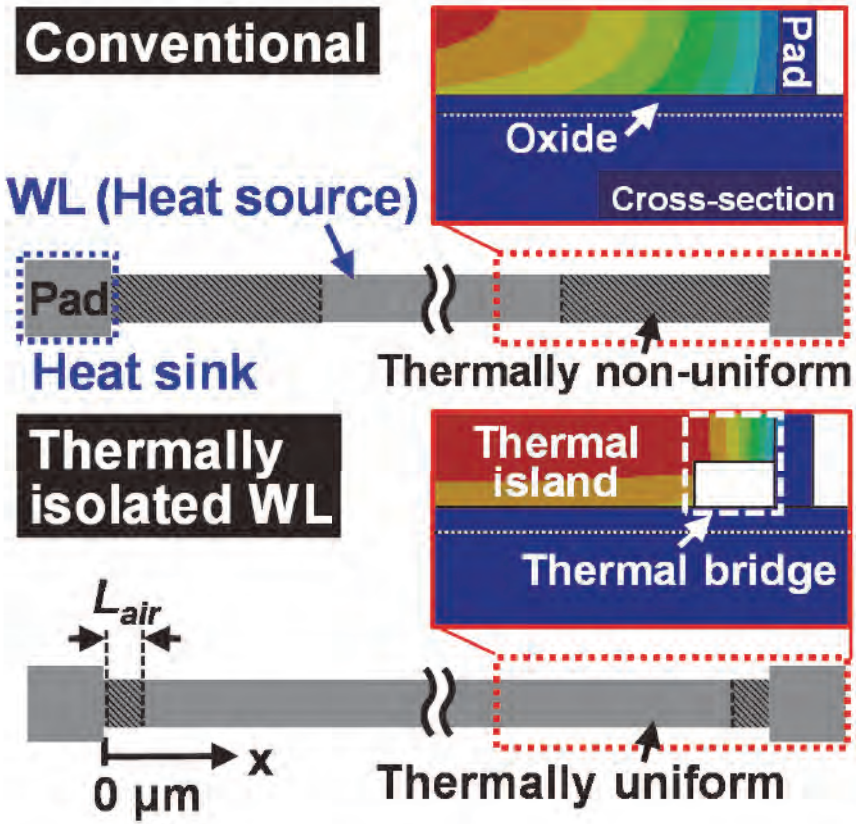


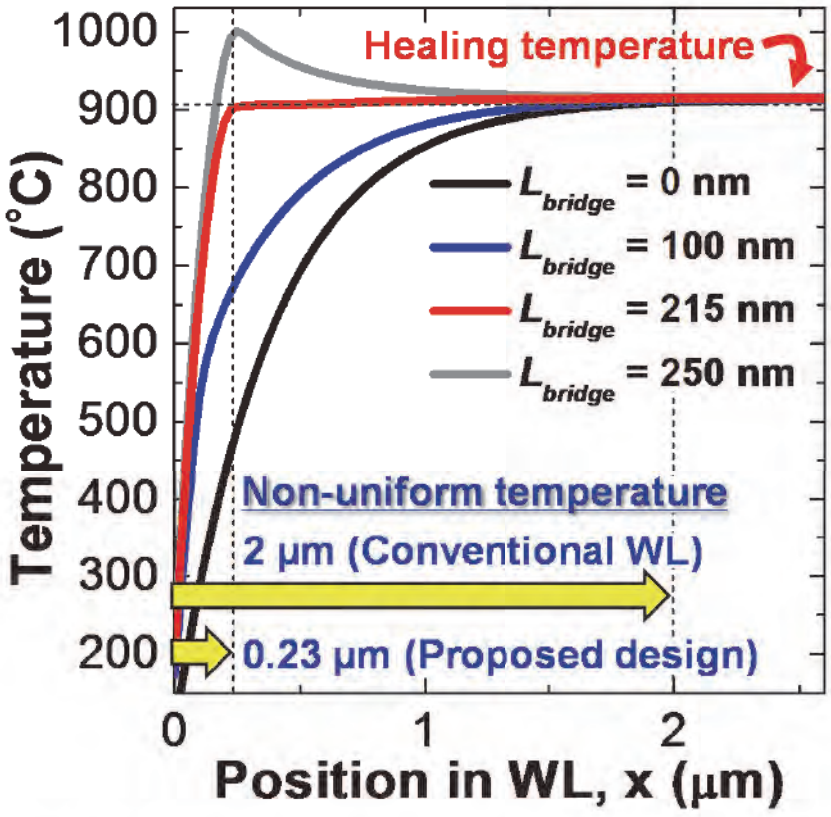
In memory array,
a long word-line (WL) is required for high density.
And many bit-lines are included in one WL.

Thermal distribution
: non-uniform along the WL

- Center temp. : 900 °C
- Edge temp. : 300 °C

Thermally Uniform WL

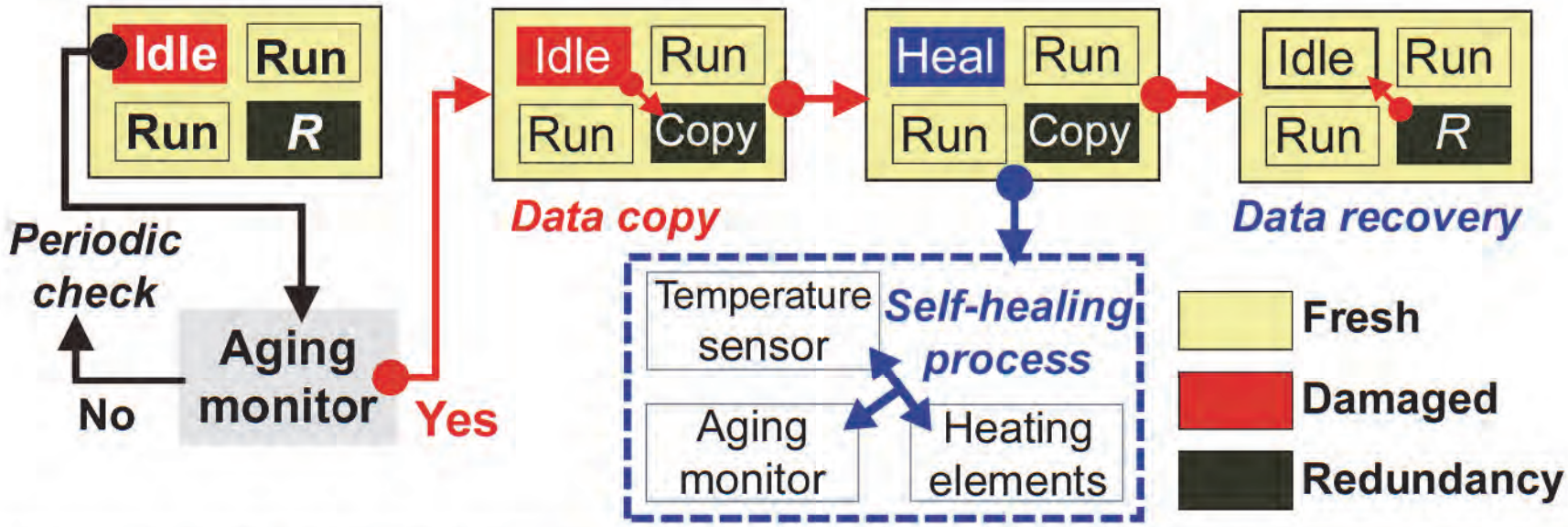




Thermal bridge between heat source and sink

- Heat source (WL) ➔ thermal island
- Uniform temperature regardless of a length of WL

Flow Chart



All parts of logic and memory are not used at the same time!

On-the-fly thermal annealing

Idle state → aging check → recovery process

Data loss during the healing: copy to redundancy

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High Reliability Applications

Space

Image: Texas Instruments

Military

Image: Texas Instruments

Transportation

Image: Texas Instruments

Automobile

Image: Tesla

Medical equipment

Image: Intuitive Surgical Systems

Server and network

Image: Google

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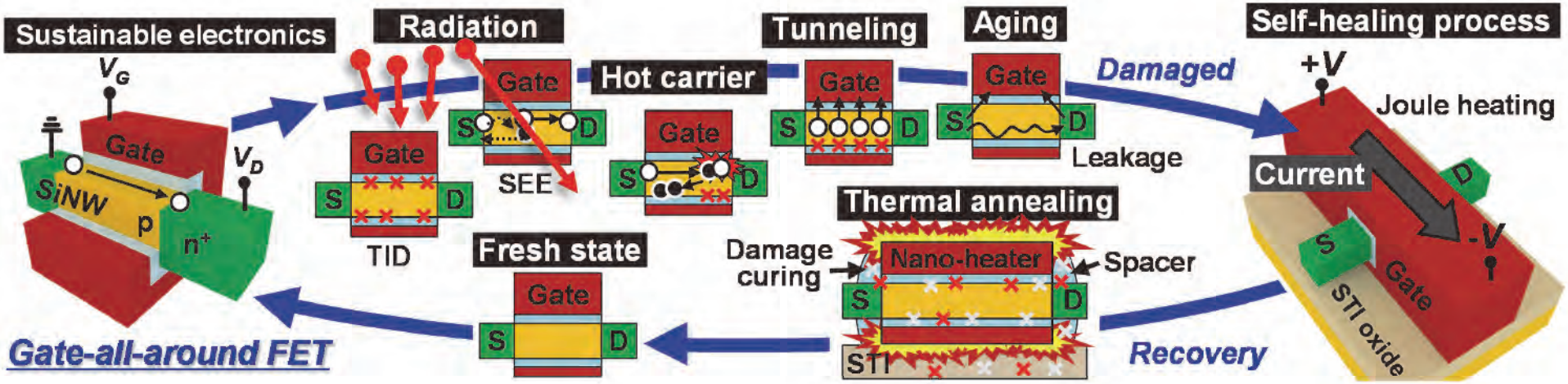
Conclusions



- The temperature arising from Joule heat by the gate was applied for the on-the-fly self-healing process.
- The lifetime of devices can be extended, which opens an opportunity for nano-spacecraft to sustain more than 20 years of deep space exploration.

Acknowledgment

- Prof. Yang-Kyu Choi's group
  School of EE, KAIST
- Prof. Hee Chul Lee's group
  School of EE, KAIST
- National NanoFab Center, Korea

By far, R&D activities across in industry, academia, and government have focused on "***How to improve endurance against the radiation***."

But, this project is
"***How to recover and self-heal to healthy condition***"
as human immune systems.

Thank you for your attention.