ims chips

Ultra-Thin Si Chips

A New Paradigm in Silicon Technology

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IEEE EDL Distinguished Lecture 2015

INSTITUT FÜR MIKROELEKTRONIK STUTTGART

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Overview of IMS CHIPS

- Independent, non-for-profit foundation in Baden-Württemberg, Germany
- Located at campus of the University of Stuttgart
- >100 staff members + guest researchers
- 26.2 M€/a total budget (2014)
- 1200 m^2 Class-10 clean room
- ISO 9001 certification (since 1992)
- Certified low/mid-volume manufacturing
- 4 business units
  - Integrated Circuits&Systems
  - Semiconductor Integration Techn.
  - MEMS Technologies
  - Nanostructuring
  - Imaging Sensors
- Close cooperation with the University of Stuttgart
- A member of the Innovation Alliance Baden-Württemberg

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Outline

- **Introduction to ultra-thin chip applications**
- **Ultra-thin chip fabrication**
  - Dicing-before-Grinding (DBG) technology
  - ChipFilm™ technology
- **Characteristics of ultra-thin chips**
  - Warpage of thin chips
  - Mechanical stability of ultra-thin chips
  - Piezoresistive effect
- **Ultra-thin chip assembly and embedding**
  - 3D chip stacking
  - Embedding in foil substrates
- **The KOSIF project – a technology platform**
- **Conclusions**

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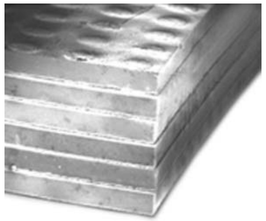
Generic Thin-Chip Applications

3D chip stacking



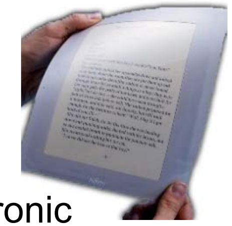
3D IC

Smart Dust

Stacked Microsystems

Mechanical flexibility

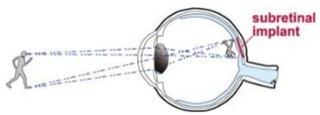
Document Security



Electronic Paper

RF ID

Mini Endoscope

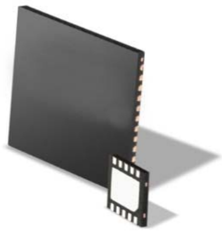


Retinal Implant

Video Pill

Chip shape and adaptivity

Chip Card

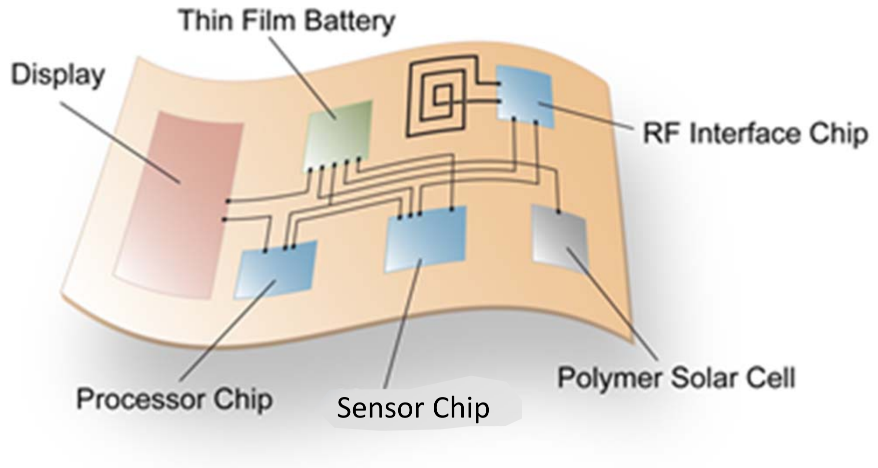


Ultra-thin and Power

Smart Tags

Ultra-thin chips

Hybrid Systems-in-Foil



Thin Film Electronics ⟷ **Si Integration**

- **Pro**: devices widely spaced
- **Con**: low performance
- **Con**: low integration density
- **Pro**: mechanical flexibility

\+

- **Con**: devices on chip
- **Pro**: high performance
- **Pro**: high integration
- ~~**Con**: thick Si chips~~

↓

- **Pro**: thin, flexible chips !

→ Hybrid systems-in-foil = combining technologies with complementary merits!

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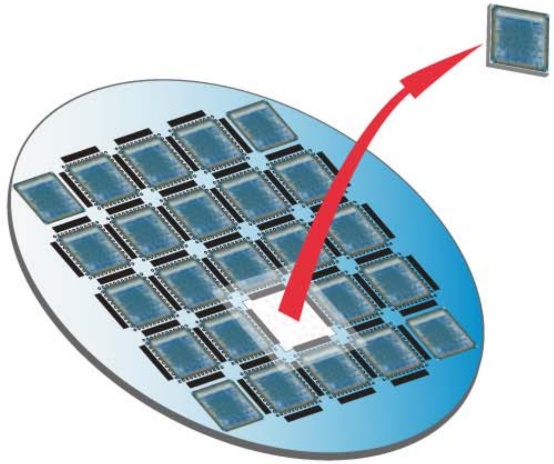
Process Technologies for Ultra-Thin Chips

ChipFilm™

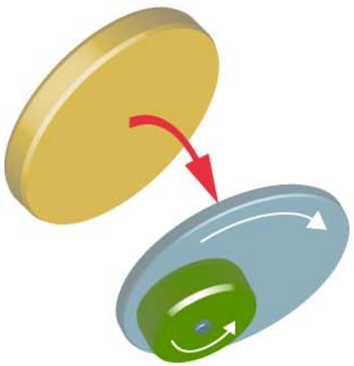


Additive process

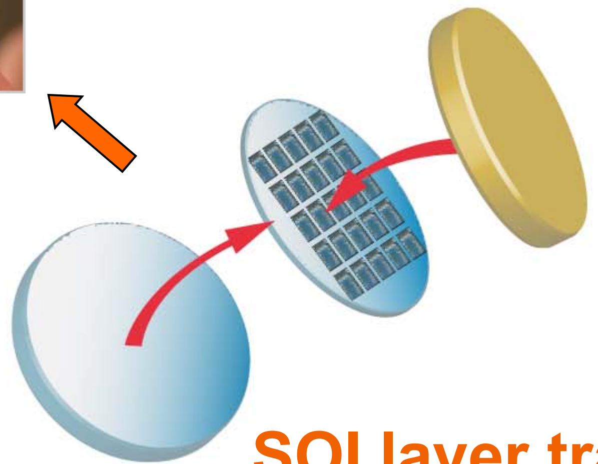
Subtractive processes

Die-level thinning

Wafer-level thinning



Wafer back thinning



SOI layer transfer

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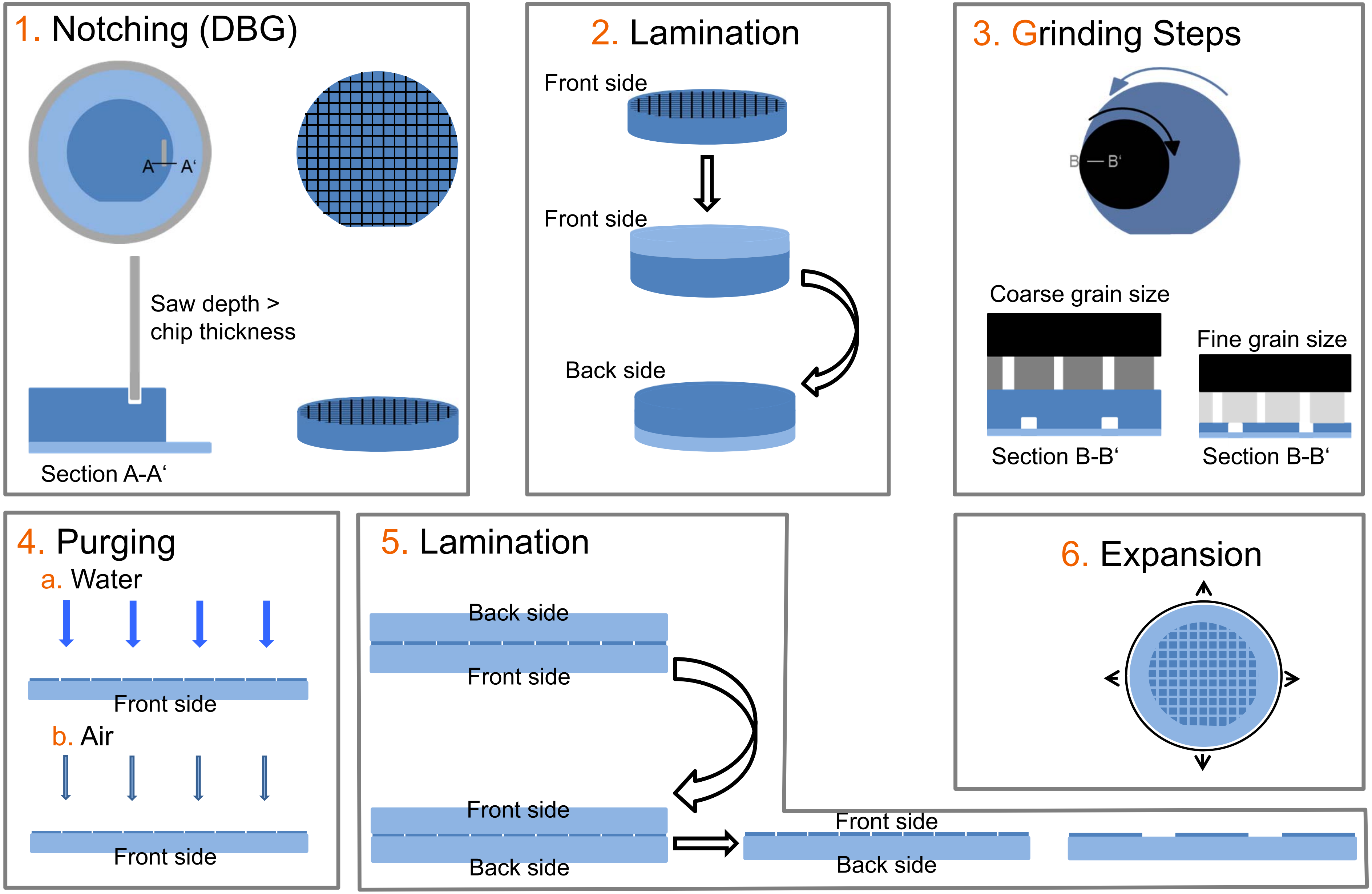
Wafer Back-Grinding (I)



Wafer Back-Grinding (II)

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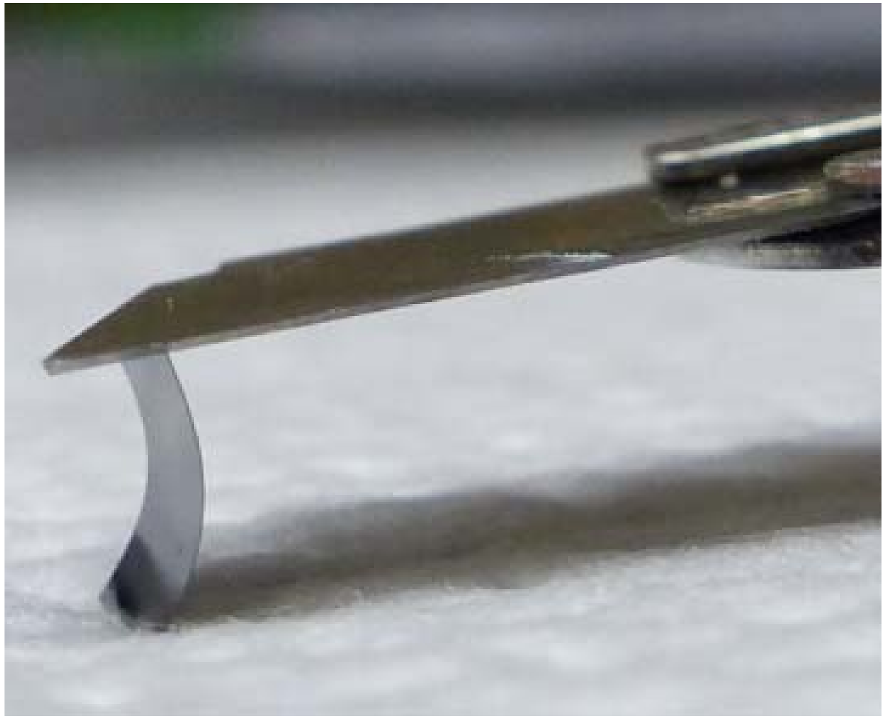
- **20-µm thin experimental chips demonstrated**

Thinned wafer at expansion step



Thinned chip under bending force

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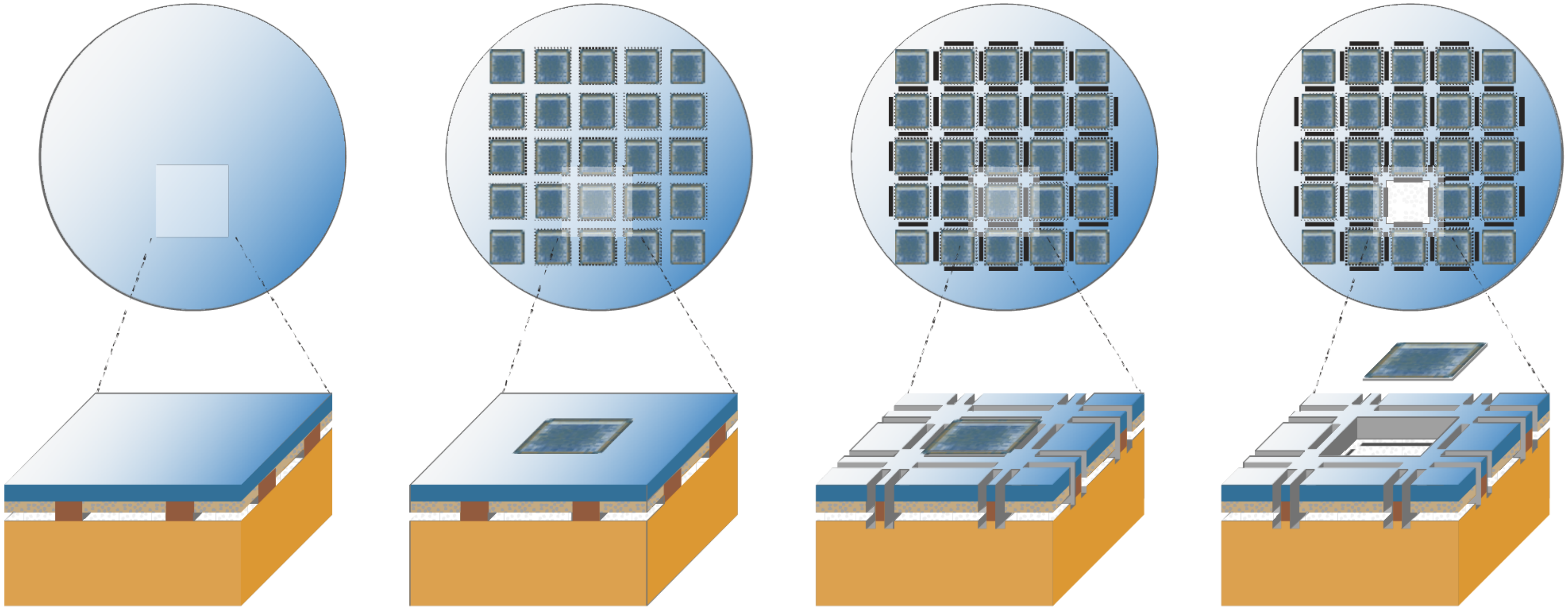
ChipFilm™ Technology

ChipFilm™ Wafer	CMOS Process	Trench & Test	Pick, Crack & Place™
Buried cavities	Device integration	Anchor structures • lateral (ChipFilm™-I) • vertical (ChipFilm™-II)	Chip singulation



IEDM 2006 Late News: Introduction of ChipFilm™-I

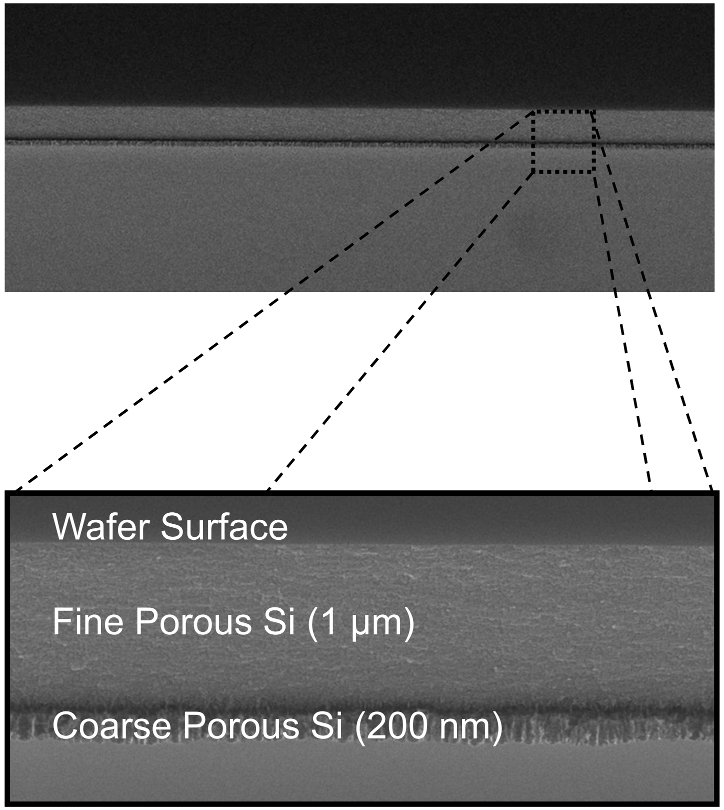
IEDM 2010: Introduction of ChipFilm™-II

Since July 2008: Joint development with Robert Bosch GmbH

The ChipFilm^{TM} Pre-Process

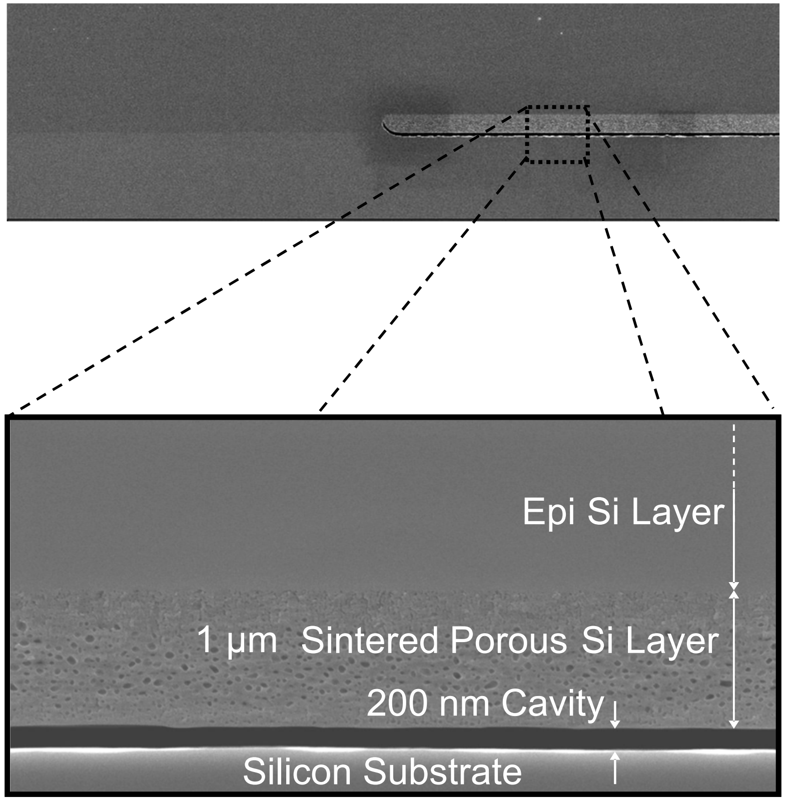
Step1:

- **Anodic etching of a Si wafer**
  - Dual porous Si formation
  - Masking through n^{+} doping

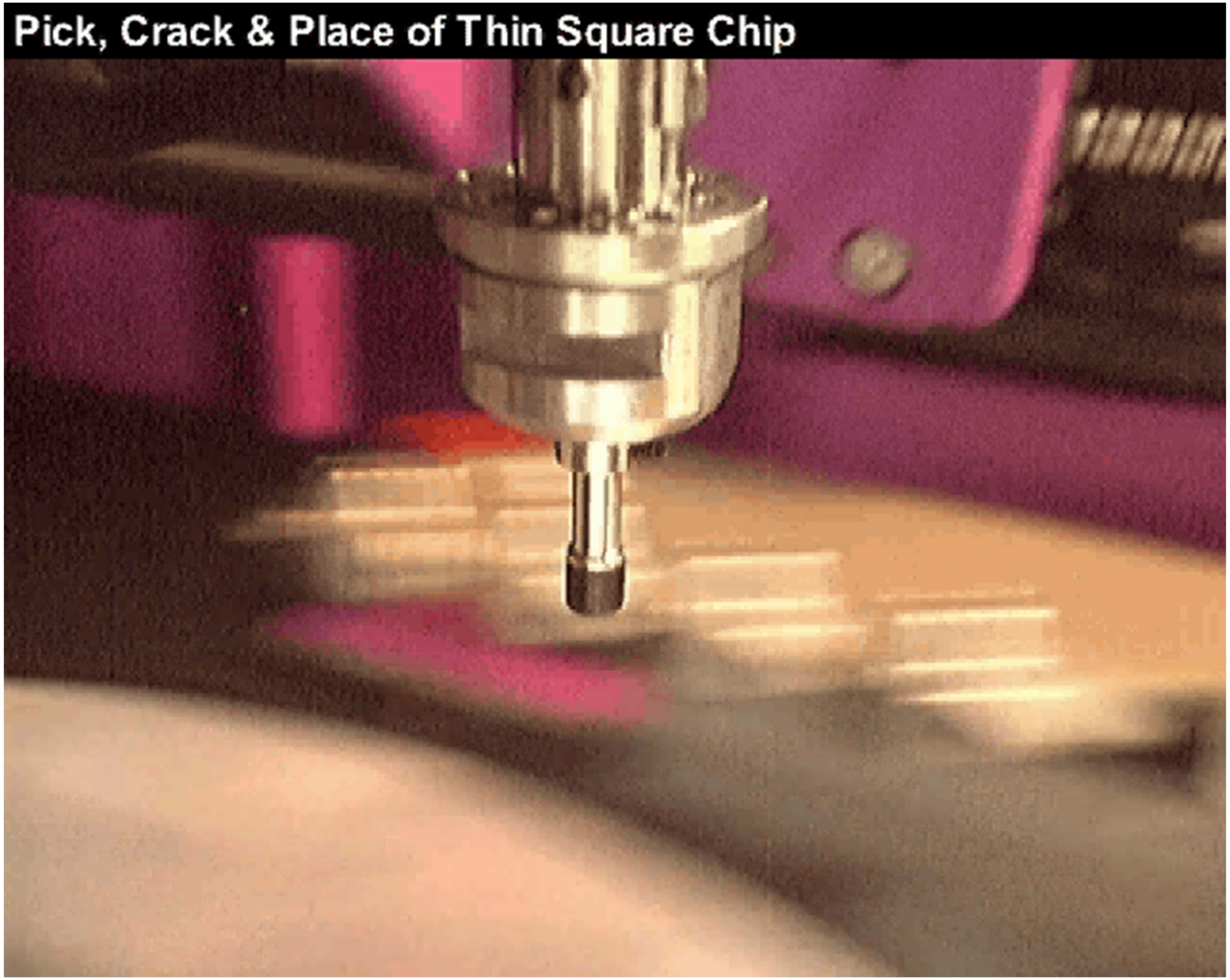


Step2:

- **Sintering in oxygen-free ambient**
  - Silicon reflow
  - Fine porous Si → Nano grains
  - Coarse porous Si → Buried cavity



The Pick, Crack & Place™ Post-Process



Technology Comparison

- **ChipFilm™-I ®** *IEDM 2006*
  - Continuous cavity
  - Lateral anchors

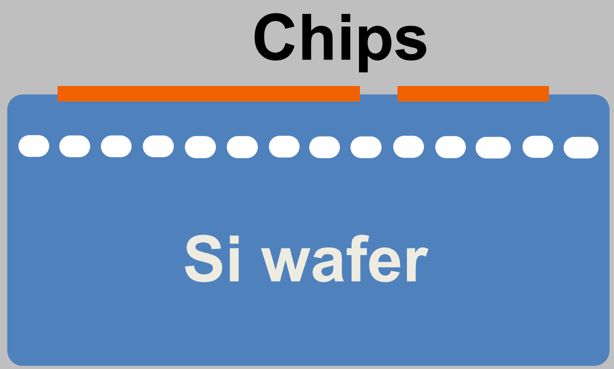
Pros:

+ Thickness limit < 20 µm

Cons:

- Surface steps (~ 200 nm)
- Predefined chip size

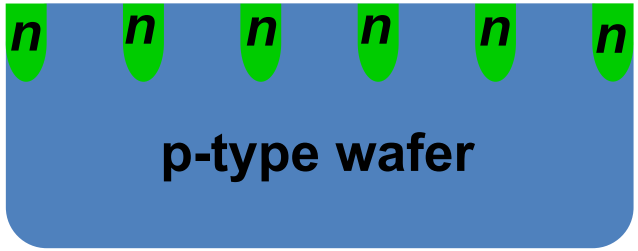
- **ChipFilm™-II ®** *IEDM 2010*
  - Discontinuous cavity
  - Vertical anchors



Pros:

+ Thickness limit < 20 µm
+ High planarity (r_{avg}~ 7 nm)
+ Generic wafer substrate

ChipFilm™-II Process Flow



- **Pre-process module (I)**
  - **n-implant**
  - **anodic etching**
  - **thermal annealing**
  - **epitaxial growth**

- **Device Integration**

- **Post-process module**
  - **Trench etching**
  - **Chip detachment**

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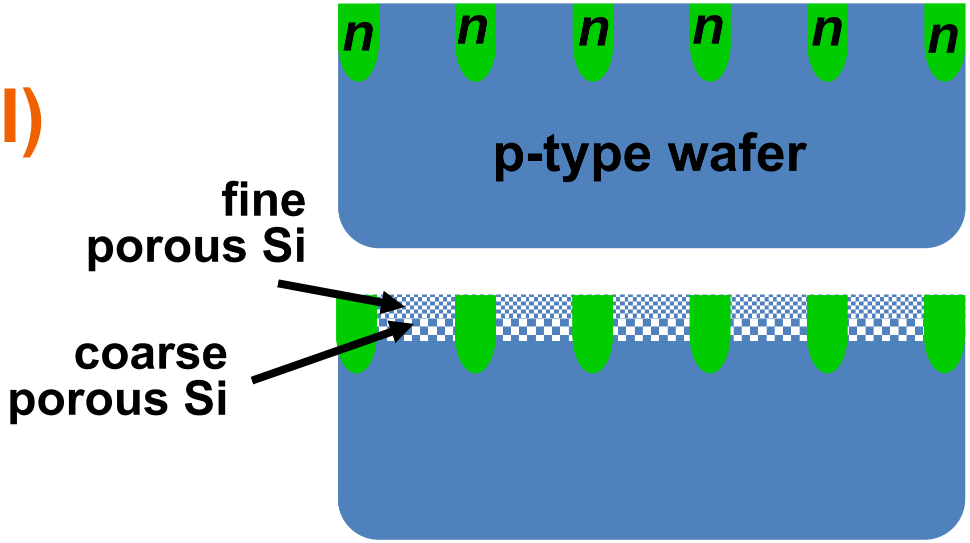

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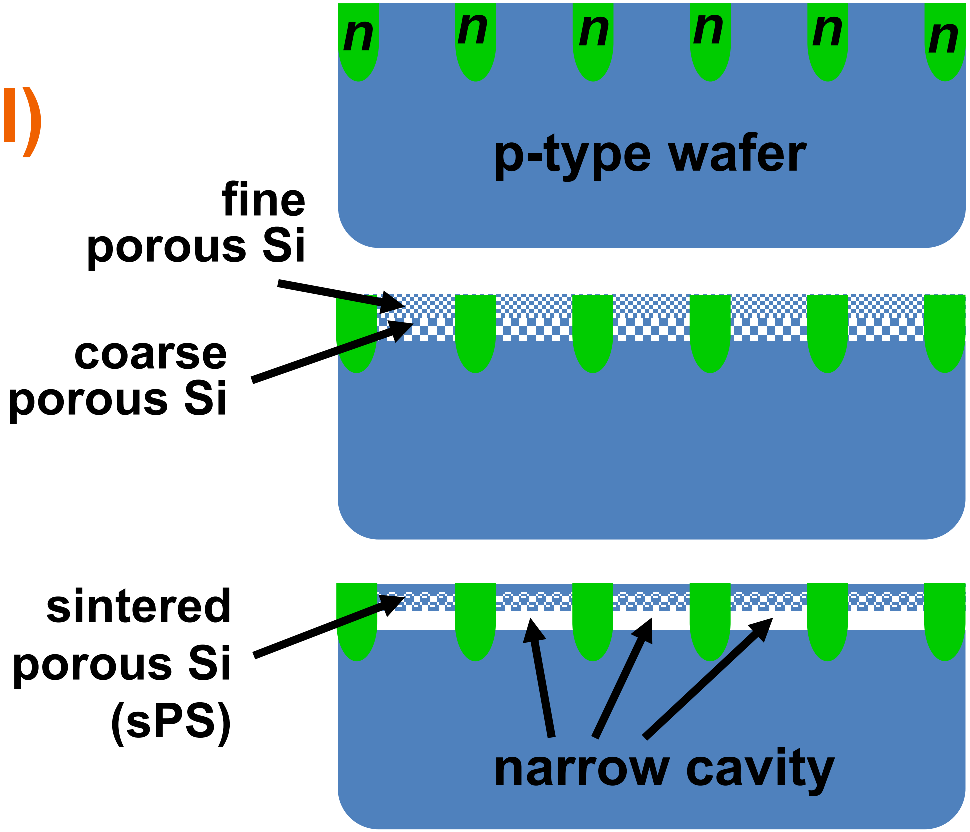

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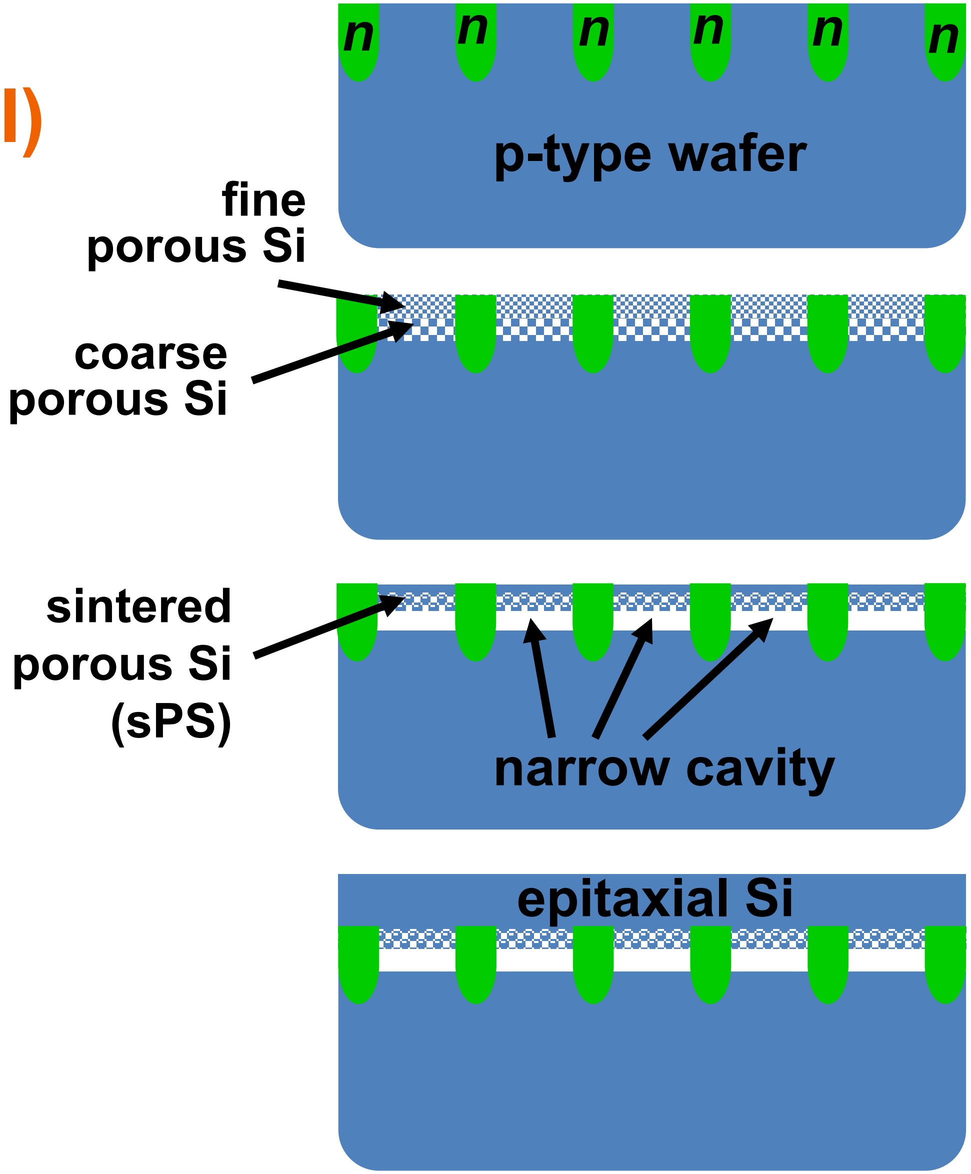

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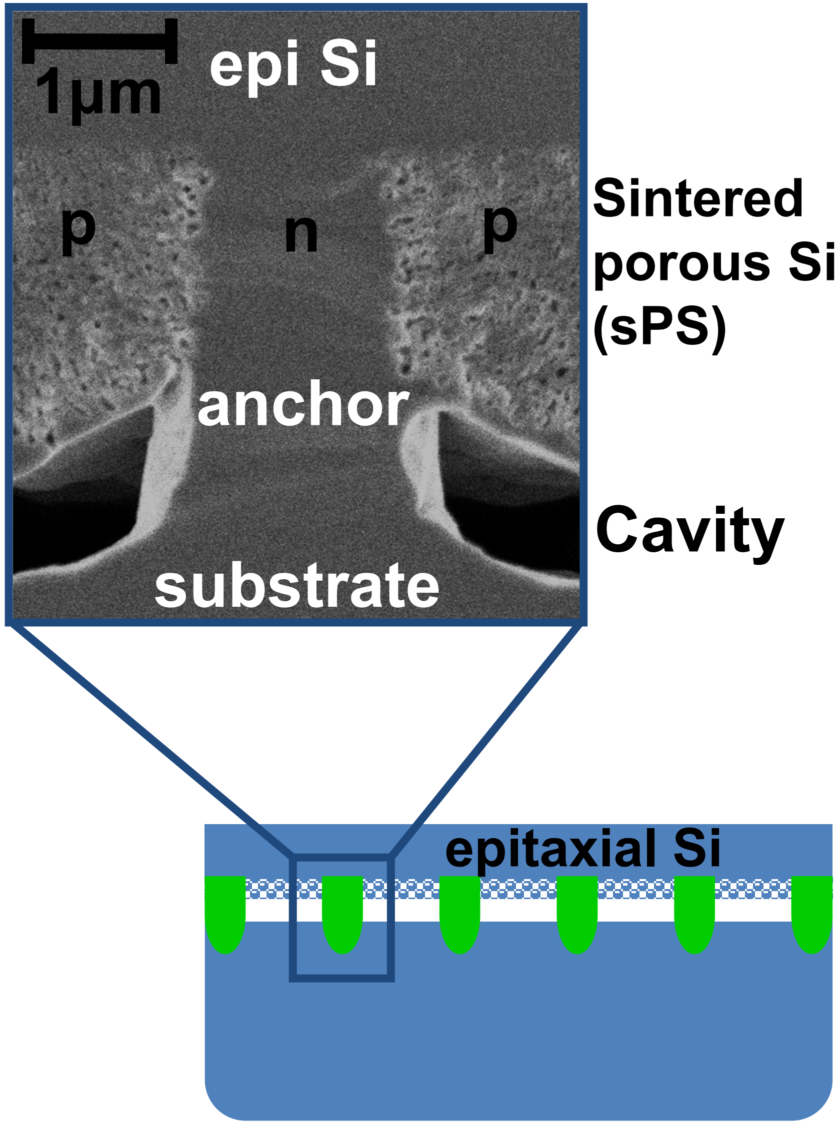

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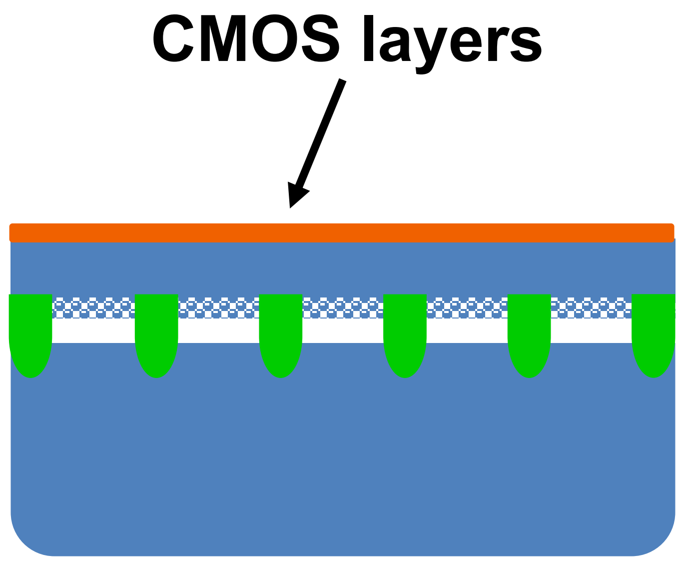

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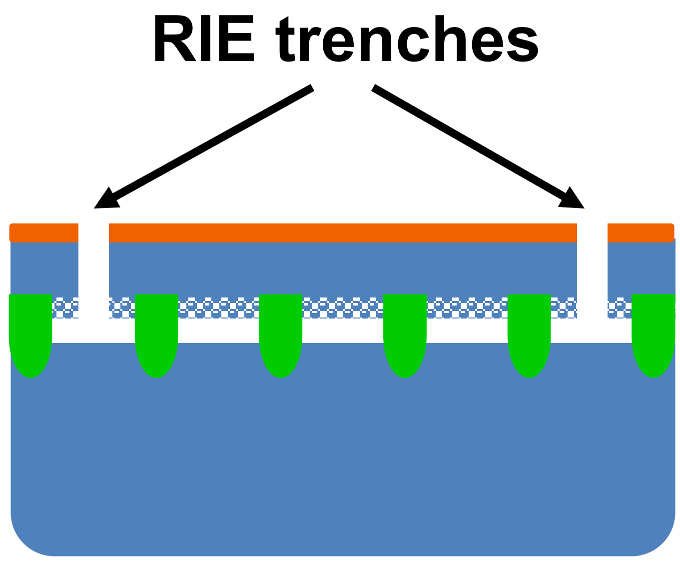

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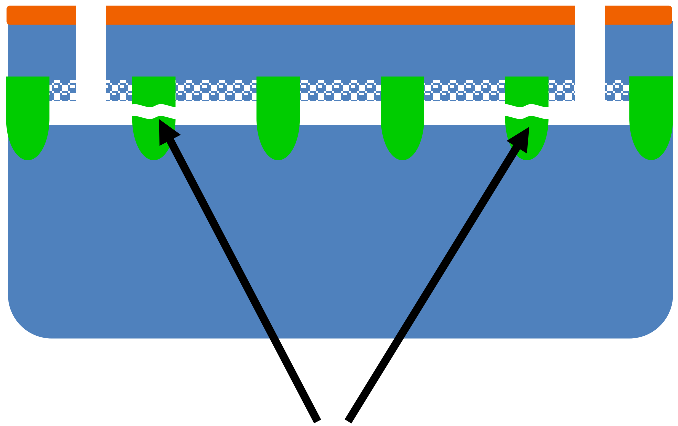

fracture of specific anchors (weak attachment)

ChipFilm™-II Process Flow

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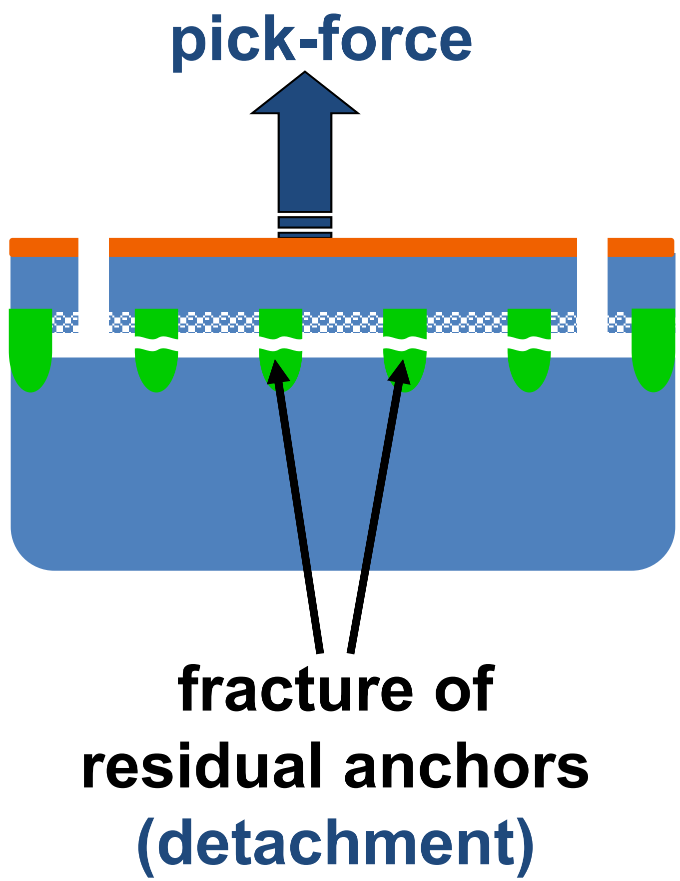

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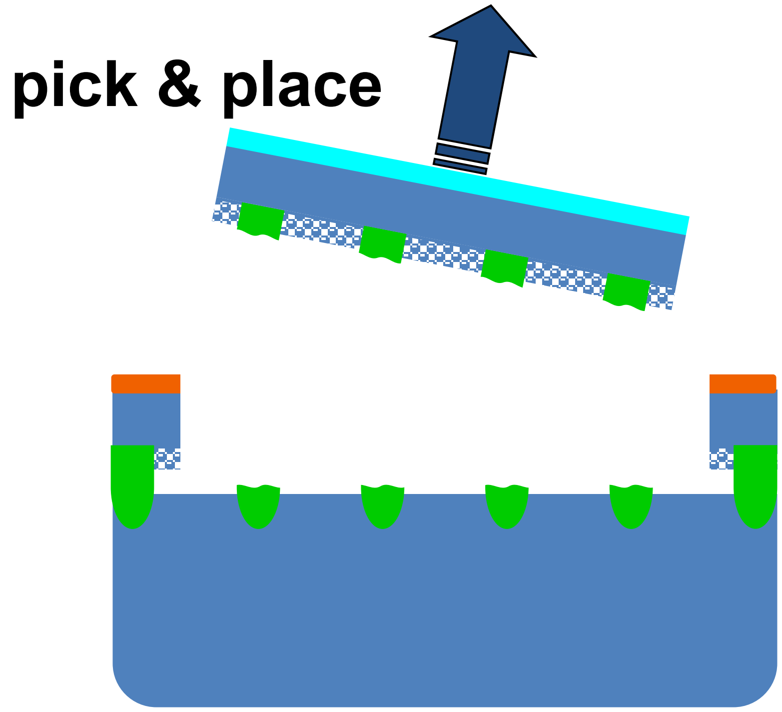

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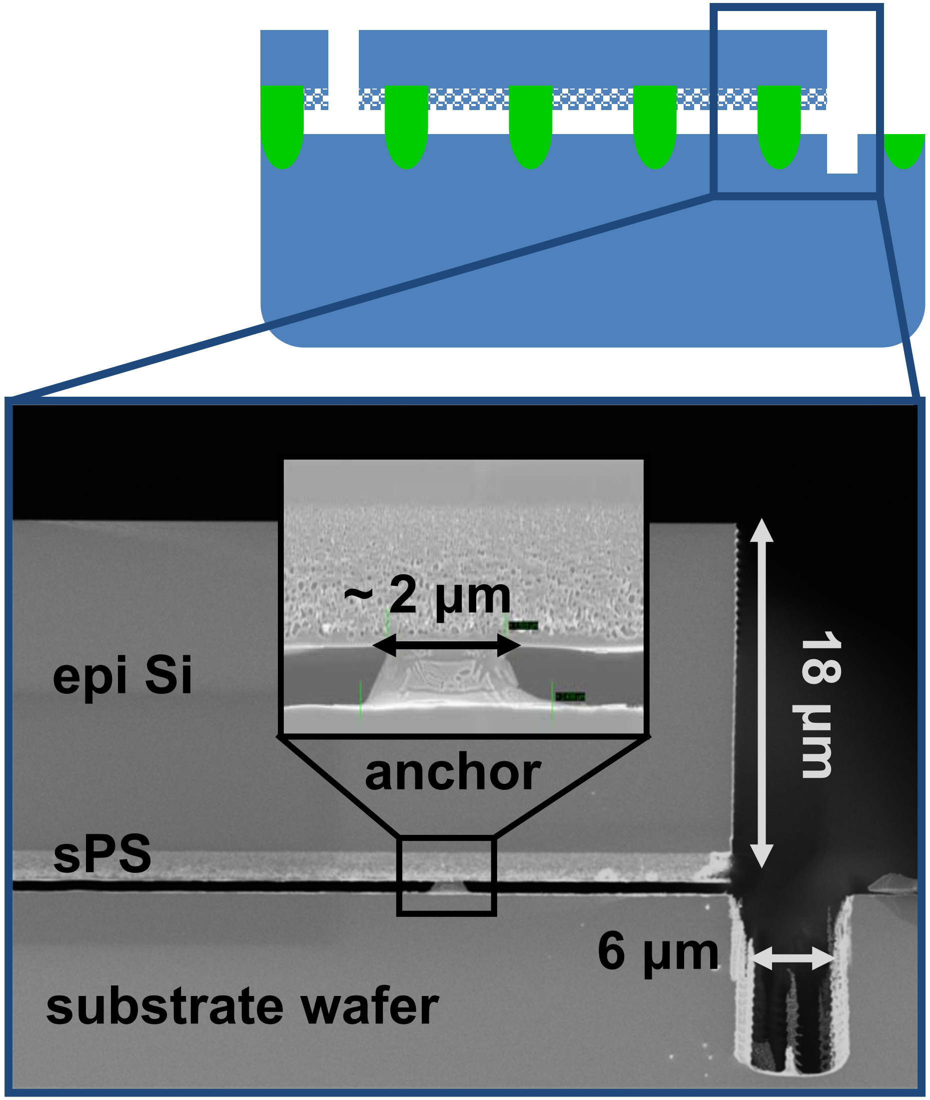
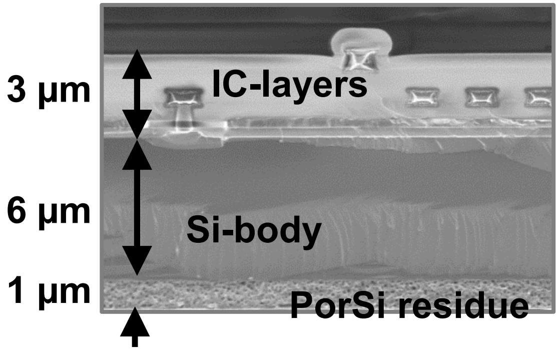
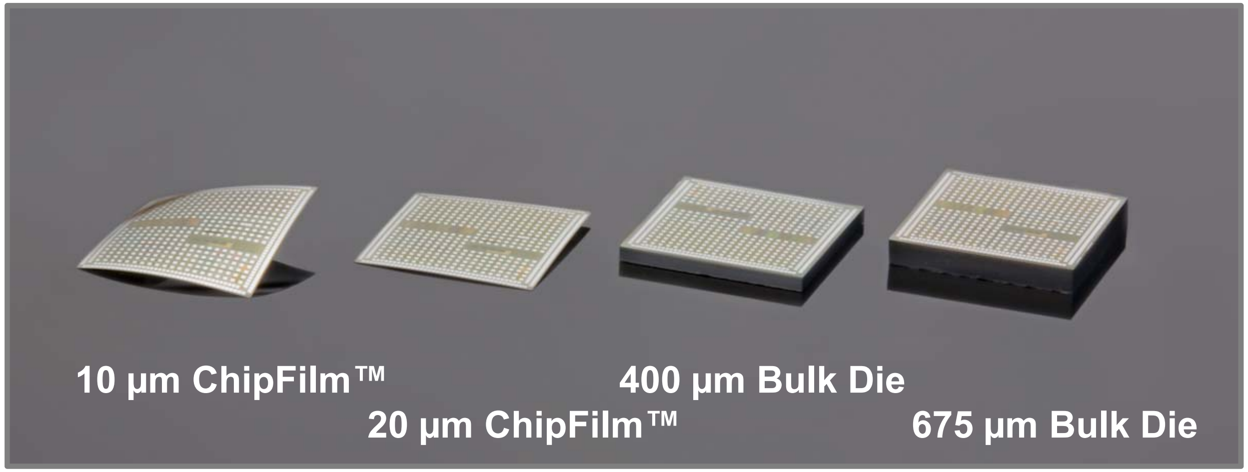
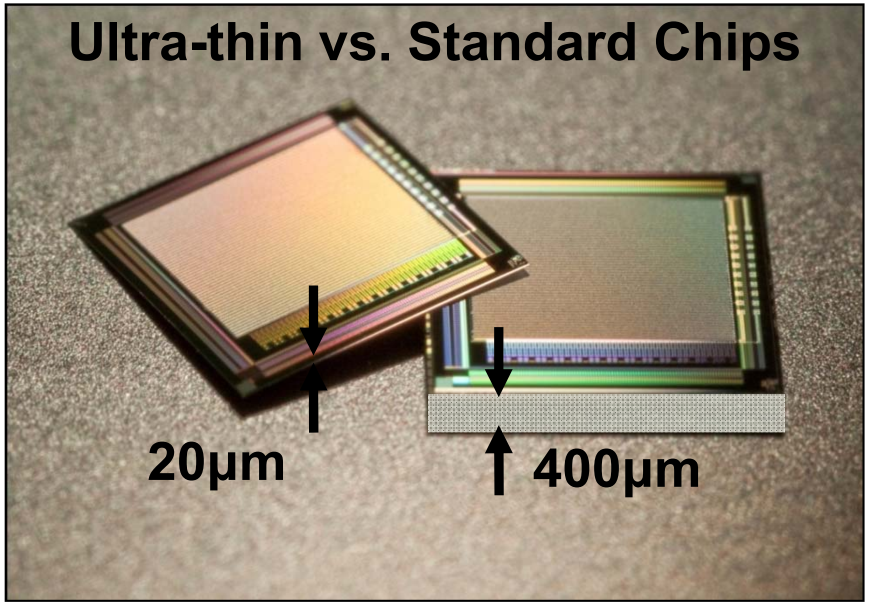


Ultra-Thin vs. Conventional Chips



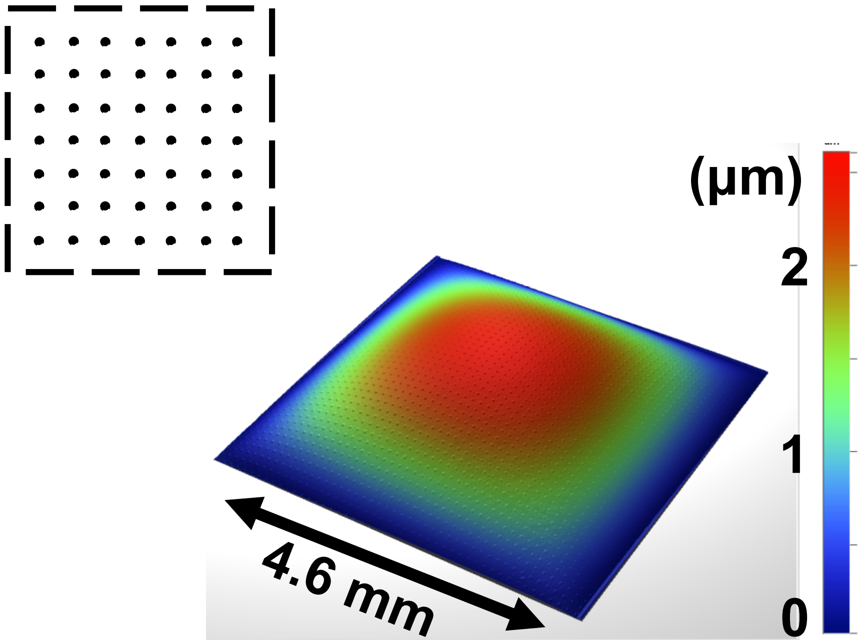




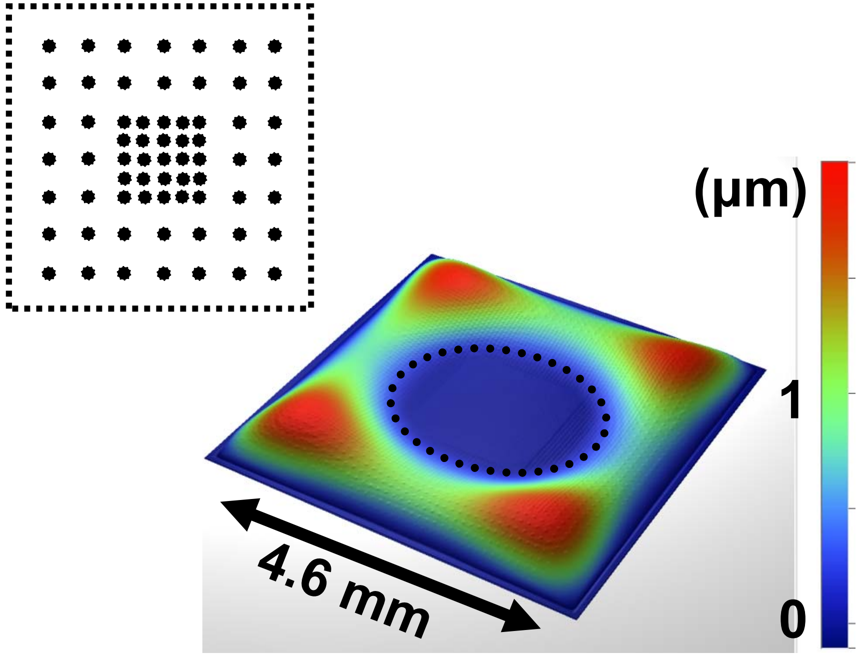
- **0.8/0.5 µm CMOS bulk wafers**
  - 675 µm initial thickness
  - 400 µm after back-grinding
- **0.8/0.5 µm ChipFilm™ IC dies**
  - 20 µm and 10 µm

Process Window (I)

- **Uniform anchor array**
  - After externally induced stress:
    - Outer ring of anchors remains
  - For generic wafer use

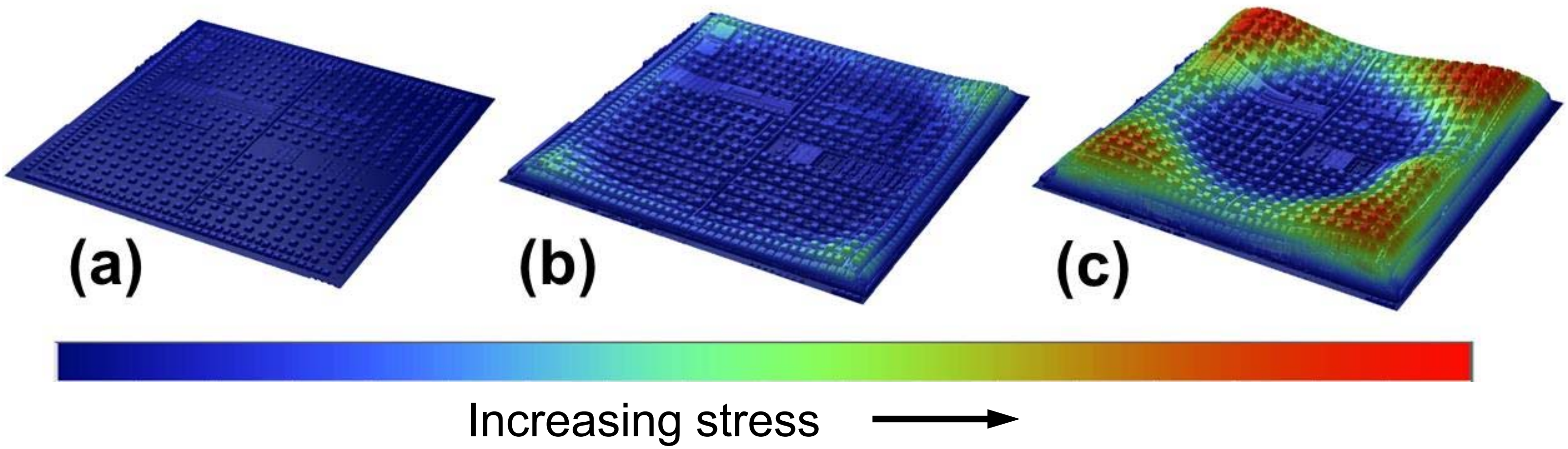


- **Non-uniform anchor array**
  - After externally induced stress:
    - Outer ring of anchors remains
    - Inner group of anchors remains
  - Pre-defined chip locations



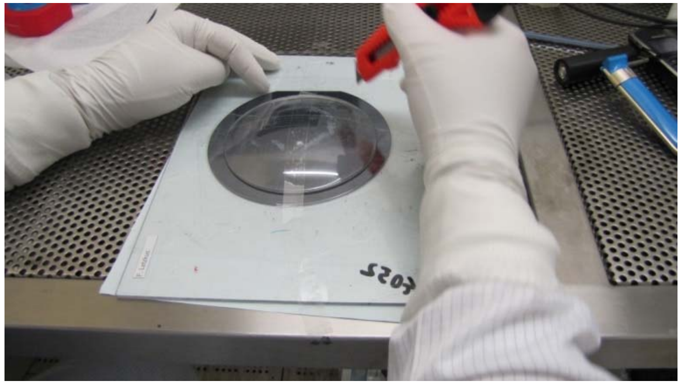
Controlled chip detachment procedure:

- a) **Before trenching:** all anchors are intact!
- b) **After trenching:** some anchors are broken due to process-induced stress!
- c) **After externally applied stress:** well-defined groups of anchors are broken!
- d) **During PC&P:** all anchors are broken and chips are detached**!**

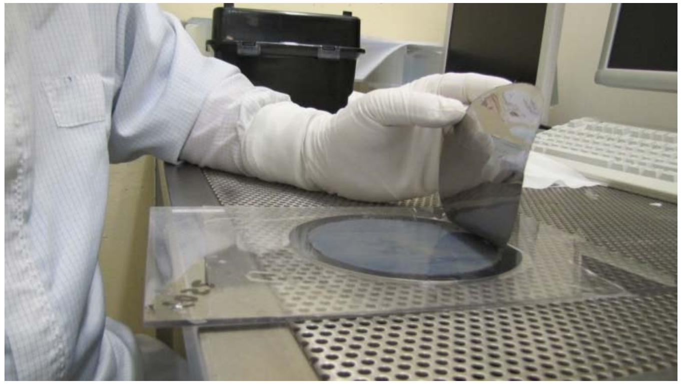


Attach foil carrier

Define scratch area



Manual release of ultra-thin film



Deep scratching

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Thin-Chip Warpage (I)

- **Silicon-chips**

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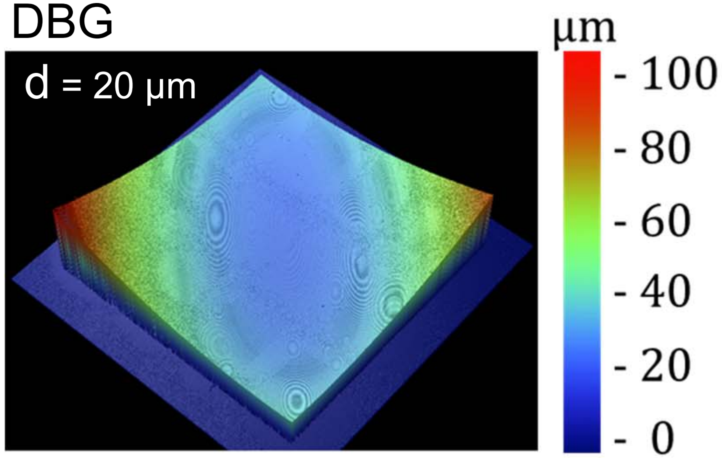
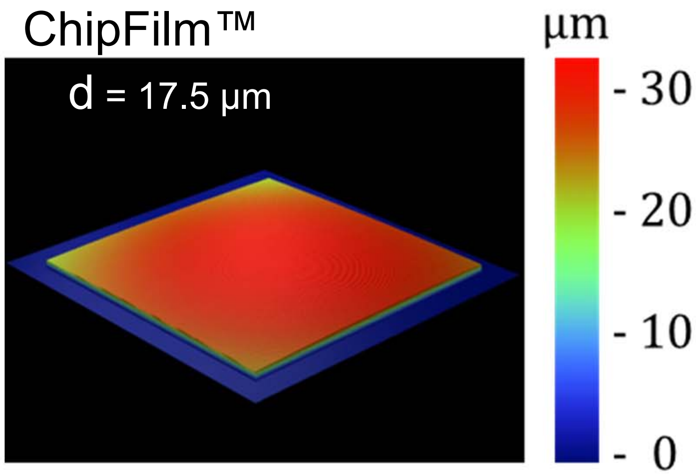
DBG



ChipFilm™

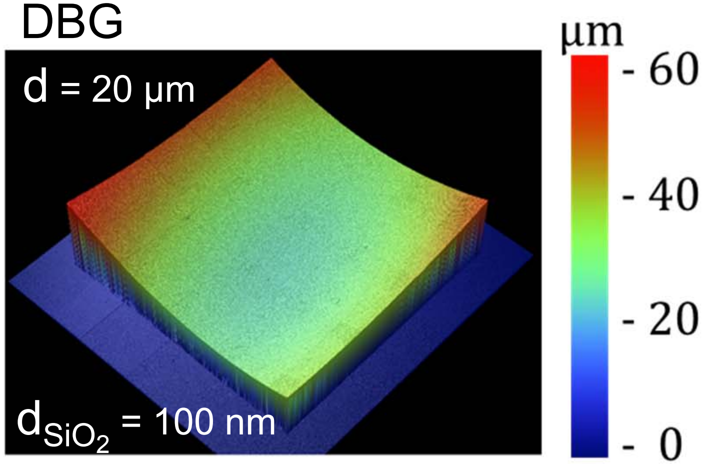


$E_{w,DBG} \approx 80$ µm

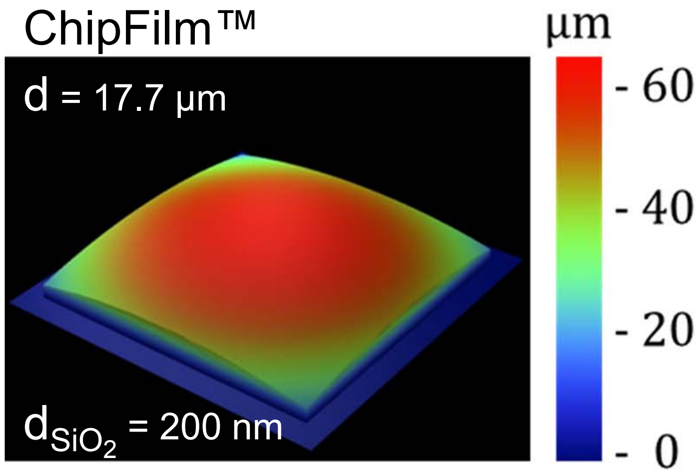
$E_{w,ChipFilm} \approx 9$ µm

- **Silicon-chips with a thin SiO_2 layer**

DBG



ChipFilm™



$E_{w,DBG} \approx 40$ µm

$E_{w,ChipFilm} \approx 40$ µm

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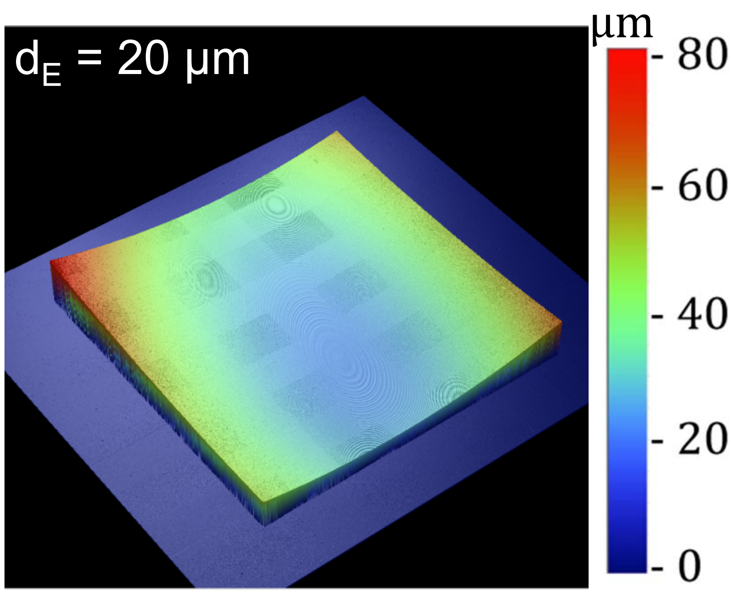
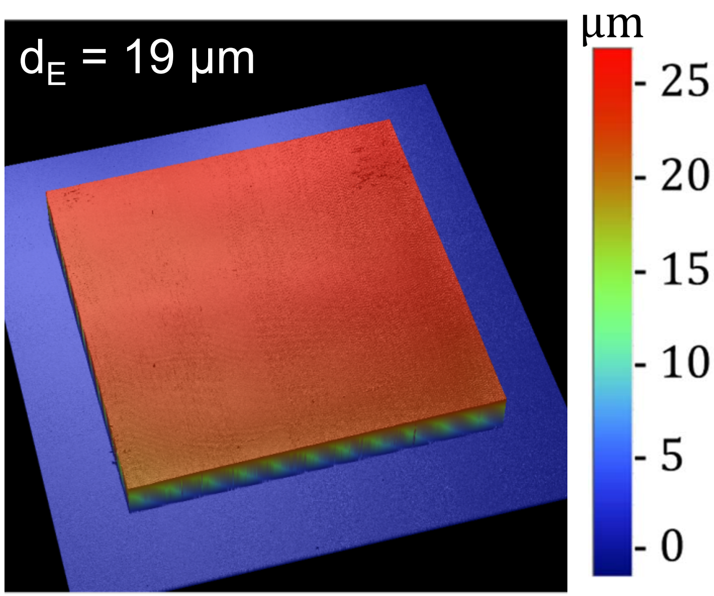
Warpage of the DBG chips

- Before dry-etch post-treatment
- After dry-etch post treatment



$E_{w,DBG} \approx 60$ µm



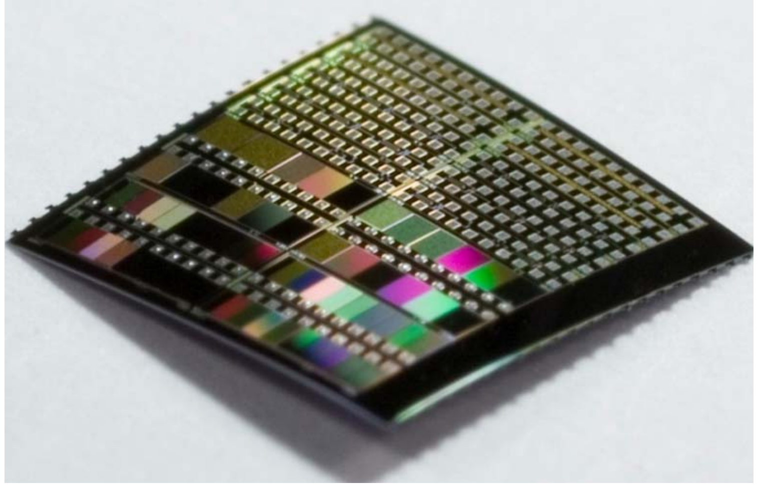
$E_{w,DBG} \approx 10$ µm

→ Reduction of stress and, thus, warpage by dry-etch post processing

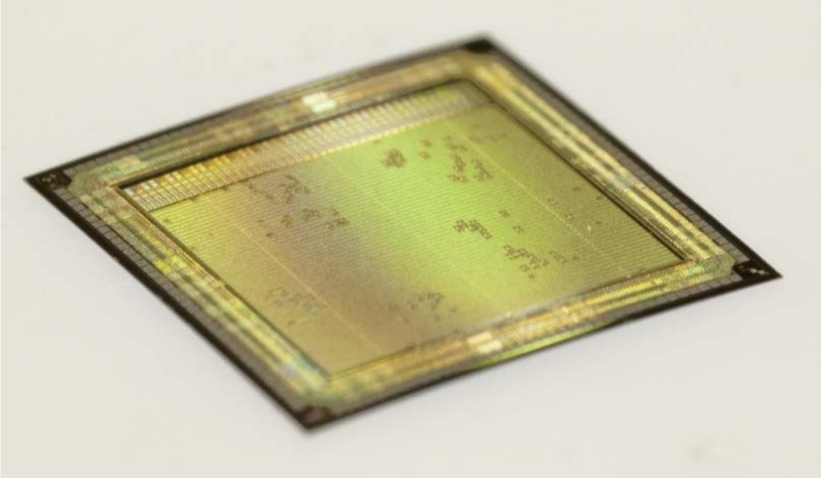
Thin-Chip Warpage (III)

- **Degree of warpage also depends on chip layout**
- **Opportunity to tailor warpage …**
  - … by suitable layout ground rules
  - … through layer and structural stress management

ESTC 2010



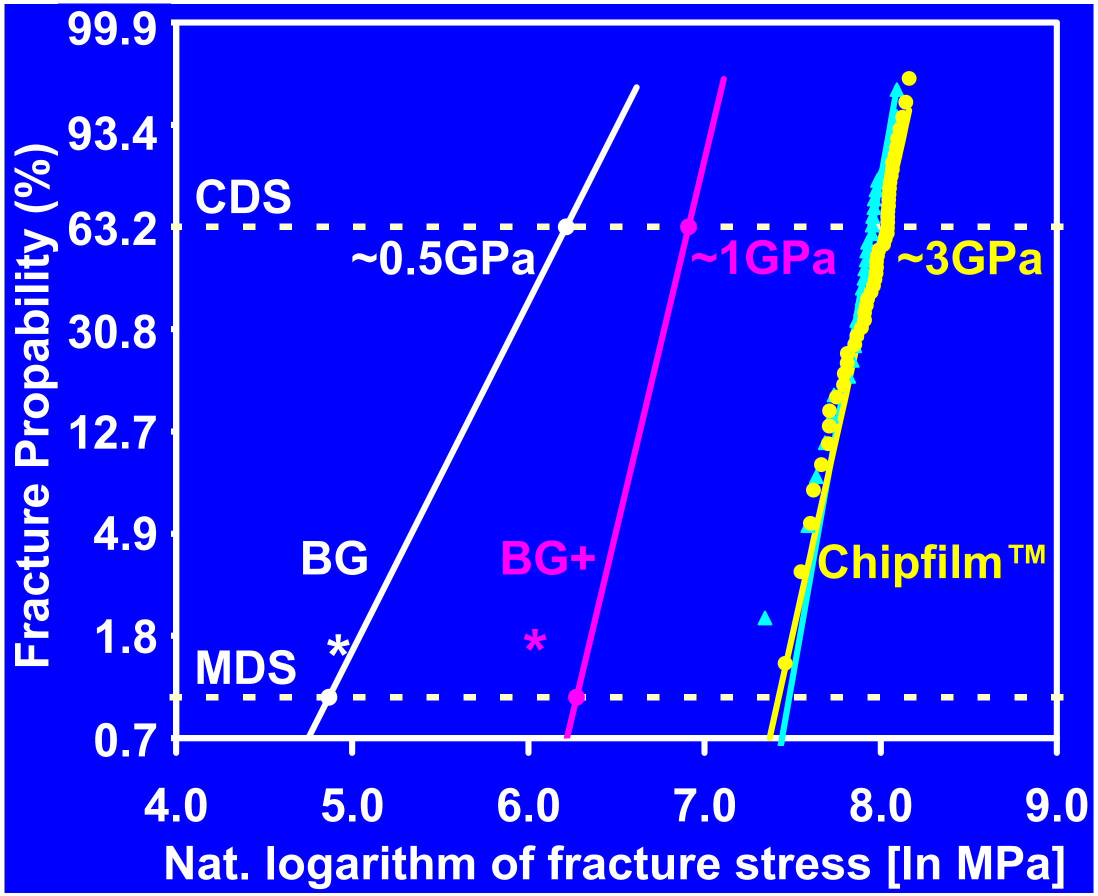
20 µm chip exhibiting severe warpage due to stress



20 µm chip having reduced warpage due to stress management by layout

Mechanical Chip Stability

IEDM 2010



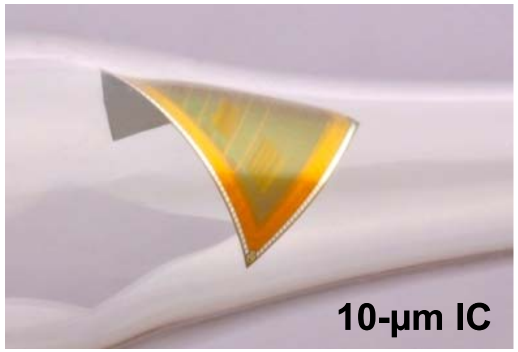
50 µm back-grinded (BG)*

50 µm back-grinded with plasma etch-relief (BG+)*

20 µm Chipfilm™/oxide layer

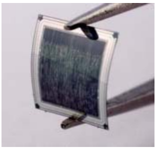
18 µm Chipfilm™ bare Si

* P. M. Heinze, Int. Forum *be-flexible*, Munich, 2008 (data trend lines).

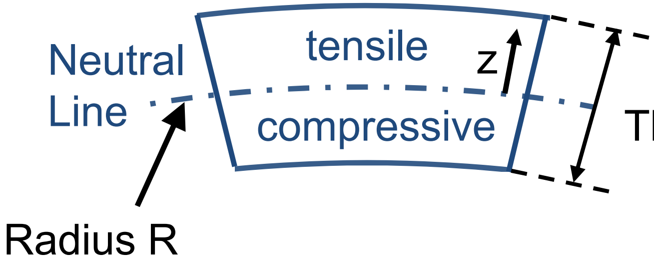


✓ **ChipFilm™ technology offers superior chip stability !**

Piezoresistive Effect (I)



Chip Bending: → Strain ε: → Stress σ:

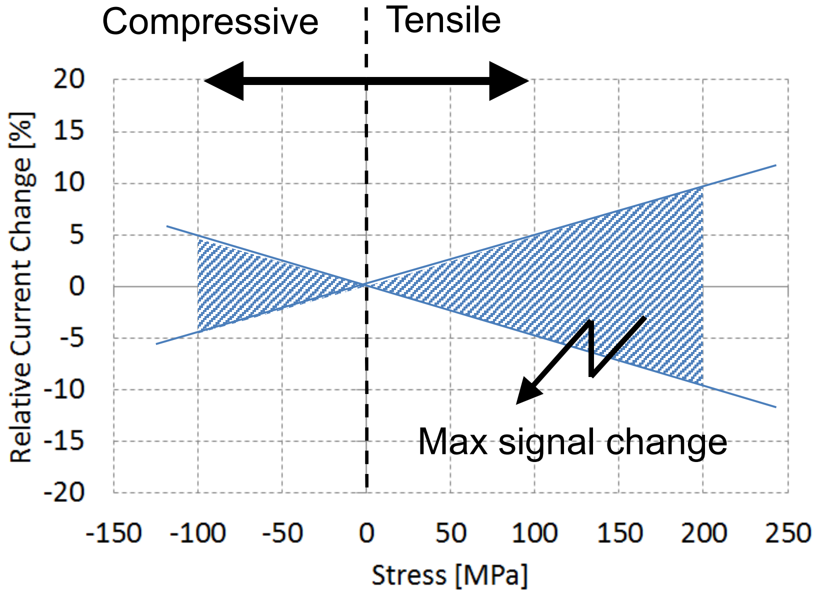


$$\varepsilon = \frac{1}{R} \cdot z$$

$$\sigma = E \cdot \frac{1}{R} \cdot z$$

Piezoresistive Effect in CMOS:

$$\frac{\Delta I}{I} = -\underbrace{\pi}_{\text{Tensor of piezoresistive coefficients}} \cdot \sigma$$

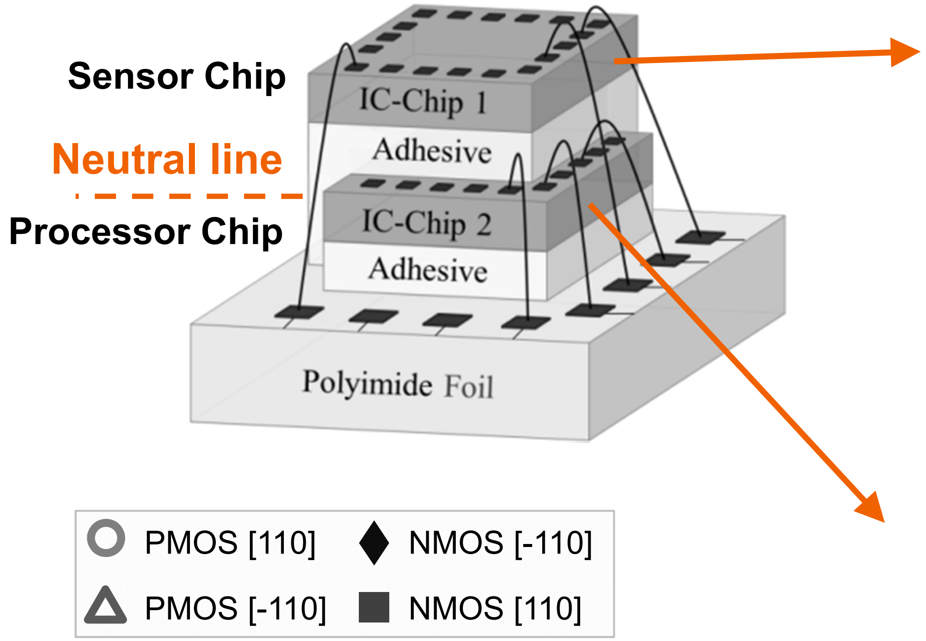


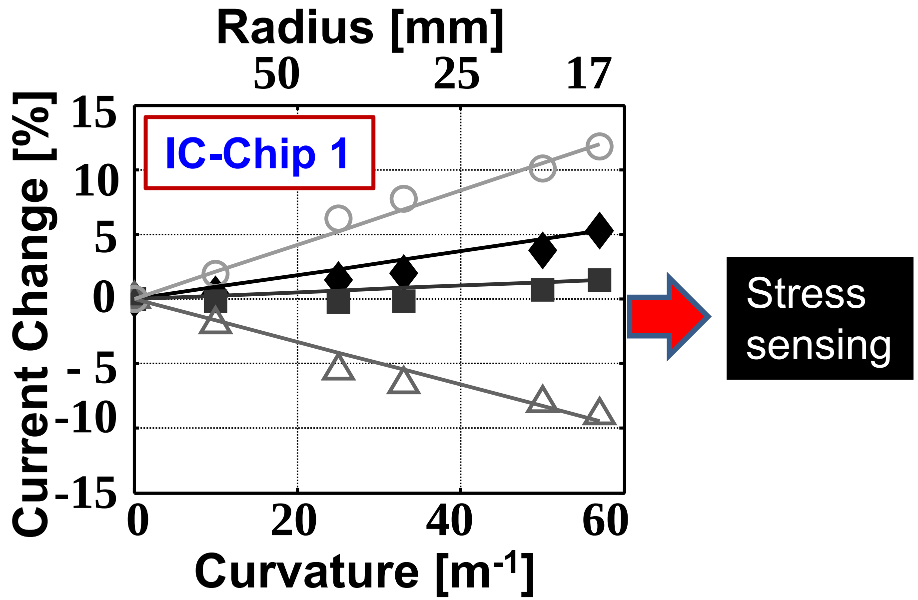
✓ **Active devices receive maximum stress with bending !**

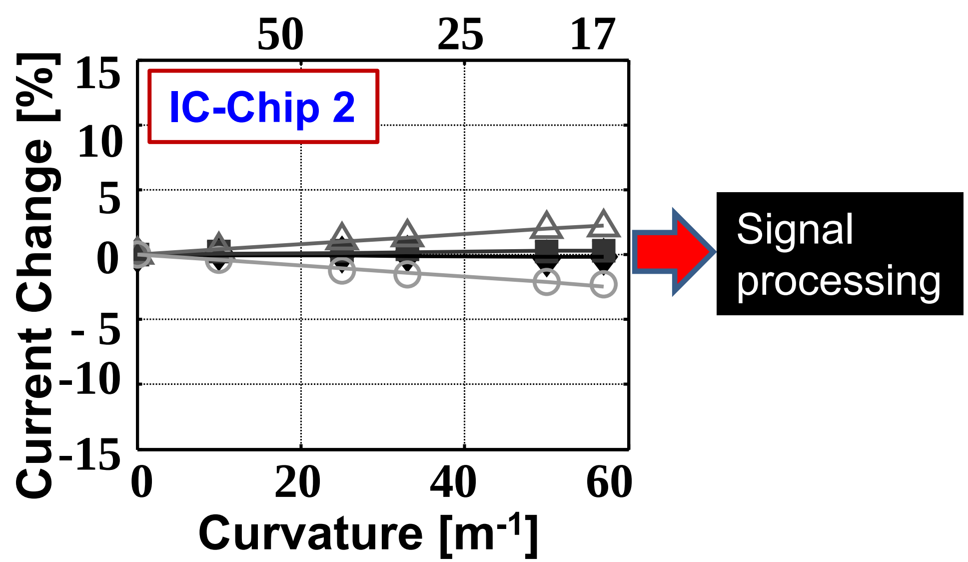
Piezoresistive Effect (II)

IEEE EDL 2011

ESSDERC 2011







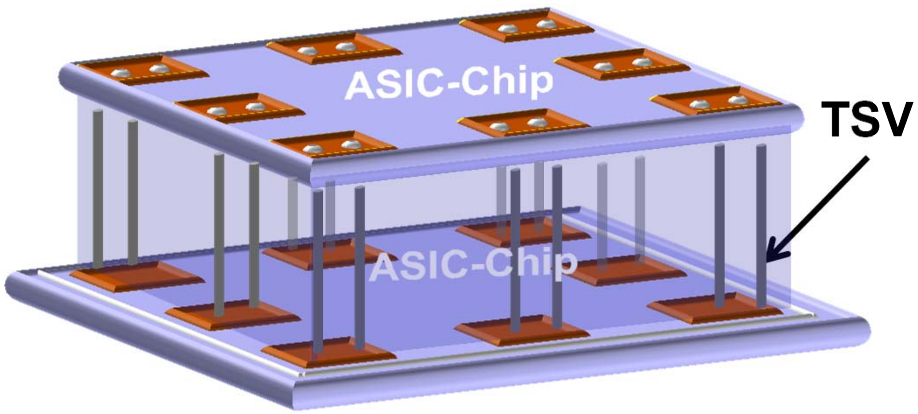
Further benefits:

- Elimination of temperature effects!
- Elimination of vertical stess impact!

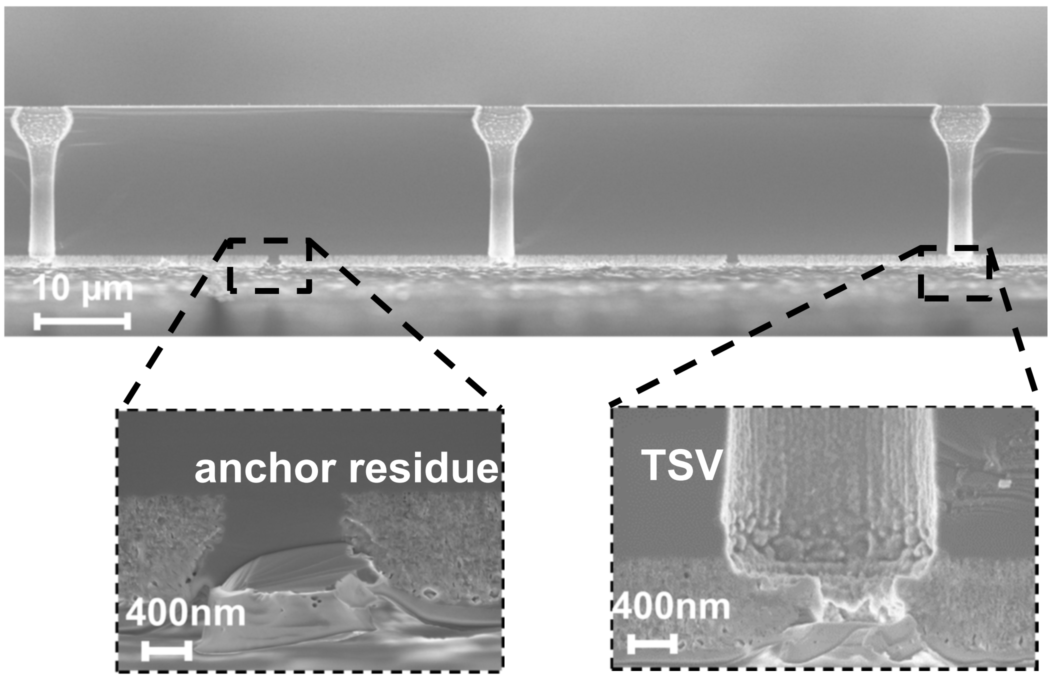
Outline

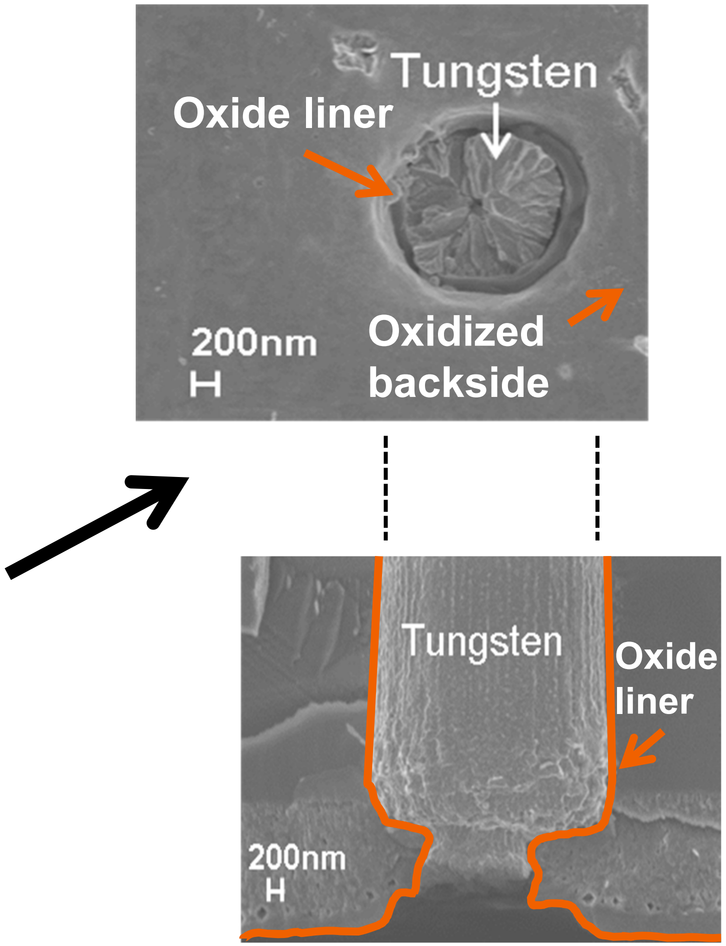
- Introduction to ultra-thin chip applications
- Ultra-thin chip fabrication
  - Dicing-before-Grinding (DBG) technology
  - ChipFilm™ technology
- Characteristics of ultra-thin chips
  - Warpage of thin chips
  - Mechanical stability of ultra-thin chips
  - Piezoresistive effect
- **Ultra-thin chip assembly and embedding**
  - 3D chip stacking
  - Embedding in foil substrates
- The KOSIF project – a technology platform
- Conclusions

3D Chip Stacking



Transducers 2013
EMPC 2015





Assembly & Embedding in Foil

Direct thin-chip embedding

EMPC 2015

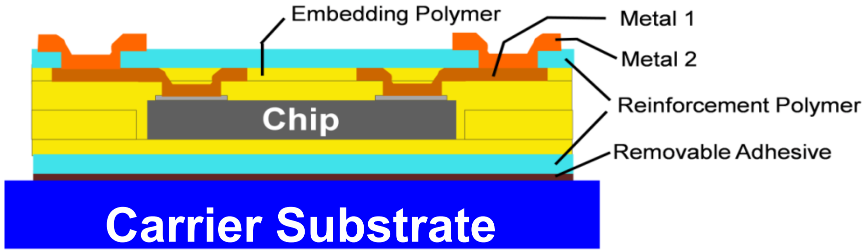
Liquid crystal polymer (LCP) foil

- Assembly-type interconnects
- Structure size 50-100 µm
- Thickness: 60 µm
- Copper metallization
- Laser drilled microvias on chips
- Chip thickness: 20 µm

Courtesy of Würth Elektronik GmbH & Co. KG

ChipFilm Patch®

EMPC 2015



BCB/polymer composite foil

- CMOS-type interconnects
- Structure size : < 10 µm
- Thickness : ~ 50 µm (with 20 µm chip)
- Microvias to pads outside chip area
- Bendability : < 4 mm radius of curvature
- Also feasible as stand-alone foil system

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Research cluster project on Hybrid Systems-in-Foil

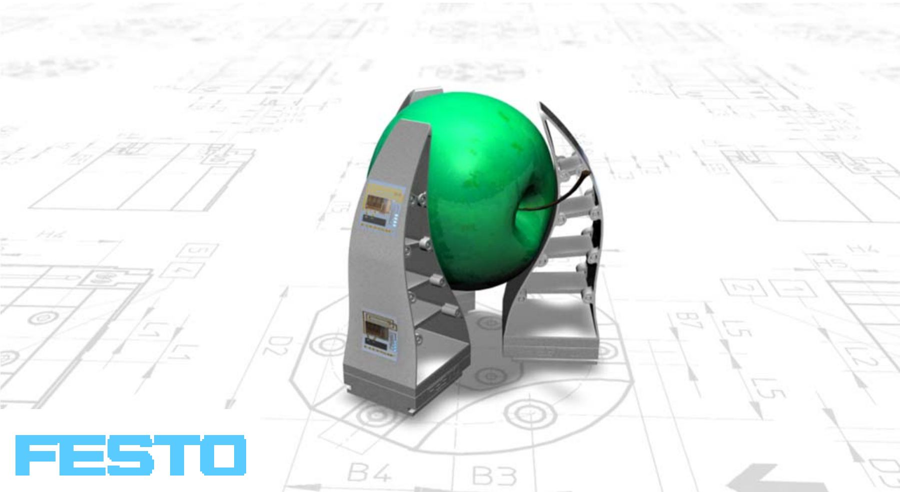
- All partners are from the wider Stuttgart area
- Investigation and benchmarking …
  - … of industrial applications
  - … of candidate technological solutions
- Industrial demonstrators
- Bridge to industrial product applications

http://kosif.ims-chips.de/

Demonstrator 1

Smart Skin

- Sensing force and shape of a pneumatic bionic gripper



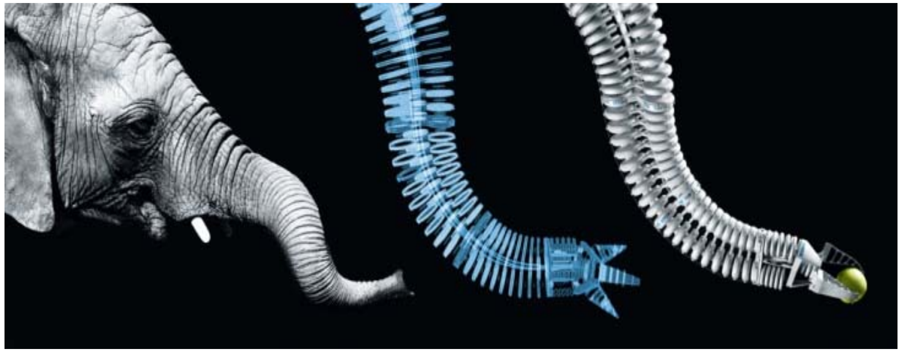
Demonstrator 2

Smart Switch

- Secure, low-cost and form adaptive switch solution

pilz
the spirit of safety

Bionic Handling Assistant



- Sensor controlled gripper
- Wireless communication
- Energy storage/harvester

Bionic Handling Assistant

- Sensor controlled gripper
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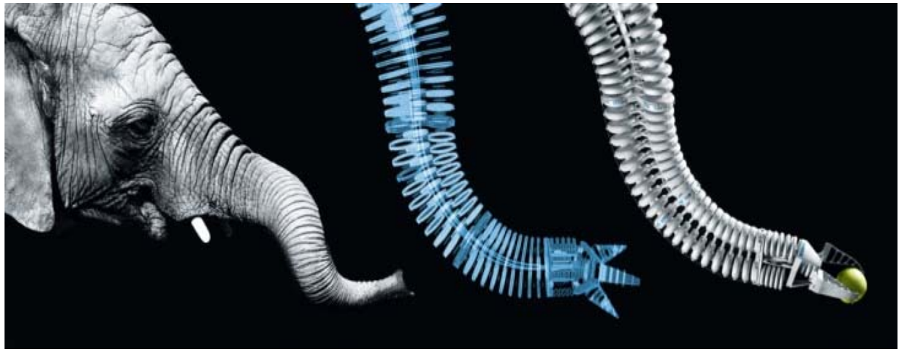
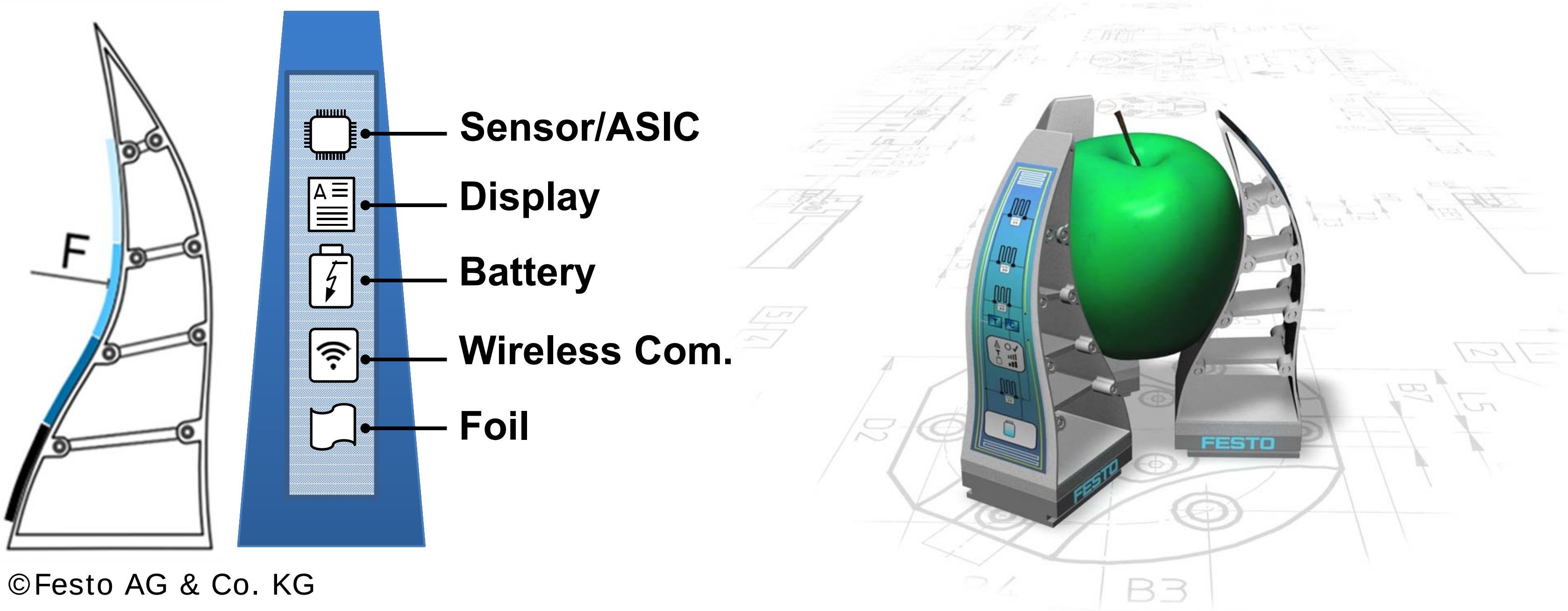
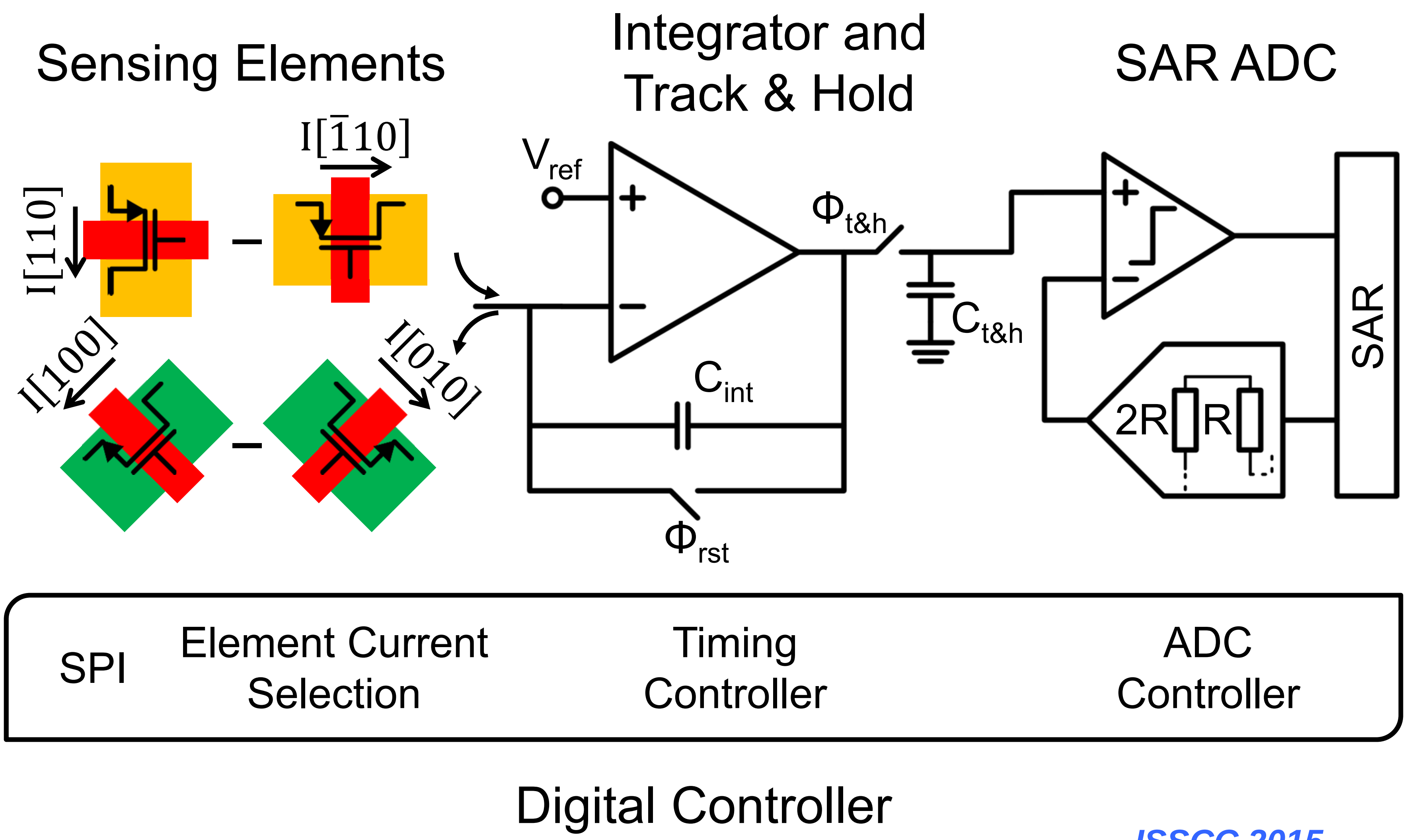
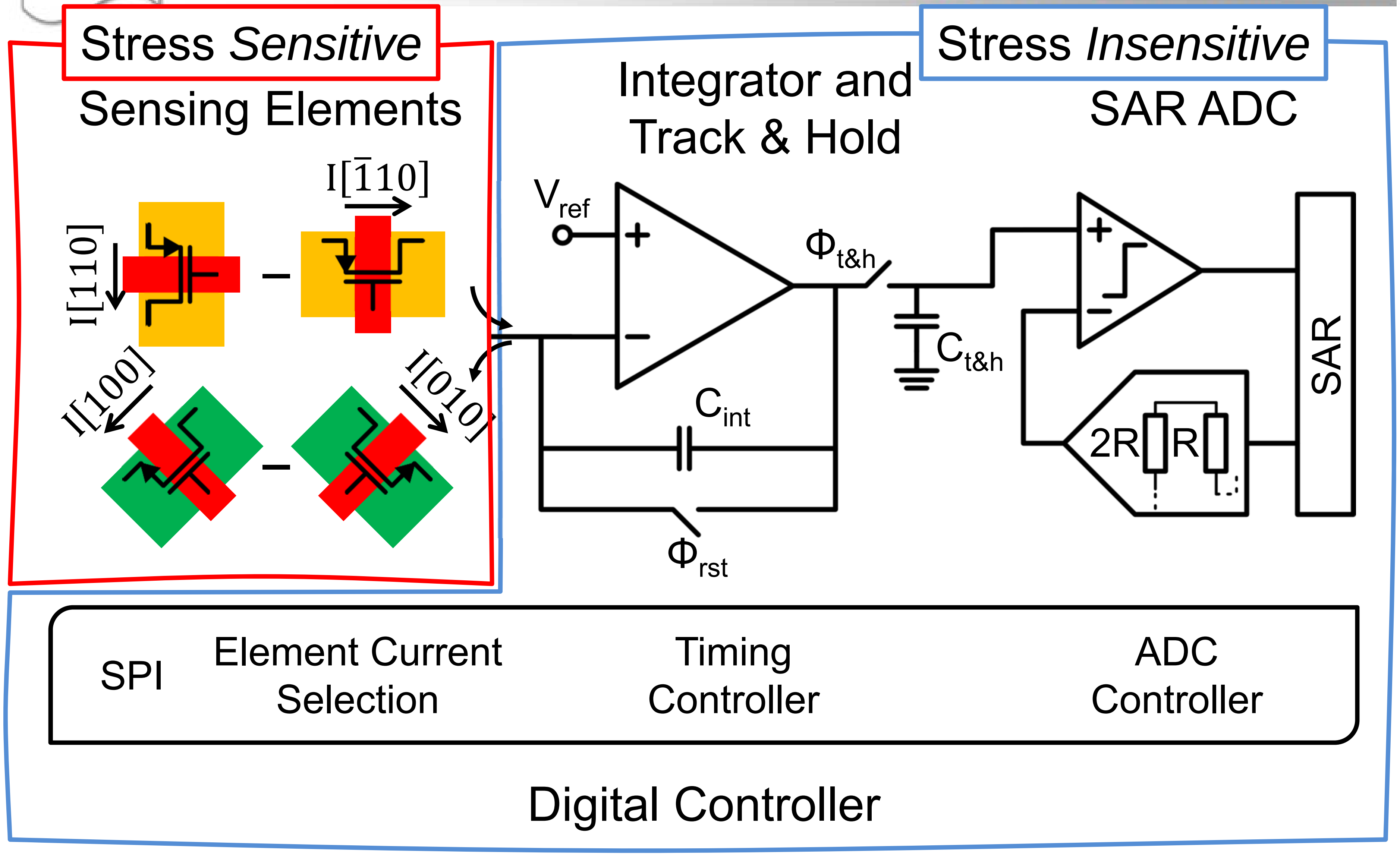





Sensing Elements
Integrator and
Track & Hold
SAR ADC
I[1̄10]
I[110]
I[100]
I[010]
Vref
Φt&h
Ct&h
Cint
Φrst
2R
R
SAR
SPI
Element Current
Selection
Timing
Controller
ADC
Controller
Digital Controller

ISSCC 2015


Stress Sensitive
Sensing Elements
I[1̄10]
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I[010]
Stress Insensitive
Integrator and
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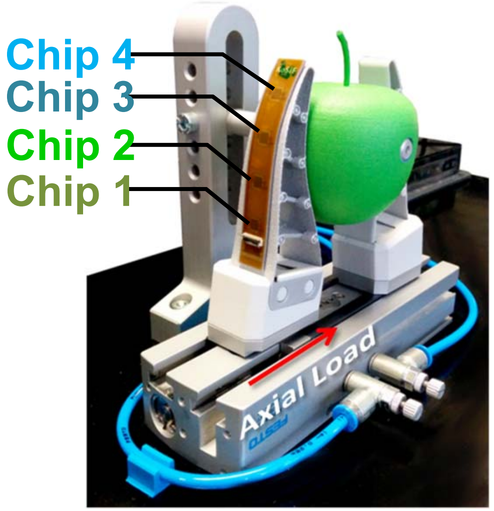
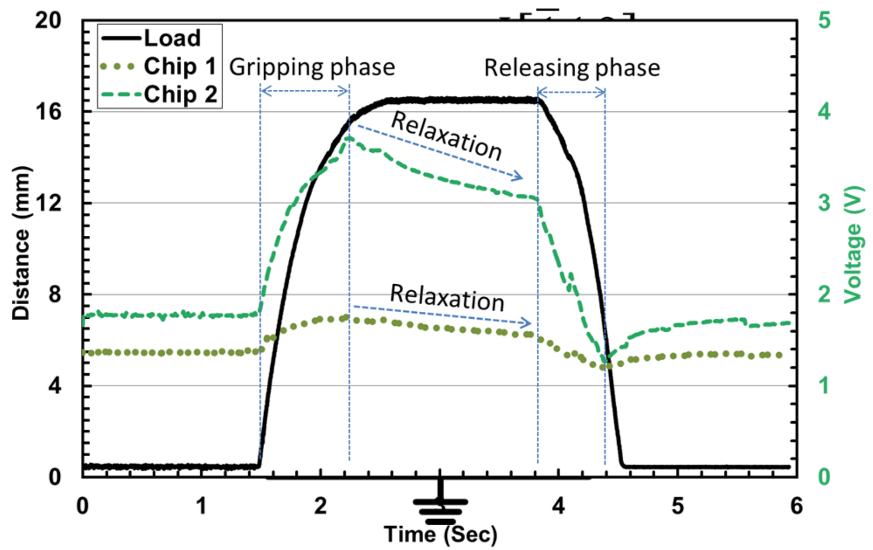
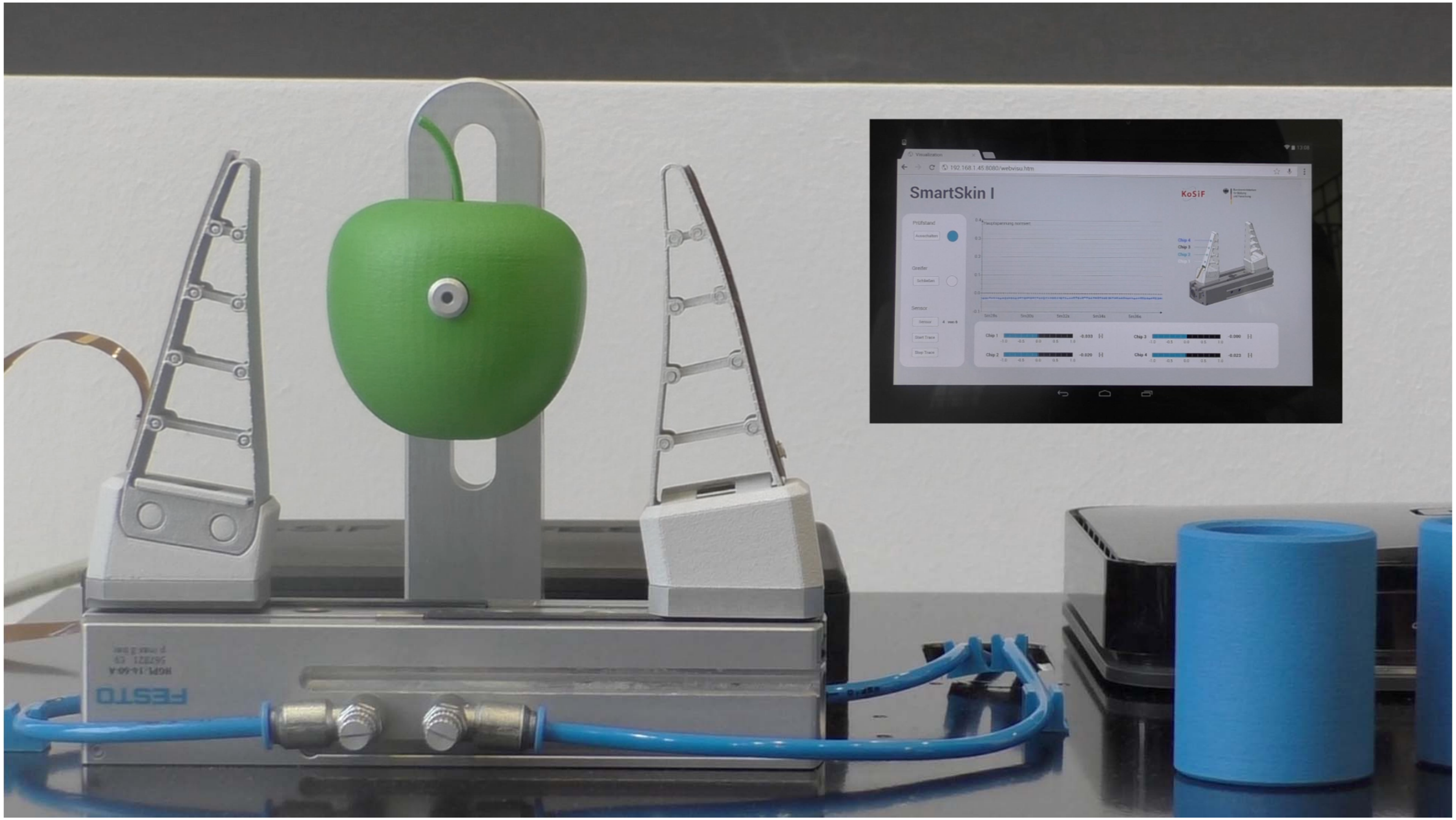
SAR ADC
Vref
Φt&h
Ct&h
Cint
Φrst
2R
R
SAR
SPI
Element Current
Selection
Timing
Controller
ADC
Controller
Digital Controller

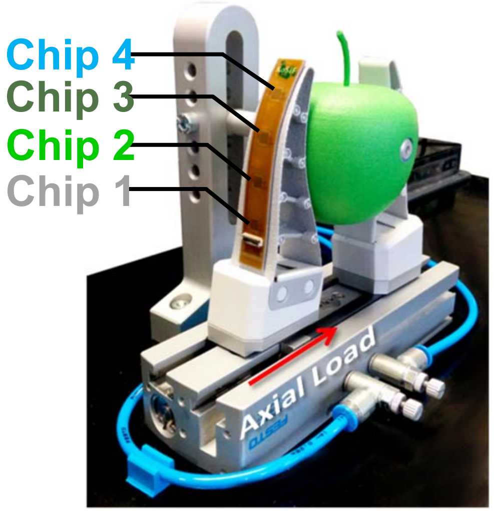
- **Piezoresistive effect based stress sensing**
- **Orthogonal NMOS and PMOS transistors in current mirrors**
- **Conversion of current to voltage signals by *trans-impedance amplifier***

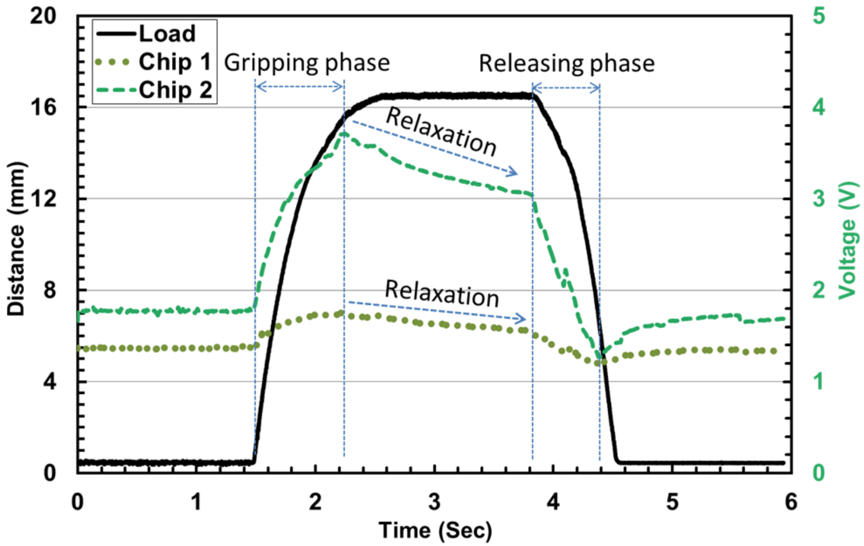





SmartSkin I
KoSiF
FESTO

- **Piezoresistive effect based stress sensing**
- **Orthogonal NMOS and PMOS transistors in current mirrors**
- **Conversion of current to voltage signals by *trans-impedance amplifier***
- **Relaxation effect**
  - **Associated to glue relaxation over time**
  - **Hysteresis effect of the gripper material**
- **Signals from all 4 chips need to be processed with suitable algorithm**





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Conclusions

- **Hybrid Systems-in-Foil (HySiF)** are enablers of industrial high-performance, reliable, secure and cost-efficient solutions in flexible electronic applications
- The implementation of ultra-thin chips in flexible electronic system features a **paradigm shift in silicon technology**
- **Ultra-thin chip technology** for flexible electronics needs to be optimized for high mechanical bendability and reliability, minimum warpage and cost-effective manufacturing
- The **KOSIF project** creates a technology platform for HySiF aiming at high-performance industrial applications

Our Publications on Ultra-Thin Chips

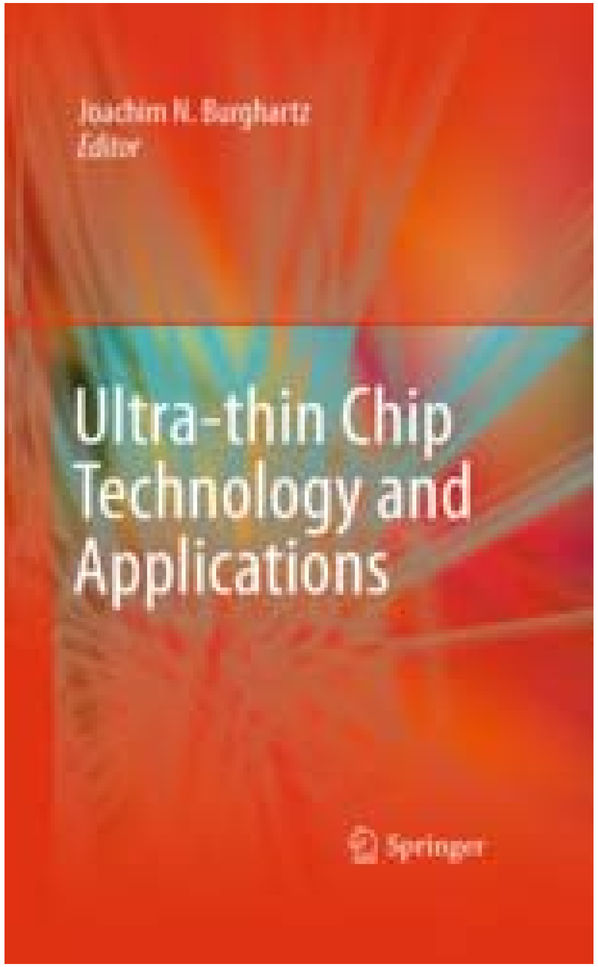
ieee spectrum INSIDE TECHNOLOGY

appeared in

March 2013

YOU CAN'T BE TOO THIN OR TOO FLEXIBLE

ULTRATHIN, FLEXIBLE SILICON TECHNOLOGY WILL IMPROVE 3-D CHIPS— AND A LOT MORE BESIDES



Other Publications:

- ESSDERC-ESSCIRC 2009 (Athens, Greece)
- IEDM 2006 (San Francisco, USA)
- ISSCC 2008 (San Francisco, USA)
- IEDM 2009 (Baltimore, USA)
- IEDM 2010 (San Francisco, USA)
- IEEE Trans. El. Dev., 2009

1st Edition., 2011, XXII, 467 p. 252 illus., 157 in color., Hardcover
ISBN: 978-1-4419-7275-0

