Electronics and Energy Applications of 1D and 2D Nanomaterials

Eric Pop

Electrical Engineering (EE) and Precourt Institute for Energy (PIE)
Stanford University

http://poplab.stanford.edu

Acknowledgements

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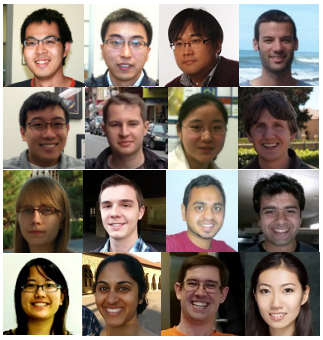
- Alumni:
  - Prof. D. Estrada, Drs. Z.-Y. Ong, A. Liao, J. Wood, Z. Li, V. Dorgan, F. Xiong, Z. Li, E. Carrion, S. Islam, K. Grosse
  - 8 M.S. and 10 B.S. theses
- Post-docs:
  - Feng Xiong, Yong Cheol Shin, Eilam Yalon, Miguel Munoz
- Grad students:
  - C. English, F. Lian, S. Deshmukh, S. Bohaichuk
  - M. Mleczko, C. Neumann, I. Datye, M. Chen, A. Gabourie
  - K. Smithe, S. Suryavanshi, N. Wang, R.L. Xu, C. McClellan
- Undergrads:
  - Andrew, Tim, Job, Justin, Yeshar, Erin



- Sponsors:
  - National Science Foundation (NSF), Army Research Office (ARO)
  - Air Force (AFOSR), Intel, STARnet-SONIC, **SystemX Alliance**

- Collaborators:
  - Z. Bao, K. Goodson, S. Mitra, Y. Nishi, E. Reed, K. Saraswat, H.-S.P. Wong (Stanford), D. Cahill, W. King, J. Lyding, J. Rogers, M. Shim (UIUC), M. Rudan (Bologna), C. Jacoboni (Modena), M. Hersam (NWU), I. Knezevic (Wisc.), D. Jena (Cornell), D. Ielmini, R. Sordan (Milano), J. Shiomi (Tokyo)

What Motivates Us

(IBM Watson, *Jeopardy!* champion)

20 Watts

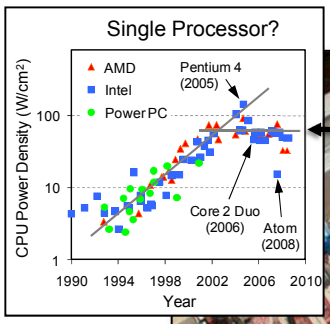
200 kiloWatts

10,000x

(conventional Moore's Law size scaling can get us ~10x)

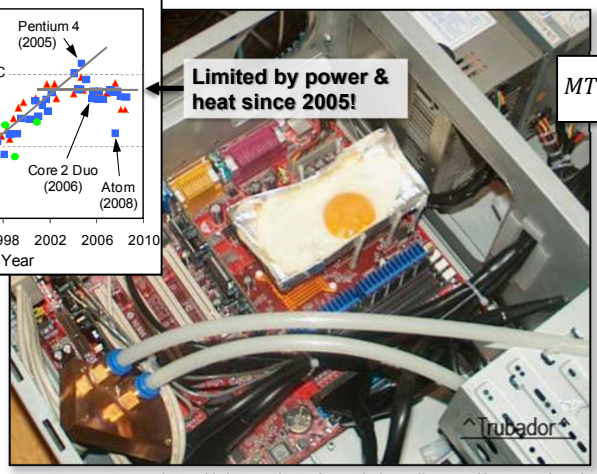
Electronics Use (and Waste) Much Power

E. Pop, *Nano Research* 3, 147 (2010)
new course: Energy in Electronics, EE 323 (Fall 2014)



Limited by power & heat since 2005!

$$MTF \sim \exp\left(\frac{E_A}{k_B T}\right)$$



http://phys.ncku.edu.tw/~htsu/humor/fry_egg.html

energy limits performance from processors, to mobile devices, to data centers

Electronics Use (and Waste) Much Power

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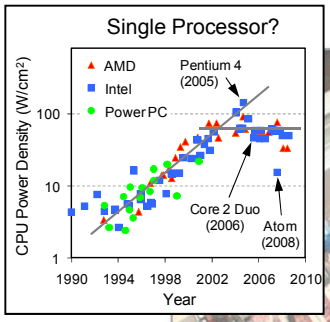
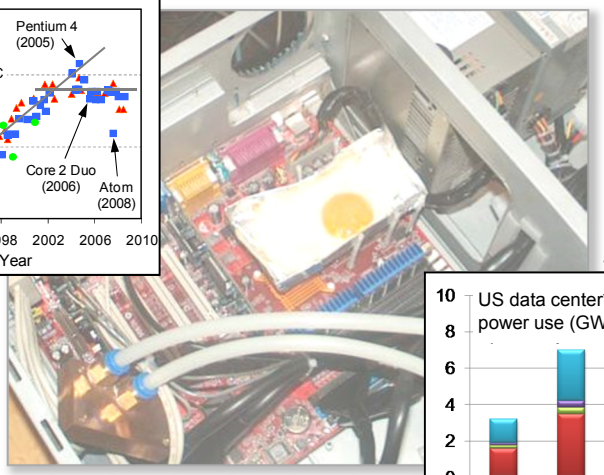
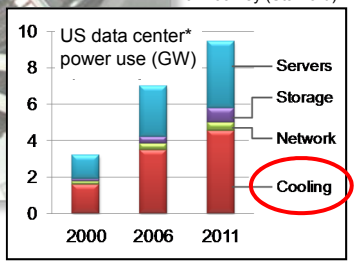




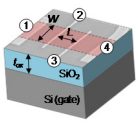
J. Koomey (Stanford)

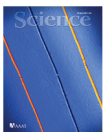


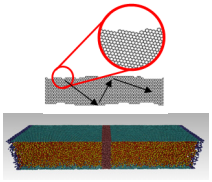
Calibrating: 1 GW ~ 1 nuclear power plant
12 GW ~ all electricity used by Argentina

*World-Wide about 30 GW

Our Work: Two Sides of the Same Coin





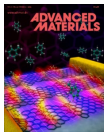


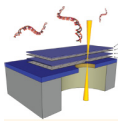
Lower power at its source

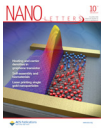
(devices, sensors, circuits)

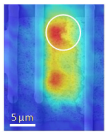
Harvest and manage heat

(energy, thermoelectrics)





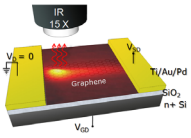


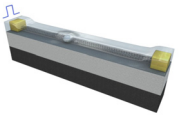


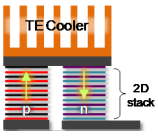
fundamental understanding
practical applications

Outline of Talk

- **The SystemX Alliance at Stanford**
- **Transistors**
  - Heterogeneous integration of beyond-Si materials
- **Data Storage**
  - Approaching limits of phase-change memory
- **Thermal Energy at Nanoscale**
  - Ballistic heat flow and fundamental limits

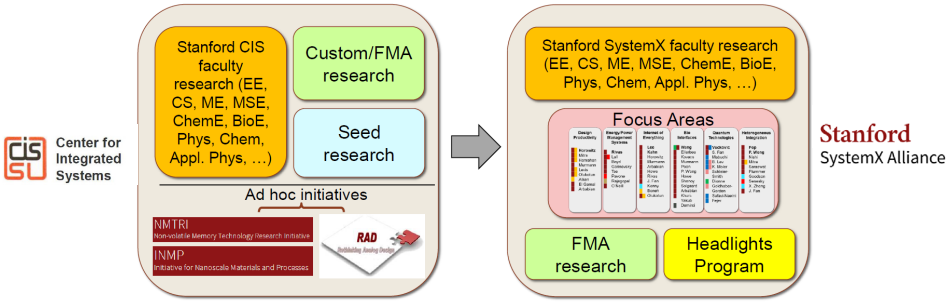






What Is the SystemX Alliance at Stanford?

- Center for Integrated Systems (CIS) → SystemX Alliance
  - Industry-academic Alliance to repositioned for 21st century research
  - Become "the" hub for electronic research at Stanford

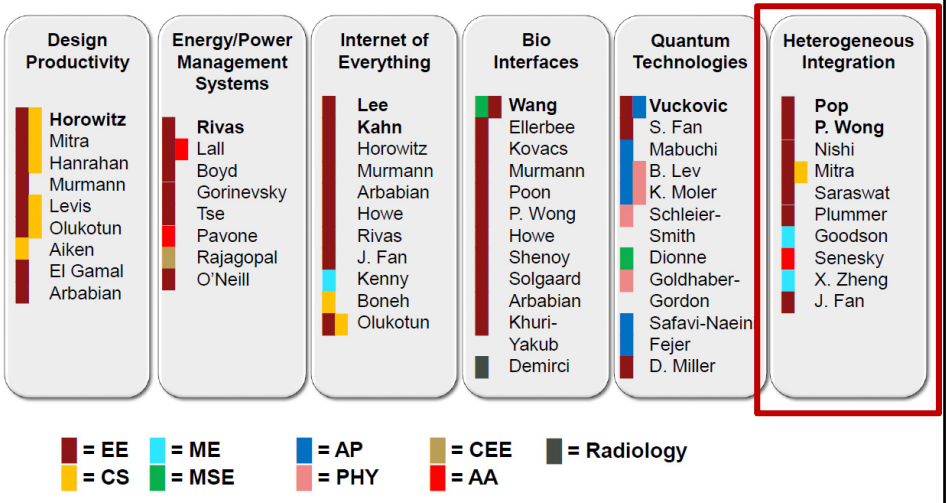


- What's New?
  - Stronger emphasis of top-down, **systems research**
  - Introduce **focus areas** to create coherent thrusts
  - Additional **sponsor benefits** including workshops, E-Seminars

Value Proposition for Industry Sponsors

- See **everything** that is going on at Stanford
  - Real-time **view of all faculty research**, including NSF, DARPA, etc. activities
  - **Student** recruiting, internships, and networking
- Participation in Focus Area research
  - Invitation-only attendance to **bi-annual workshop** & discussion
- Customized Fellow-Mentor-Advisor (FMA) projects
  - **Company-specific research** performed by student & advisor with industry mentor
- Faculty liaisons, company visits, and weekly **E-Seminars**

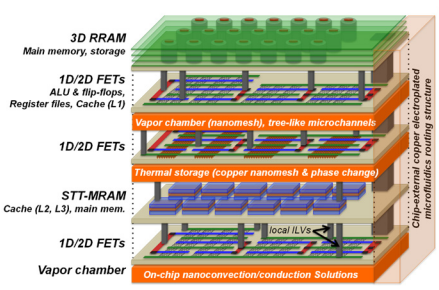
SystemX Focus Areas

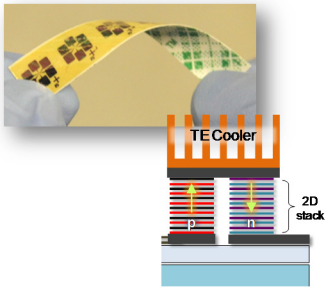


- Focus areas change dynamically and have finite life-cycle (~3-5 years)

Heterogeneous Integration Focus Area

- Heterogeneous Integration of Everything onto Anything (HIEA)
- Integration of "beyond-Si" platforms for "beyond Moore" applications
  - Monolithic integration of logic, memory, sensors, thermal management, flexible substrates
  - Energy-efficient and brain-inspired design opportunities
  - Autonomous electronics and energy-harvesting opportunities

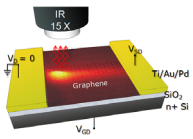




- Core faculty: E. Pop, H.-S.P. Wong (co-leads), J. Fan, K. Goodson, S. Mitra, Y. Nishi, J. Plummer, K. Saraswat, D. Senesky, X. Zheng

Outline of Talk

- The SystemX Alliance at Stanford



- **Transistors**
  - Integration of electronics based on 2D materials

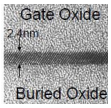
- Data Storage
  - Approaching limits of phase-change memory

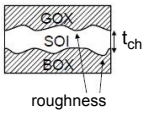
- Thermal Energy at Nanoscale
  - Ballistic heat flow and fundamental limits

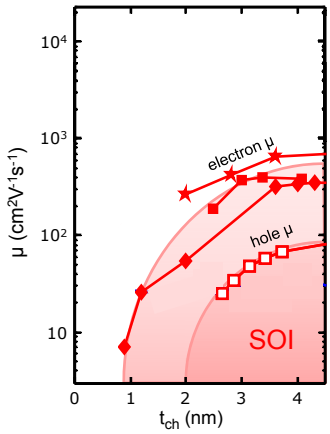
Transistors Beyond Silicon?

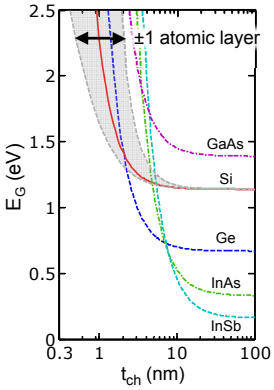
- **Problem:** 20th century transistors "carved" out of **3D** materials (Si) → surface roughness restricts mobility, band gap, variability

3D









Transistors Beyond Silicon?

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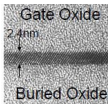
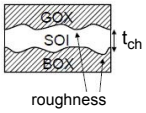
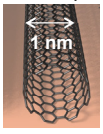
3D



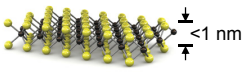


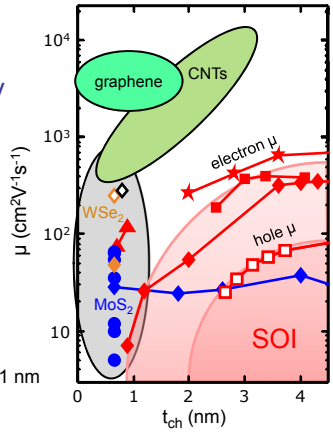
- **Solution?** 21st century atomically thin materials

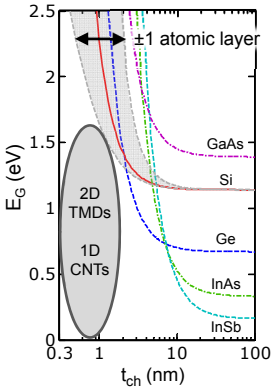
1D carbon nanotube (CNT)



2D TMD (MoS_2, WTe_2, $ZrSe_2$)

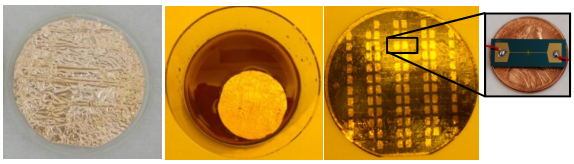


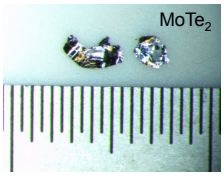


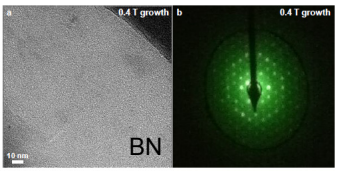


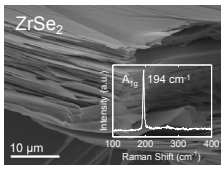
Beyond-Silicon 2D Materials

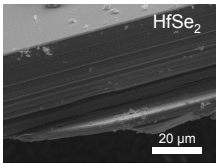
CVD growth of graphene, BN and MoS_2

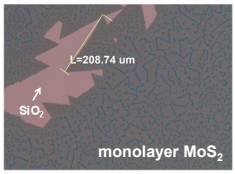


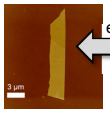




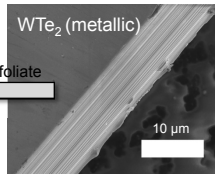


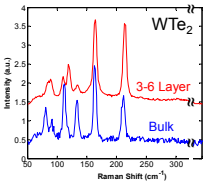






exfoliate

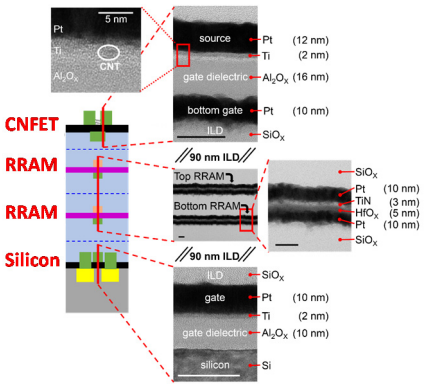


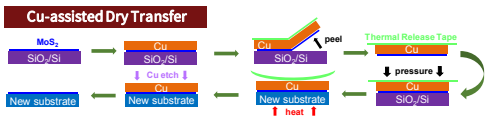


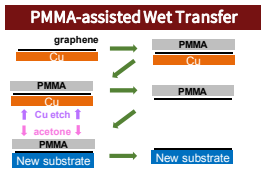
collab. H.S.-P. Wong, Y. Nishi, I. Fisher

CVT growth of $MoTe_2$, WTe_2, $ZrSe_2$, $HfSe_2$

Heterogeneous Integration Progress







Monolithic 3D: low-temperature 3D integration of CNT logic and RRAM memory on CMOS substrate

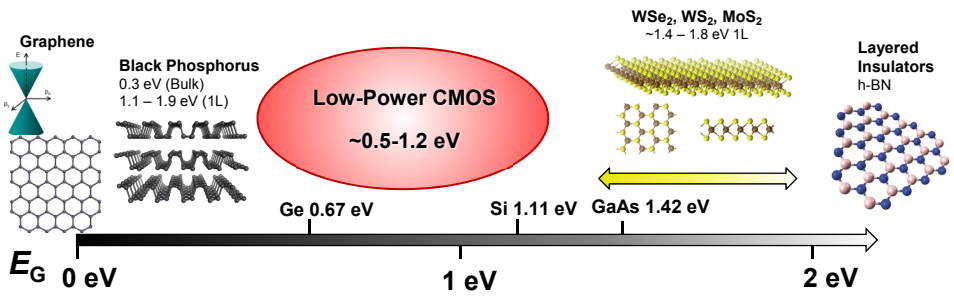
source: Shulaker, Wong, Mitra (IEDM-2014)

Wet or Dry Transfer: layer transfer of 2D monolayers onto insulators while preserving the electronic properties

source: K. Smithe (Pop Lab, 2015)

Band Gaps (E_G) of Several 2D Materials

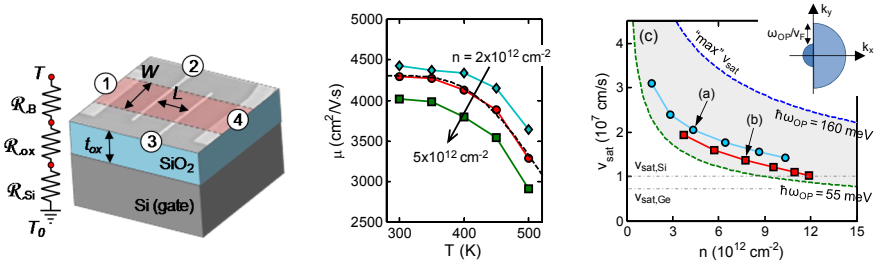
courtesy of M. Mleczko (Pop Lab)



- Low-E_G but high mobility → high-speed and RF applications
- Medium-E_G (0.3 to 1.1 eV) → low-power CMOS
- High-E_G → power devices

Early Work: Graphene Transport Parameters

V. Dorgan, M.-H. Bae, E. Pop, *Appl. Phys. Lett.* 97, 082112 (2010)



$$\Delta T = T - T_0 \approx P\left(\mathcal{R}_B + \mathcal{R}_{ox} + \mathcal{R}_{Si}\right)$$

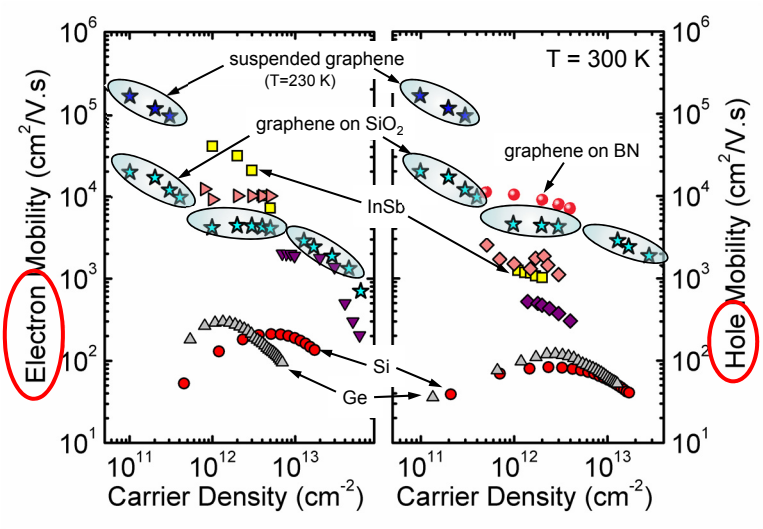
$$\mu(n,T) = \frac{\mu_0}{1+\left(n/n_{ref}\right)^{\alpha}} \times \frac{1}{1+\left(T/T_{ref}-1\right)^{\beta}}$$

$$v_{sat}(n,T) = \frac{2}{\pi}\frac{\omega_{OP}}{\sqrt{\pi n}}\sqrt{1-\frac{\omega_{OP}^2}{4\pi n v_F^2}}\frac{1}{N_{OP}+1}$$

- Lack of transport data* at T > 300 K and high-field v_{sat} (>1 V/μm)
- High-field v_{sat} measurement is tricky, needs constant field
- Also extracted practical electrical and thermal compact models

*J.-H. Chen, Nature Nano (2008); W. Zhu, PRB (2009); I. Meric, Nature Nano (2008)

Graphene Mobility – Where Does it Stand?

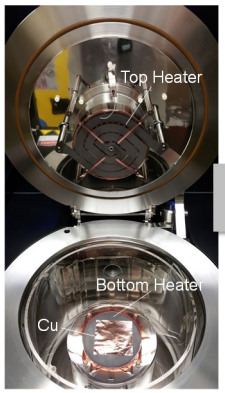


mobility = characterizes "ease" of current flow in a material; e.g. $I \alpha n\mu E$

Today: Graphene-Based Functions and Systems

- Goal: graphene switched analog circuit (SAC). Why?
- Graphene = nanofabrics with high mobility (~10x > Si), flexible…
- SAC tolerates low I_{on}/I_{off} ratio (~5x) of graphene (no band gap)
- Breakthroughs in heterogeneous integration of graphene & CMOS

4" Aixtron Black Magic System



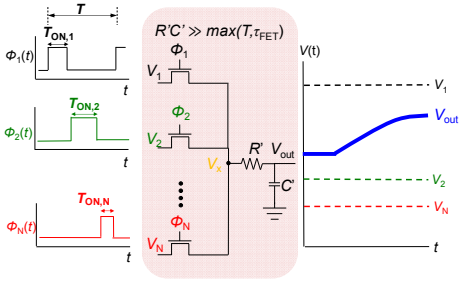
Growth Chamber

Graphene Dot Product (GDOT) Nanofunction

N. Wang, S. Gonugondla, I. Nahlus, N. Shanbhag, E. Pop, *VLSI Symp.* (2016)

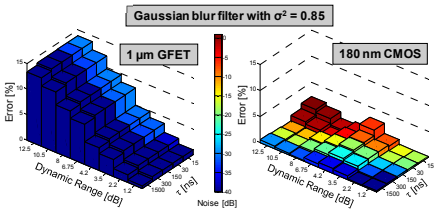
- Dot product nanofunction used for image processing, neural networks…
- Takes advantage of native graphene properties, tolerates drawbacks

Idea:



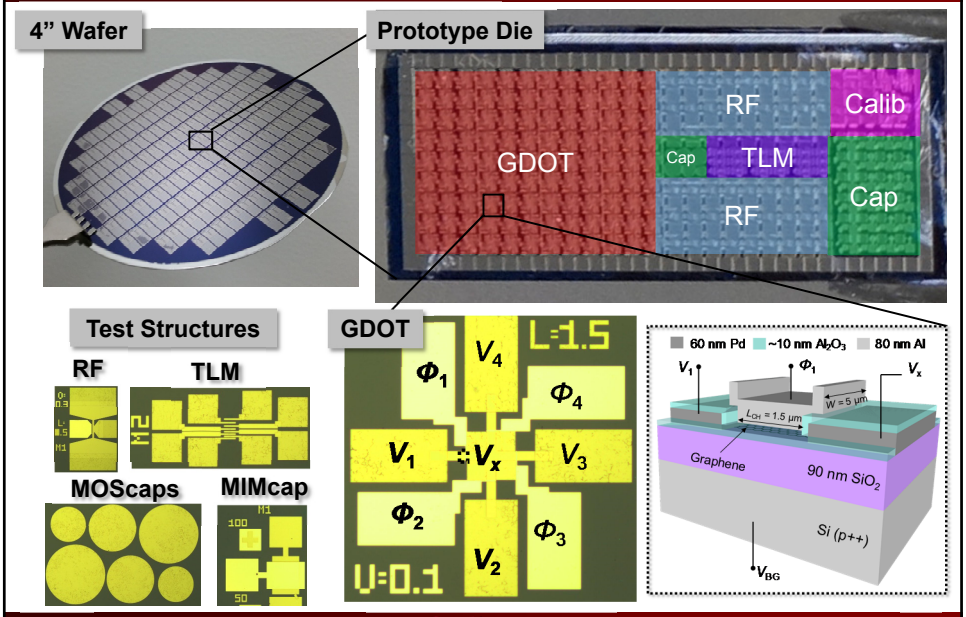
weights encoded by pulse widths $p_i T$

Simulation:



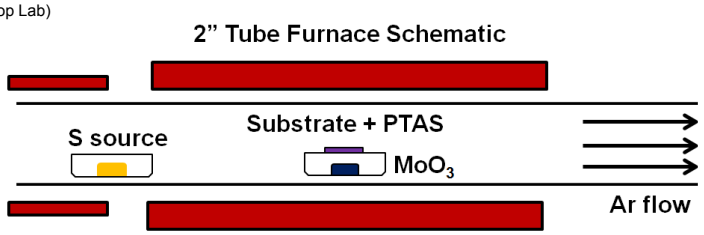
+ Fast	+ High accuracy
+ Smaller area	+ Wide input range
+ Low noise	- Slow and noisy
- Narrow input range	- Larger area

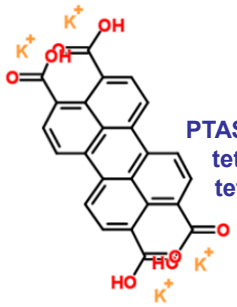
… and Implementation



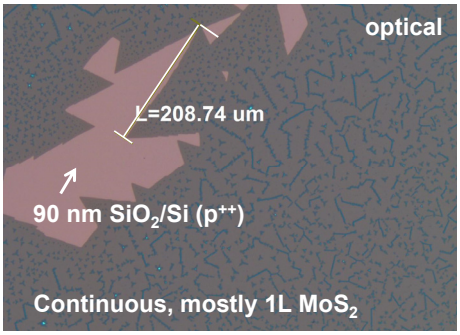
CVD Growth of Monolayer MoS_2

Kirby Smithe (Pop Lab)





PTAS: perylene-3,4,9,10-tetracarboxylic acid tetrapotassium salt

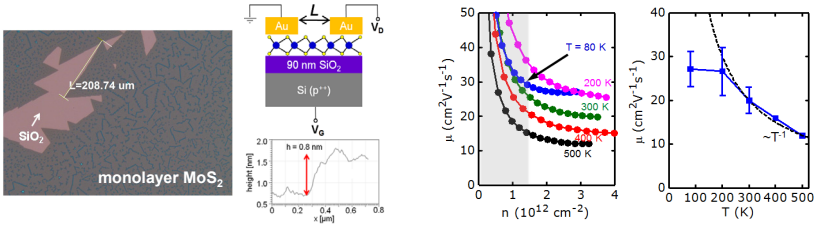


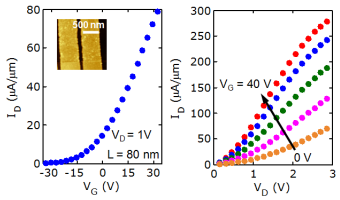
Y.-H. Lee, et al., *Nano Lett.* **13**, 1852 (2013)
Y.-H. Lee, et al., *Adv. Mater.* **24**, 2320 (2012)

Digital Electronics → Monolayer CVD MoS_2

K. Smithe, C. English, S. Suryavanshi, E. Pop, *Device Research Conf.* (2015)

- Large-area monolayer CVD MoS_2, direct band gap ~1.8 eV
- Wish to scale up devices for low-power **digital** electronics



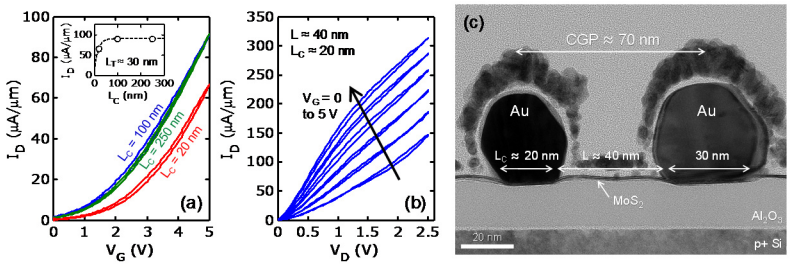


Good current achieved (~275 μA/μm) in 80 nm device, but contact resistance remains dominant

Scaled Semiconducting MoS_2 Transistors

Goal: Aggressively scale 2D transistors (e.g. MoS_2) for ultra-low power *digital* electronics

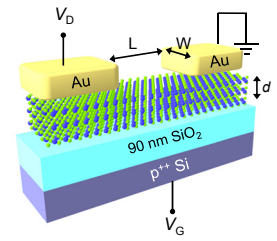
Source: C. English, G. Shine, K. Saraswat, E. Pop, *Nano Lett.* (2016)

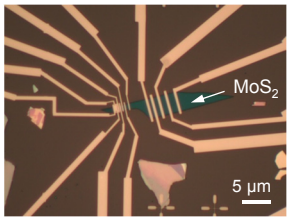


- Demonstrated how **contacts are limiting** the performance of small MoS_2 transistors
- Built devices with ~40 nm channel length and variable contact sizing (L_C = 20 to 100 nm)
- **Smallest MoS_2 transistor with smallest contacts to date** (contacted gate pitch CGP ~ 70 nm, smaller than "22 nm" Si technology from Intel and Samsung

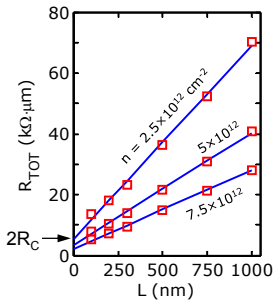
Metal Contacts to MoS_2 (Clean but Undoped)

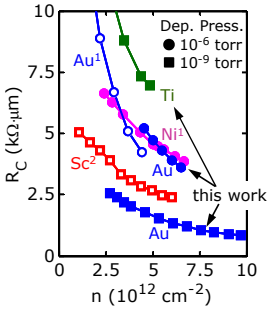
C. English, G. Shine, V. Dorgan, K. Saraswat, E. Pop, *Device Research Conf.* (2014)





Transfer Length Method (TLM)



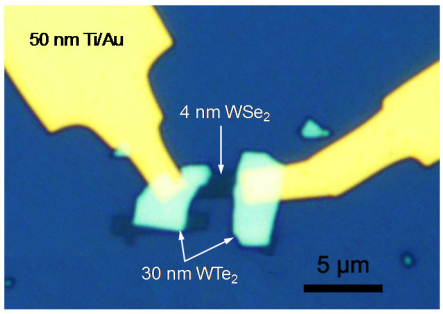


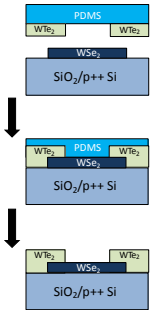
- Contacting 2D materials is **difficult**
- Cleaner Au deposition (~10^{-9} torr) leads to improved contact resistance
  - R_C ~ 740 Ω·μm and $\rho_C \approx 4 \times 10^{-7}$ Ω·cm²

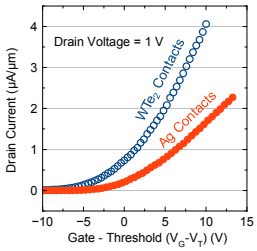
[1]H.Liu & P. Ye (2013), [2]S. Das & J. Appenzeller (2013)

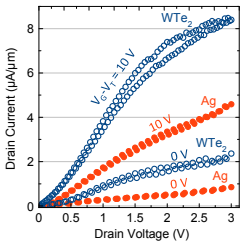
2D Contacts to 2D Transistors

C. McClellan, M. Mleczko, Y. Nishi, E. Pop, *Device Research Conf.* 2016





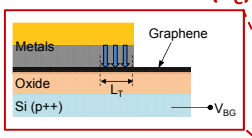


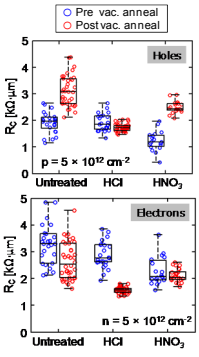


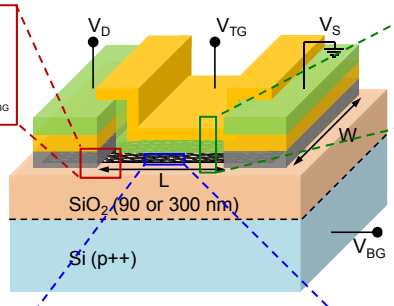
- WTe_2 (2D metal) contacts to WSe_2 (semic.)
- Residue-free transfer process
- 2x improvement over Ag contacts ("best known")
- Observed current saturation

Summary of Challenges in 2D Devices

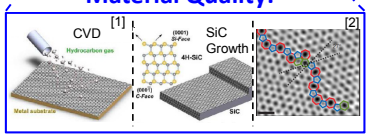
Contact Resistance (R_C):





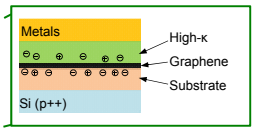


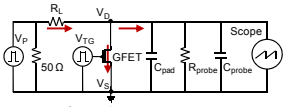
Material Quality:

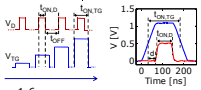


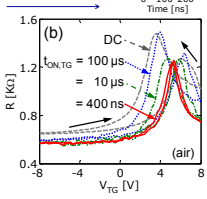
+Variability!

Interfaces:





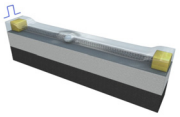




E. Carrion, E. Pop et al, *IEEE TED*, 61, 1583 (2014)

Outline of Talk

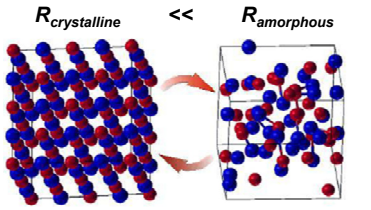
- The SystemX Alliance at Stanford
- Transistors
  - Integration of electronics based on 2D materials
- **Data Storage**
  - Approaching limits of phase-change memory
- Thermal Energy at Nanoscale
  - Ballistic heat flow and fundamental limits



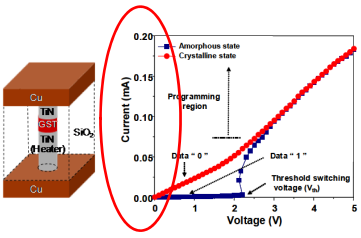
Phase-Change Memory (PCM) Materials

- Chalcogenide compound: $Ge_2Sb_2Te_5$ (GST)
- Used in RW-DVDs

- Crystalline vs. amorphous: fast phase change (~1 ns)
- Large change in resistance (>100x)
- Promising candidate for memory, BUT… high programming current (~0.1 mA at IBM, Intel, Samsung)



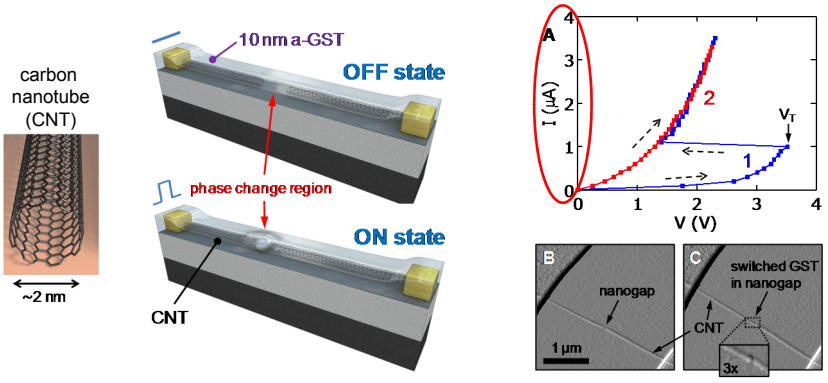
switching induced by Joule heating



Kolobov *et al.* Nature Materials (2004)
Lee *et al.* Nature Nano (2007), Chen and Pop IEEE-TED (2009)

Phase-Change Memory with CNT Electrodes

F. Xiong, A. Liao, D. Estrada, E. Pop, *Science* 332, 568 (2011)

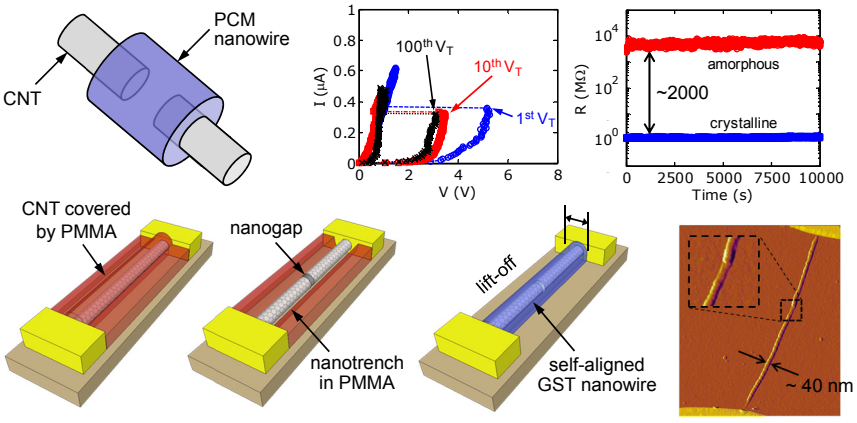


- Key idea: CNTs are smallest possible electrodes (1-2 nm diameter)
- Use CNT to contact sub-10 nm bits of phase-change material
- Switching at **~100x lower power** than conventional PCM!

also see. J. Liang, H.-S.P. Wong, et al., *IEEE-TED* (2012)

Self-Aligned Nanotube-Nanowire Devices

F. Xiong, M.-H. Bae, Y. Dai, A. Liao, A. Behnam, E. Carrion, S. Hong, D. Ielmini, E. Pop, *Nano Lett.* 13, 464 (2013)

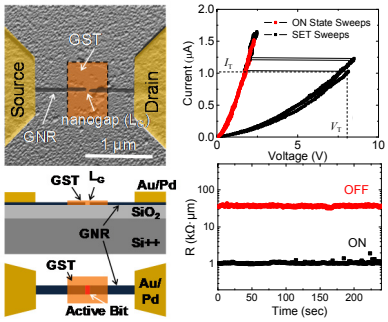


- "Marshmallow" memory bit optimized for **thermal confinement**
- PCM **nanowire self-aligned** with CNT electrodes
- Excellent R_{OFF}/R_{ON} ratio (> 1000) approaches intrinsic GST limits

We Can Also Use Graphene Electrodes

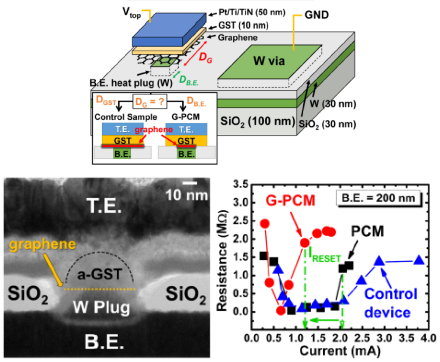
A. Behnam, F. Xiong, E. Pop et al., *Appl. Phys. Letters*. 107, 123508 (2015)
C. Ahn, S.W. Fong, Y. Kim, S. Lee, A. Sood, C. Neumann, K. Goodson, E. Pop, H.-S.P. Wong, *Nano Lett.* 15, 6809 (2015)

Lateral Device



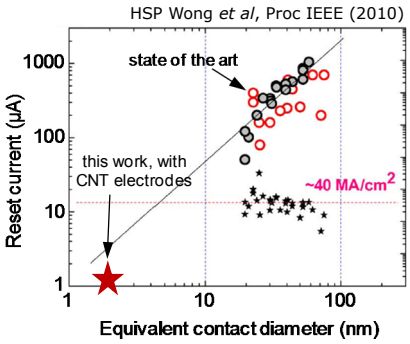
- Graphene "edge" electrode enables sub-10 μA I_{reset}
- Heterogeneous integration challenges

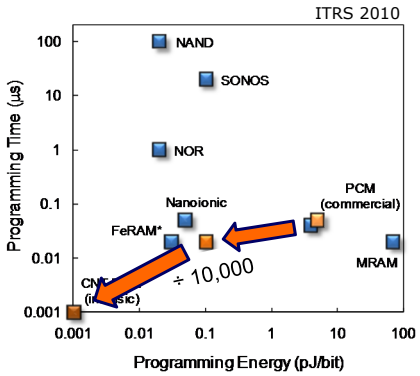
Vertical Device



- Graphene as ultra-thin thermal barrier to block PCM heat loss
- 40% lower I_{reset} than control devices

Where These Results Fit In





- These devices are highly scalable with electrode and bit size
- Lowest power <1 μW, **energy <1 fJ/bit** (with ~1 ns pulse)
- Have **not hit fundamental limits yet** (~10-100x lower… **1.2 aJ/nm³**)*

*review: S. Raoux, F. Xiong, M. Wuttig, E. Pop, *MRS Bull.* (2014)

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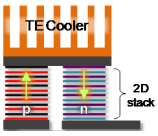
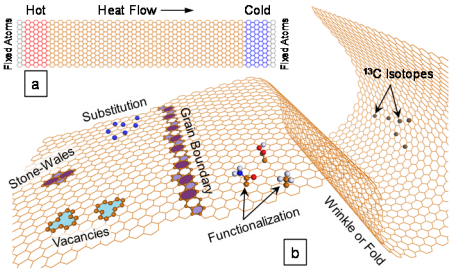


2D Material Thermal Properties

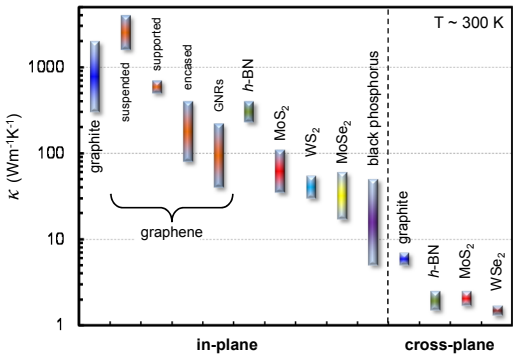
- **Large in-plane** thermal conductivity of graphene, BN (>500 W/m/K)
- **Ultra-low cross-plane** thermal conductivity of layered WSe_2 (<0.1 W/m/K)
  - Lower than plastics and ***comparable to air***
- Huge thermal anisotropy in all layered 2D materials (>10-100x)
- MRS Bulletin review with AFRL:

E. Pop, V. Varshney, A.K. Roy, "Thermal Properties of Graphene: Fundamentals and Applications," *MRS Bulletin* **37**, 1273 (2012)



- **Large thermopower** in TMDs (S ~ 0.5 mV/K) → Thermoelectrics? $ZT = \frac{S^2 \sigma T}{k}$

Thermal Conductivity (κ) of 2D Materials



$$Q'' = -\kappa \nabla T$$

heat flux

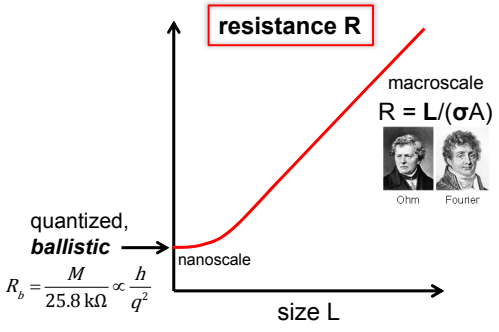
thermal conductivity

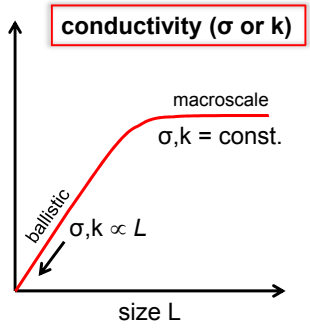
T gradient

- Flexural phonon modes play important role in 2D materials
- **Anisotropy**: $\kappa_{||}$ from ~6 $Wm^{-1}K^{-1}$ (WTe_2) to ~2000 $Wm^{-1}K^{-1}$ (graphene)
  - Cross-plane $\kappa_{\perp}$ is typically very small, e.g. 1 to 6 $Wm^{-1}K^{-1}$

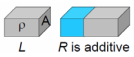
E. Pop, V. Varshney, A. Roy, *MRS Bull.* 37, 1273 (2012); Table courtesy of Z. Li (Pop Lab)

Heat (and Current) Flow in Nanoscale Samples





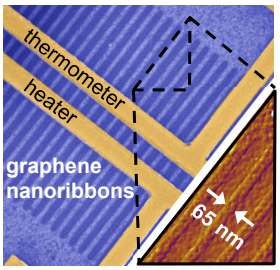
- Macroscale, R is additive: 1 + 1 = 2

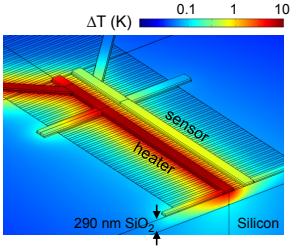


- ***Nanoscale***, R is quantized: 1 + 1 = 1
  - Occurs when system size is comparable to electron or phonon (heat) wavelengths and mean free path (10-100 nm)
  - Both electrical and thermal resistance can be **quasi-ballistic**

Heat Flow in Nanoscale Graphene

M.-H. Bae, Z. Li, Z. Aksamija, P. Martin, F. Xiong, Z.-Y. Ong, I. Knezevic, E. Pop, *Nature Comm.* 4, 1734 (2013)

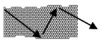




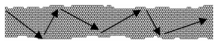
Bulk thermal properties do not apply at <1 μm!

Thermal conductivity **k(T) = f(W,L)** even at room T

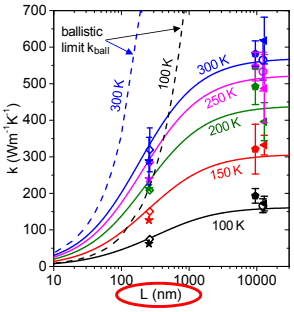
- 35% (quasi-)ballistic heat flow in short devices (λ ~ 100 nm)
- Strong edge scattering in narrow devices

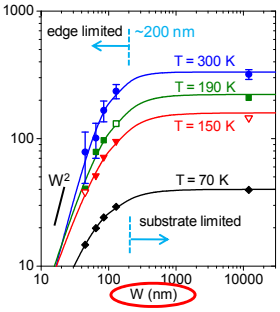


"short" (quasi-ballistic)



"long" (diffusive + edges)



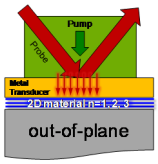


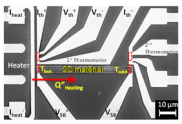
Looking Ahead: Future Opportunities

collab: E. Reed, K. Goodson, K. Saraswat, H.-S.P. Wong, Y. Cui

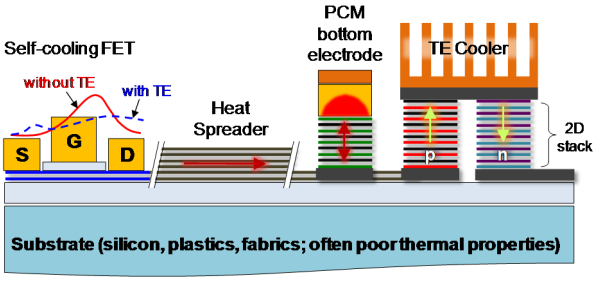
Could we:

- Exploit **anisotropy** for routing heat? (thermal diode)
- Separate thermal and electrical flow? (thermal transistor)
- Design electronics with **built-in thermoelectric cooling**?
- Achieve transparent heat spreaders and flexible thermoelectrics?





in-plane



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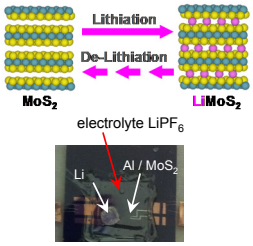
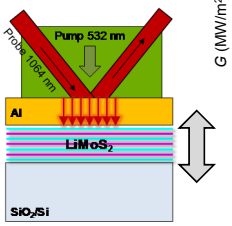
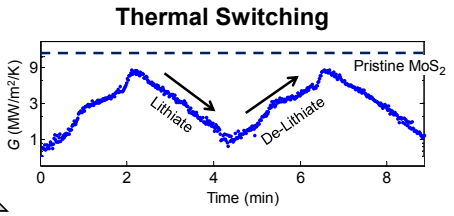
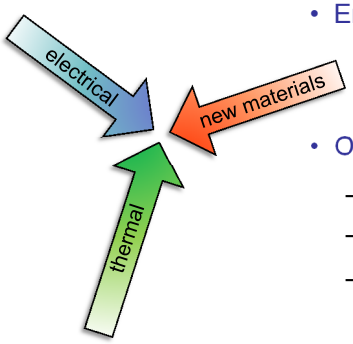






A. Sood, F. Xiong, […], E. Pop, *Spring MRS* (2015)

Summary



- Moore's Law ~10x → slowing down
- Energy scaling & harvesting ~10^4x → exciting

- Opportunity for convergence of:
  - Novel nanomaterials
  - Low power devices
  - Anisotropy, ballistic, thermoelectric

- Understand fundamental limits
- Future opportunities

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