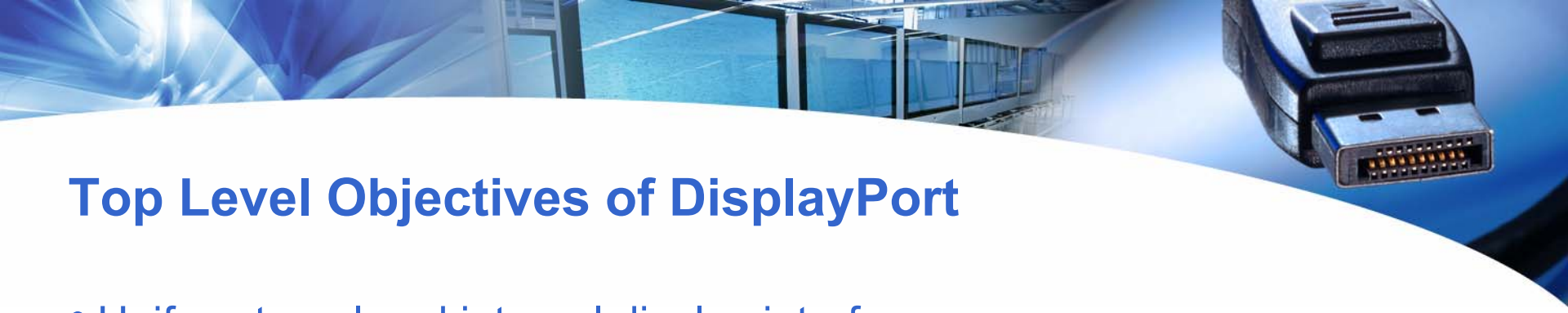
DisplayPort Ver.1.0 and Beyond

Alan Kobayashi, Director of Architecture and Strategy, Genesis Microchip

Do we need another interface?



Top Level Objectives of DisplayPort

- Unify external and internal display interfaces
- Provide scalable performance in terms of resolution, color depth, and refresh rate over fewer wires to support emerging display needs
- Provide a future foundation for new display usages
- Provide a small, user friendly external connector
- Accelerate deployment of protected digital outputs on PCs
- Enable a digital display connection as a viable alternative to VGA

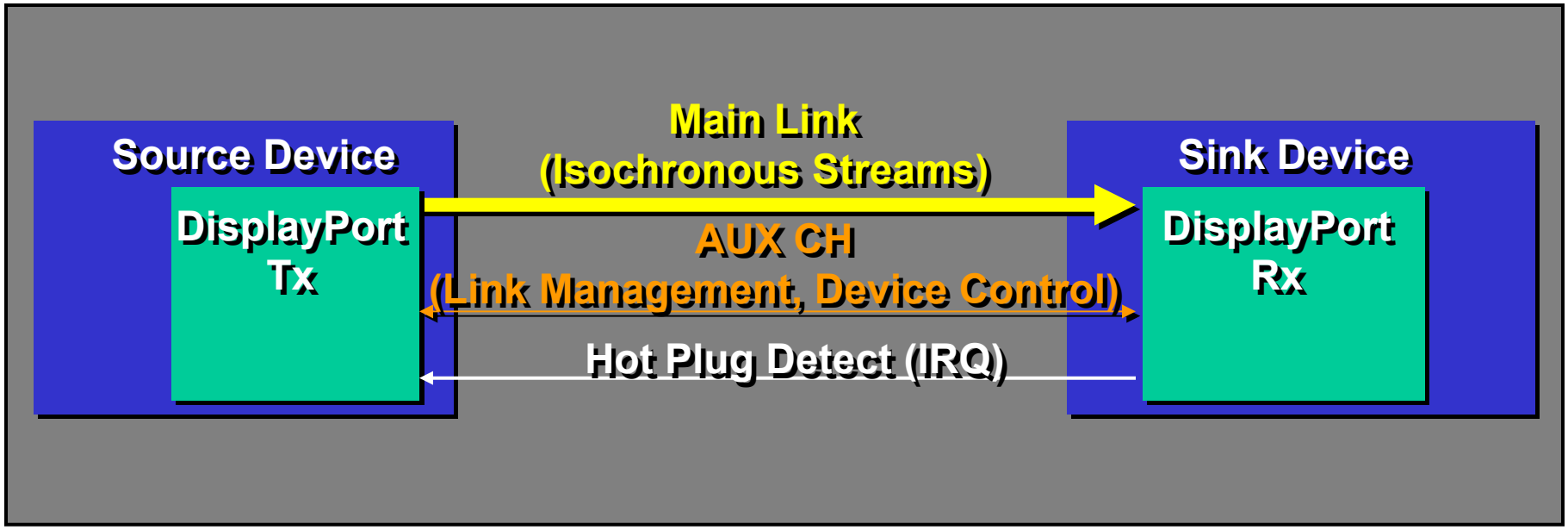
Open industry standard proposed through VESA

Goal: To provide cost-effective, scalable industry standard to consolidate external (box-to-box) & internal (LCD panel) display connections

- Open Standard
  - Administered by VESA, an independent standards body
  - Adoption open to non-VESA members
  - Sustainable standard: future versions/enhancements planned
- Complete Transparency
  - Future modifications to specification done through a transparent process
  - Any VESA member can suggest improvements and vote on future specifications
  - Changes are visible to and influenced by members
- No restrictions on field-of-use

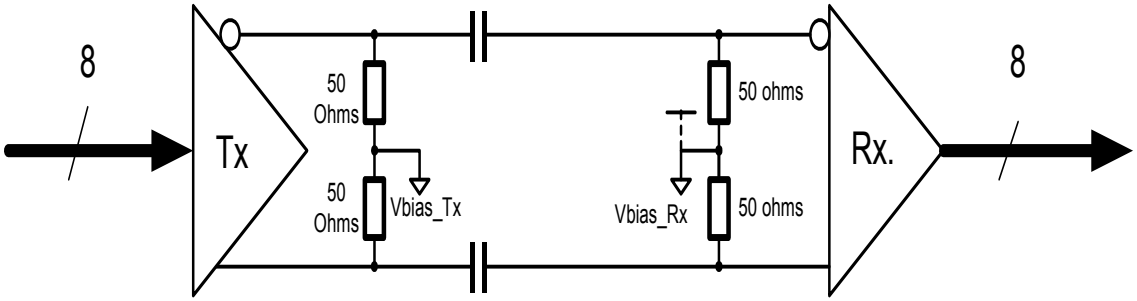
Structure of DisplayPort

- Main Link
  - High-bandwidth, low-latency, unidirectional
  - Isochronous stream transport
- AUX CH (Auxiliary Channel)
  - Consistent-bandwidth, low-latency, bi-directional
  - Main Link management, Device control (EDID, MCCS)



Structure of Main Link

- Consists of AC-coupled, doubly terminated differential pairs (lanes)
  - AC-coupled to facilitate semiconductor process migration
  - 0.35 um to 0.065um (and below)



- Link rate: Either 2.7Gbps or 1.62Gbps per lane
  - De-coupled from Pixel Rate
  - Depends on Tx/Rx capability and Channel quality

Structure of Main Link *(continued)*

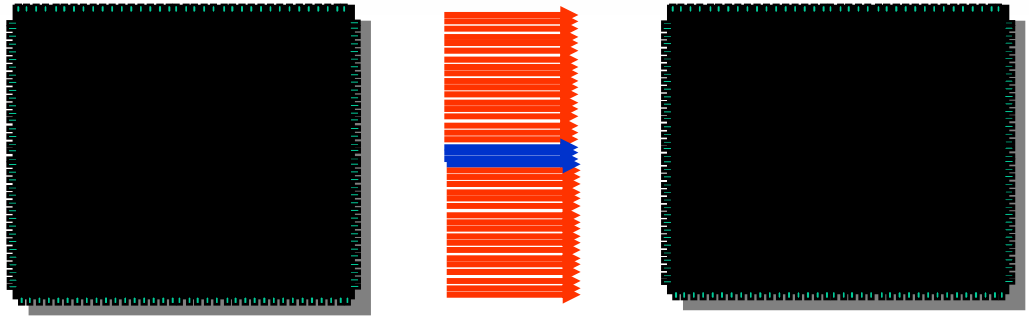
- Number of lanes: 1, 2, or 4 lanes
  - De-coupled from Pixel Bit Depth
    - » Supports 6, 8, 10, 12, and 16 bpc (bits per component), in RGB, YCbCr444/422 colorimetry formats in Ver.1.0
    - » Easily extended to any required bit depth or colorimetry
  - All lanes carry data (no dedicated clock lane)
    - » Clock extracted from ANSI8B/10B encoded data stream
    - » No reference clock required in the receiver
    - » Data symbols scrambled for EMI reduction
    - » Optional support of spread-spectrum for further EMI reduction
  - Lane count requirement
    - » Source and Sink devices allowed to support minimum number of lanes required for their needs
    - » External cable-connector assembly required to support 4 lanes

Main Link Bandwidth

- Available application bandwidth
  - 1 lane = 270Mbytes per sec
  - 2 lanes = 540Mbytes per sec
  - 4 lanes = 1080Mbytes per sec
    - » 2.2x of single-link DVI/HDMI with the same number of wires.
- Freely trade pixel depth with resolution and frame rate
  - Over 4 lanes
    - » 12-bpc YCbCr444 (36 bpp), 1920x1080p @ 96Hz
    - » 12-bpc YCbCr422 (24 bpp), 1920x1080p @ 120Hz
    - » 12-bpc RGB (36 bpp), 4096x2160 @ 24 Hz (4k digital cinema)
    - » 10-bpc RGB (30 bpp), 2560x1600 @ 60Hz
    - » 8-bpc RGB (24bpp), 2560x2048 @ 60 Hz
  - Over 1 lane
    - » 8-bpc YCbCr (24 bpp), 1920x1080i @60Hz
    - » 6-bpc RGB (18 bpp), 1680x1050 @60Hz

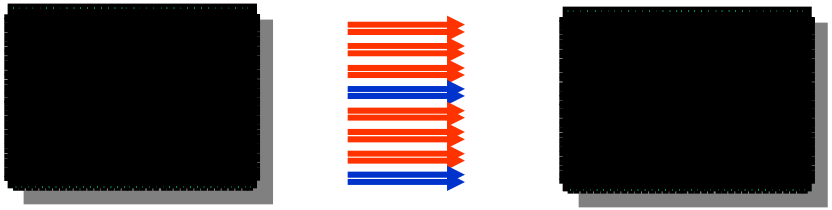
Pin-Count Reduction

TTL Interface



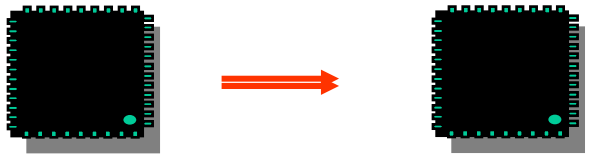
36 Data, 3 control lines,1 clock
Total 40 signals

LVDS Interface



6 Data pair, 2 clock pair
Total 16 signals

DisplayPort Interface

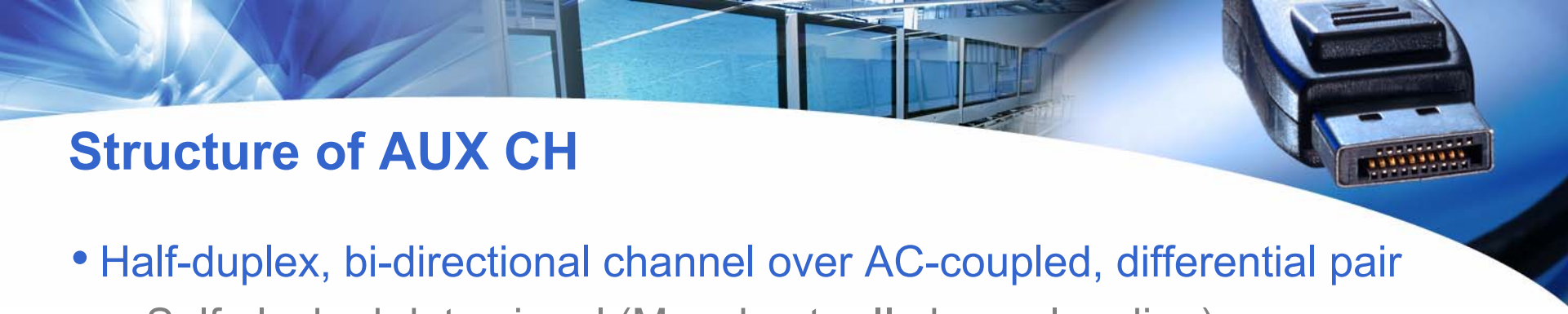


1 Data pair, 0 clock pair
Total 2 signals

Driving a WSXGA+ panel (1680x1050 resolution) 6-bits per color (18 bits per pixel)

Silicon Process Dependency

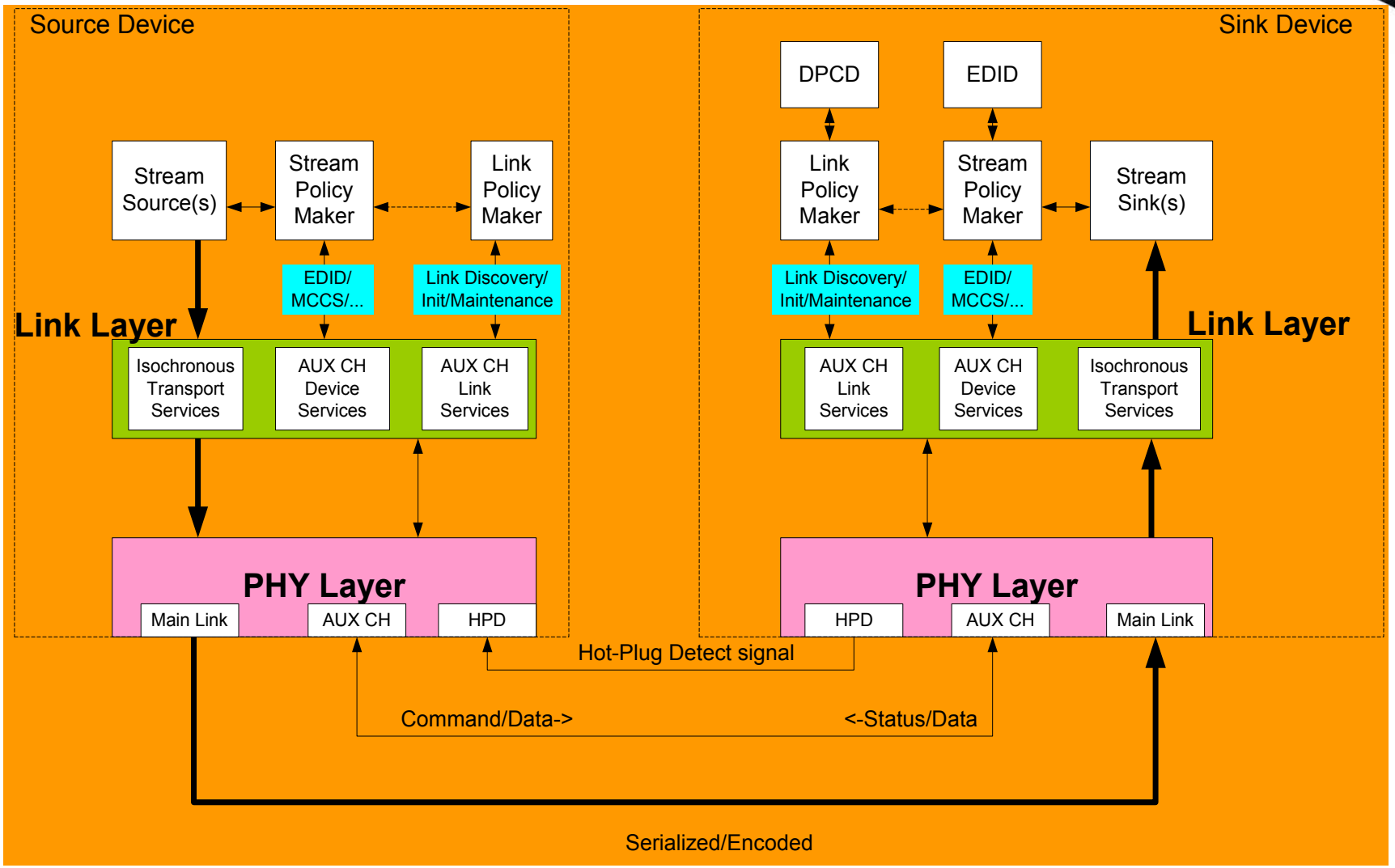
- 2.7 Gbps link rate expected to require 0.18 um (or less) technology
- 1.62 Gbps link rate feasible for 0.25-/0.35-um technology
  - Allows low cost panel electronics for standard display sizes
- Over 1 lane at 1.62 Gbps
  - 6bpc RGB (18bpp), 1280x800 @ 60 Hz
- Over 2 lanes at 1.62 Gbps
  - 6bpc RGB (18bpp), 1600x1200 or 1680x1050 @ 60 Hz
  - 8bpc RGB (24bpp), 1400x1050 @ 60 Hz
- Over 4 lanes at 1.62 Gbps
  - 6bpc RGB (18bpp), 2560x1600 @ 60 Hz
  - 8bpc RGB (24bpp), 2048x1536 @ 60 Hz



Structure of AUX CH

- Half-duplex, bi-directional channel over AC-coupled, differential pair
  - Self-clocked data signal (Manchester II channel coding)
  - Source = Master, Sink = Slave
    - » Sink sends IRQ (Interrupt Request) via HPD line
- Consistent bit rate over various cable lengths (15 m and beyond)
  - 1Mbits/sec
- Minimal latency
  - Maximum transaction period < 500us
    - » Burst data size equal to or less than 16 Bytes
    - » Prevents one AUX CH application from starving others
- Easy interoperation with DDC legacy
  - Simple protocol bridging to DDC

Layered and Modular Architecture



DisplayPort Configuration Data (DPCD)

- Link capability, Link configuration, and Link/Sink status
  - Separate from DDC address space (EDID, DDC/CI, etc)

- Works in parallel with EDID & DDC/CI – No conflict
  - DPCD for describing capability and controlling DP Rx only
  - EDID for describing capability of the sink device
    - » Video and sound rendering ability
  - DDC/CI for controlling sink device
    - » But not for controlling DP RX in Sink device

Link Layer

- Isochronous Transport Services
  - Maps stream data into Main Link lanes
    - » Facilitates the support of various lane count

- Link and Device Services
  - Link management
  - Device control

Control Symbols for Stream Framing

- "K codes" of ANSI8B/10B code set assigned
  - BS (Blank Start), BE (Blank End)
  - FS (Fill Start), FE (Fill End)
  - SS (Secondary-data packet Start), SE (Secondary-data packet End)

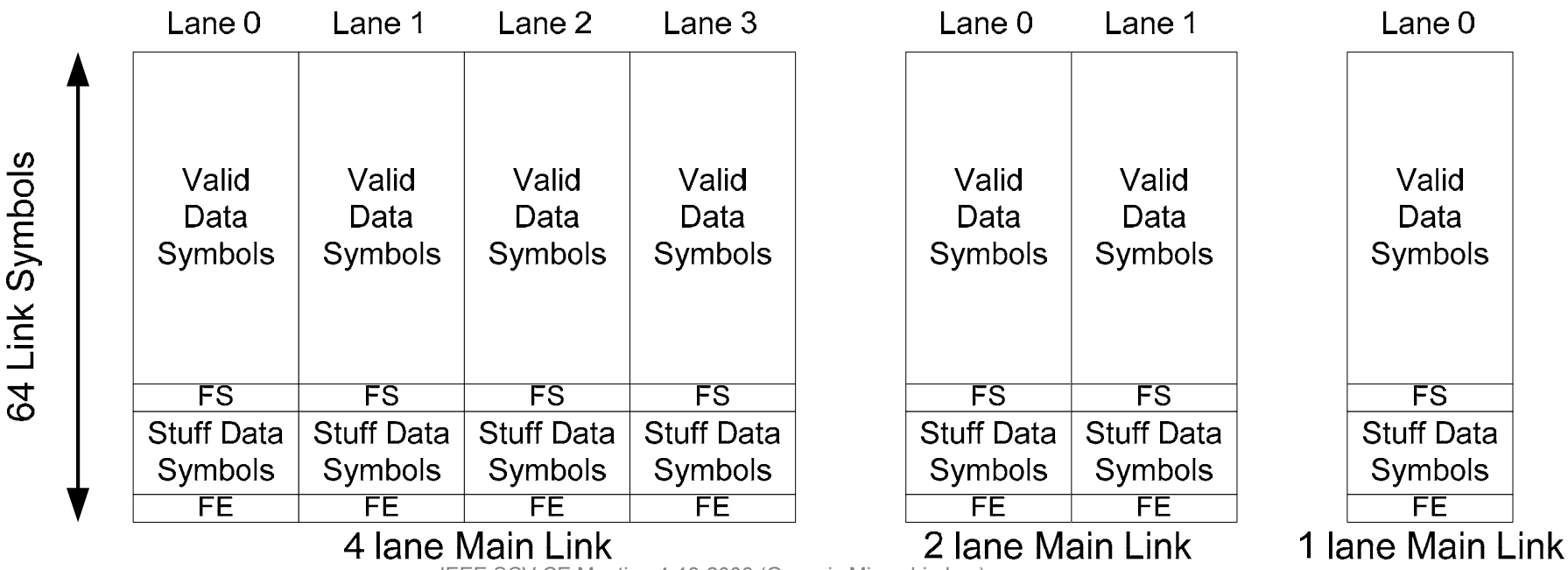
Pixel Steering

Number of Lanes	Pixel Steering (N>=0)
4	Pixel 4N to Lane 0 Pixel 4N+1 to Lane 1 Pixel 4N+2 to Lane 2 Pixel 4N+3 to Lane 3
2	Pixel 2N to Lane 0 Pixel 2N+1 to Lane 1
1	All pixels to Lane 0

- Pixel bit depth (bits per pixel) > Link Symbol size (8 bits per symbol)
  - » Each link symbol carries part of a pixel
- 1st partial pixels immediately follow BE on all lanes

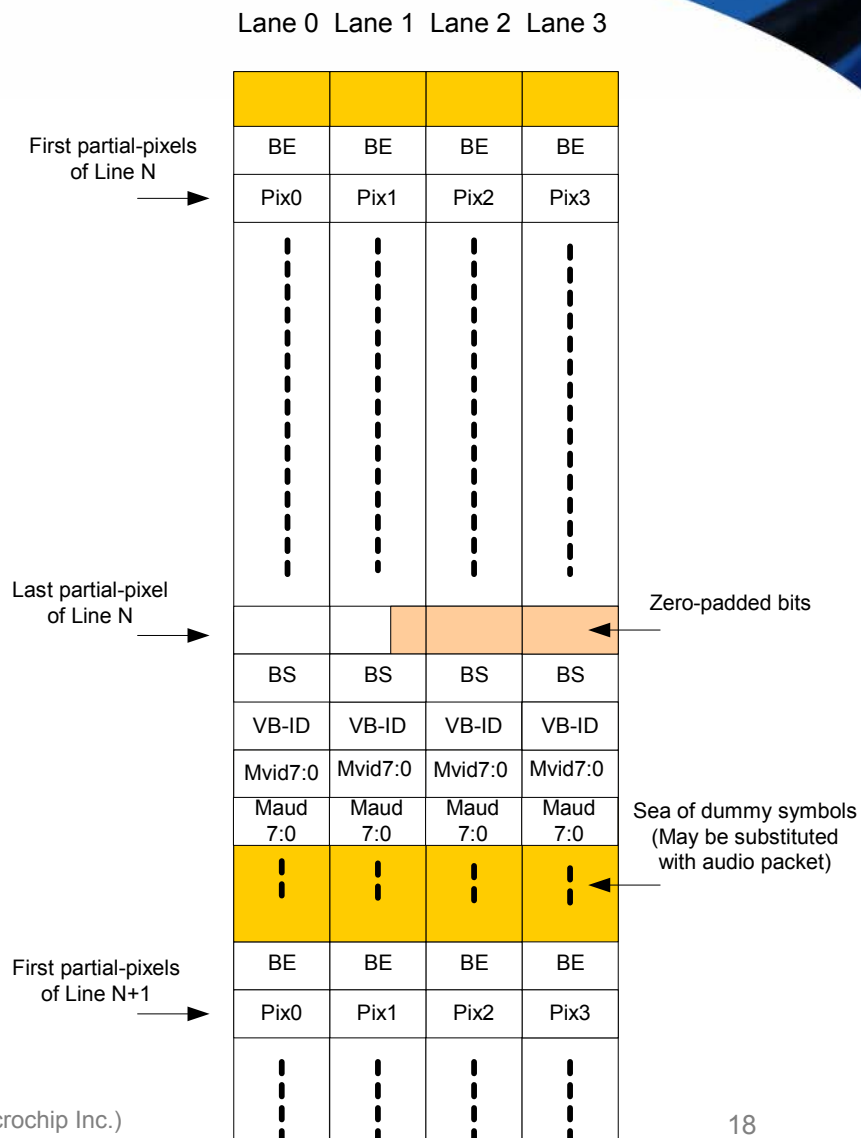
Data Packing

- Data Packing and Symbol Stuffing
  - Packed into Micro-Packet (called “Transfer Unit”, 64 symbols long per lane)
    - » Length fixed to limit size of buffers needed
  - Ratio of Valid Data to Stuff Data related to ratio between packed data stream rate and link rate
  - Terminated at the end of the active horizontal video period
    - » Marked by BS insertion on all lanes



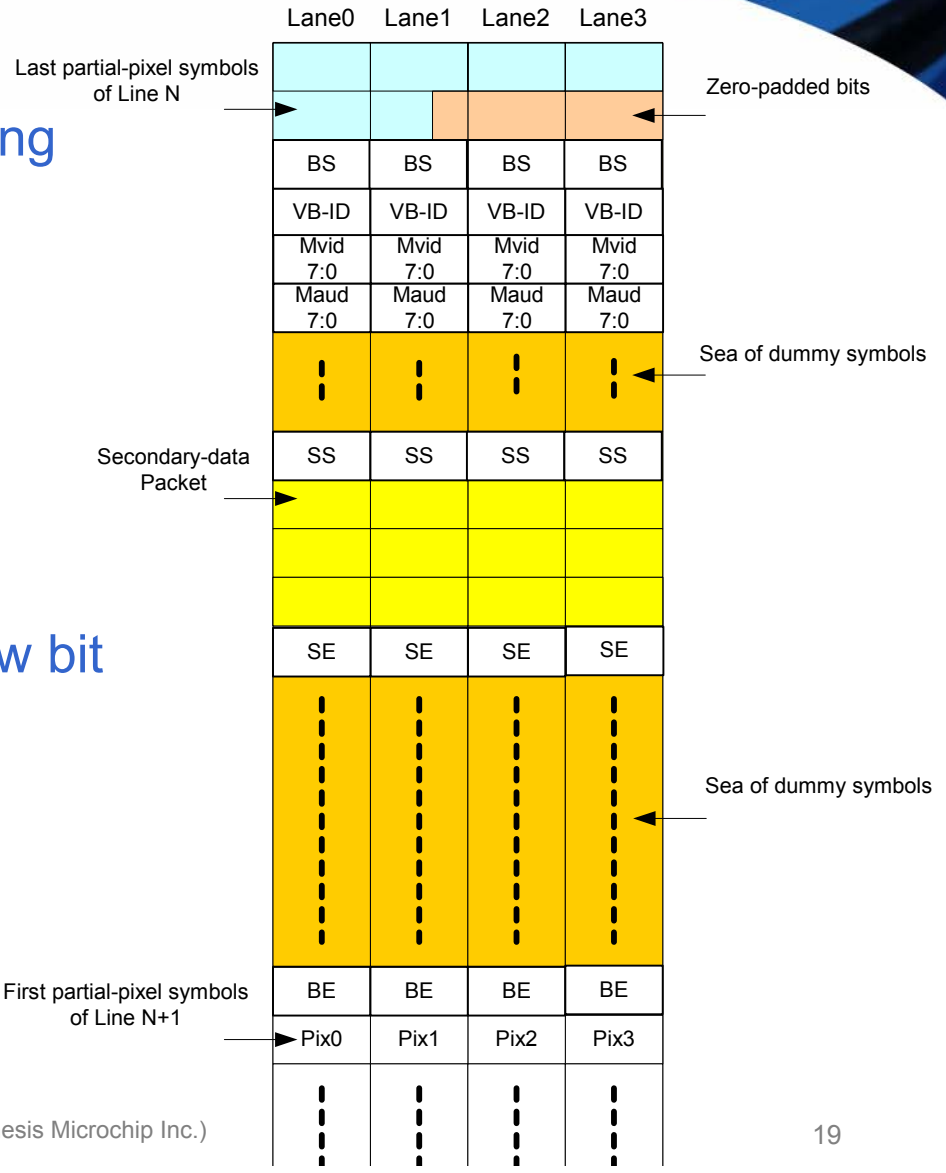
Main Video Stream Framing

- Each video raster line framed by BE and BS
- White "---" area full of 64-Byte-per-lane micro-packets
- Each line followed by stream attribute data
  - VB-ID
    - » VBlank flag
    - » Field flag
    - » Interlace flag
    - » Video "Mute"
    - » Audio Mute
  - Video clock recovery (Mvid)
  - Audio clock recovery (Maud)
  - Mvid and Maud for use when stream rate and link rate not a static fractional relationship
- Redundancy for protection



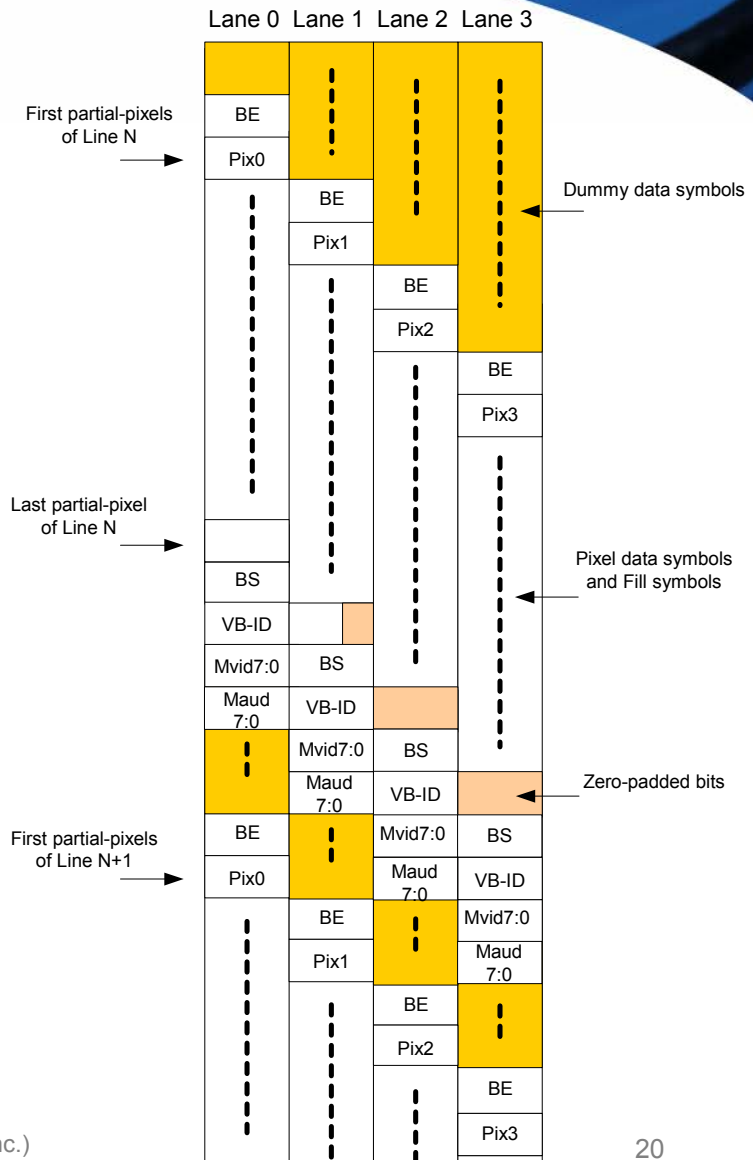
Secondary-data Packet Stream Framing

- Secondary streams are optional
- Secondary streams sent in H blanking framed by SS and SE
  - Replace “dummy” symbols
- Secondary stream types
  - Audio data
  - Audio clock recovery
  - InfoFrames (CEA 861B)
  - Extensible for future
- Protected by ECC to ensure very low bit error rates
  - $<10^{-12}$



Inter-Lane Skewing

- 2 or 4 lanes always skewed by 2 link symbol clocks
- Provides extra robustness to interference
- For 1 lane case additional redundancy added by repetition of control flags
- All controls always sent 4 times no matter how many lanes



Link and Device Services for Plug & Play

- Establishes the link upon Hot-Plug Detection
  - Transmitter reads DPCD of Receiver
  - Link configured through Link Training
    - » Proper number of lanes enabled at proper link rate for a given application with proper equalization level
  - Link status monitored
    - » Via AUX CH handshake
    - » “Close-loop” operation enhances the robustness and interoperability
  - Link stays active and stable during stream timing change
    - » Glitch-free display during timing change
- Transparently supports EDID and DDC/CI commands via AUX CH
  - Also supports remote-control pass through

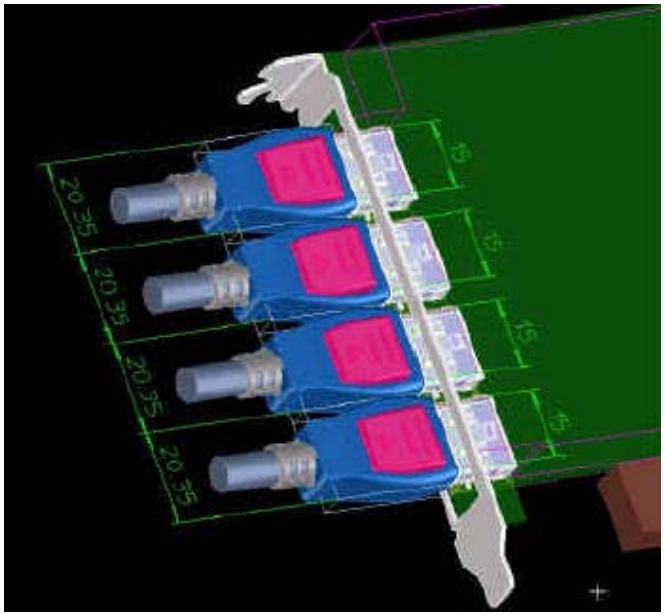
Physical Layer

- **Logical sub-block**
  - Scrambling/de-scrambling of data for Main Link
  - Encoding/Decoding
    - » ANSI8B/10B for Main Link
    - » Manchester II for AUX CH

- Electrical sub-block
  - SERDES (Serialization/De-serialization)
  - Differential current driving/receiving
  - Pre-emphasis/equalization for Main Link

Box-to-box Connectors

- **20-pin connector**
  - Symmetrical between Source and Sink
  - Compact
    - » Four connectors fit in PCI-e card bracket
    - » Fits in the back of ultra-slim notebook PC
  - DP_PWR pin
    - » Power (1.0W or larger) provided by Source for powering a dongle (repeater, interface converter, etc.)
    - » +5 ~ +12V, 500mA maximum
  - Optional latch
    - » Prevents “cable fall-off”

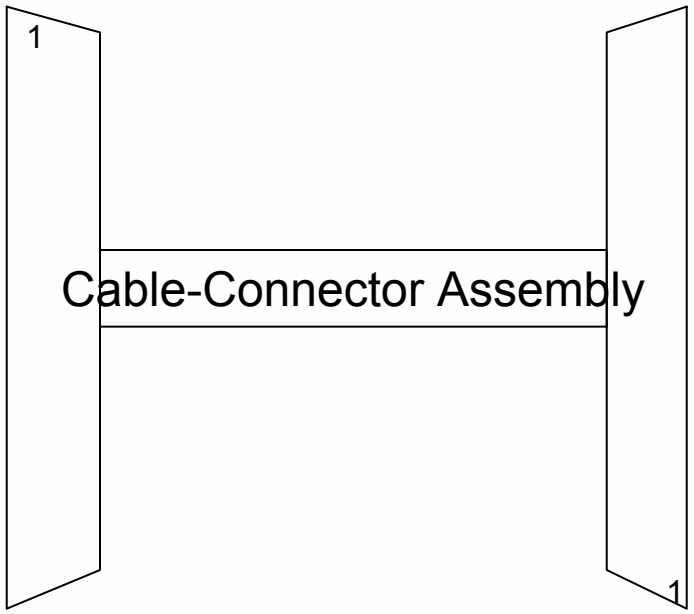


Box-to-box Connector Pin-out

- Same Tx and Rx IC pin-outs feasible both for box-to-box and embedded, even on 2-layer PCB's
- Optimized for signal integrity of Main Link
  - No vias for Main Link signal routing on PCB
  - Minimal Near-End Noise from AUX CH

Tx Connector

Pin Name	Pin #
ML_L0p	1
GND	2
ML_L0n	3
ML_L1p	4
GND	5
ML_L1n	6
ML_L2p	7
GND	8
ML_L2n	9
ML_L3p	10
GND	11
ML_L3n	12
GND	13
GND	14
AUX_CHp	15
GND	16
AUX_CHn	17
HPD	18
Pwr_Rtn	19
DP_PWR	20

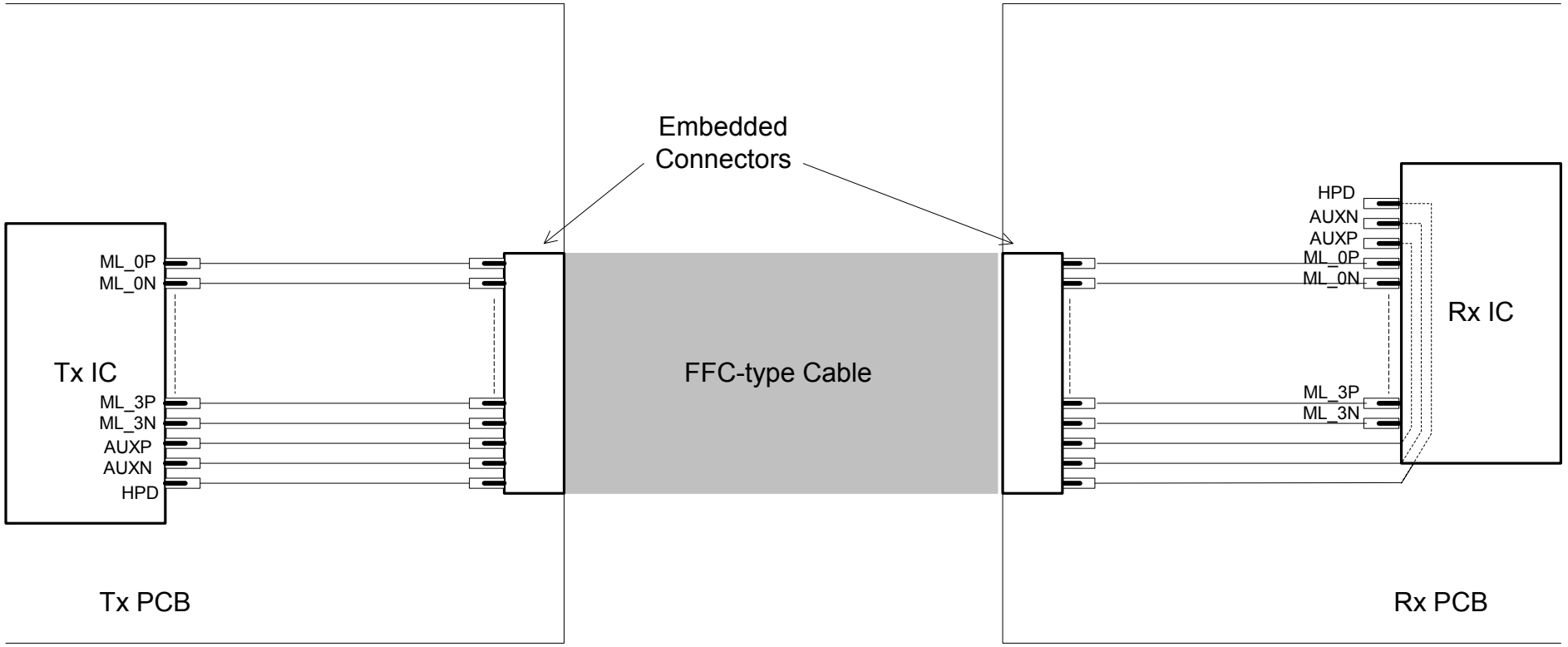


Rx Connector

Pin#	Pin Name
20	DP_PWR
19	Pwr_Rtn
18	HPD
17	AUX_CHn
16	GND
15	AUX_CHp
14	GND
13	GND
12	ML_L0p
11	GND
10	ML_L0n
9	ML_L1p
8	GND
7	ML_L1n
6	ML_L2p
5	GND
4	ML_L2n
3	ML_L3p
2	GND
1	ML_L3n

Embedded Connectivity

- Supports flat-cable without compromising the signal integrity of Main Link



DPCP (DisplayPort Content Protection)

- Optional content protection developed by Philips
- 128-bit security
  - High-speed cipher backed by 128-bit AES
  - ECC (Elliptic Curve Cryptography) Authentication
- Built-in SRM system
- Branch Device (also known as Repeater) support built-in
  - Support required, not optional

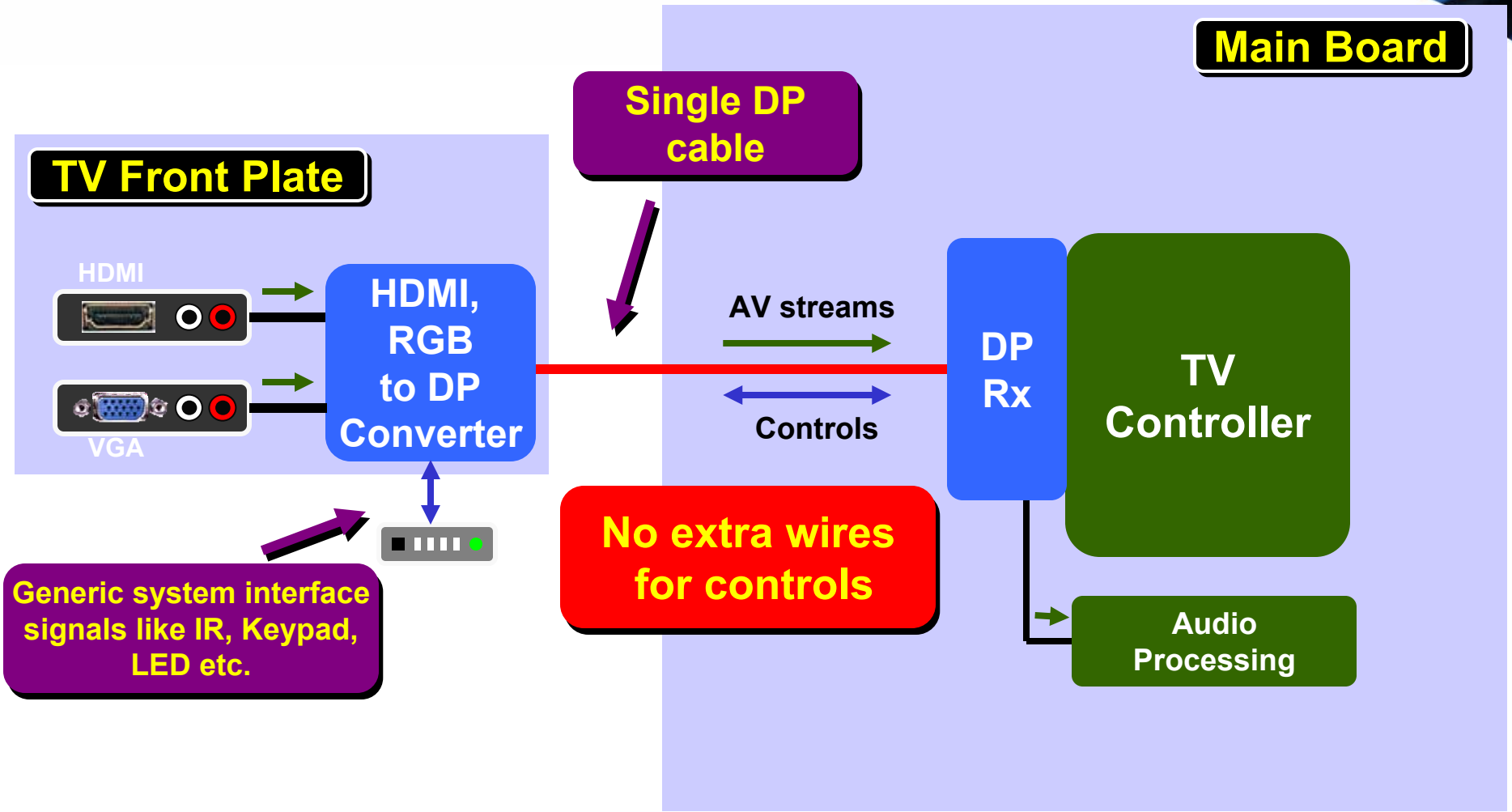
Bandwidth Extensibility

- Layered architecture for seamless bandwidth extension
  - Allows DisplayPort to replace Physical Layer in the future while the Link Layer and above stays intact
- Gen2 (circa 2008 ~ 2009) anticipated to provide for 2x of Gen1 bandwidth per lane
  - Connector specifications defined with Gen2 extension in mind
  - Backward compatibility with Gen1 maintained through Link Training/Configuration
  - Uncompressed bandwidths well beyond current Digital Cinema (DCI)
    - » 16 bpc RGB (48bpp), 2560x2048 @ 60 Hz
    - » 12 bpc RGB (36bpp), 4096x2160 @ 48 Hz
    - » 10 bpc RGB (30bpp), 4096x2160 @ 60 Hz
    - » 8-bpc RGB (24bpp), 3840x2400 @ 60 Hz
- Major upgrade of AUX CH bandwidth also feasible

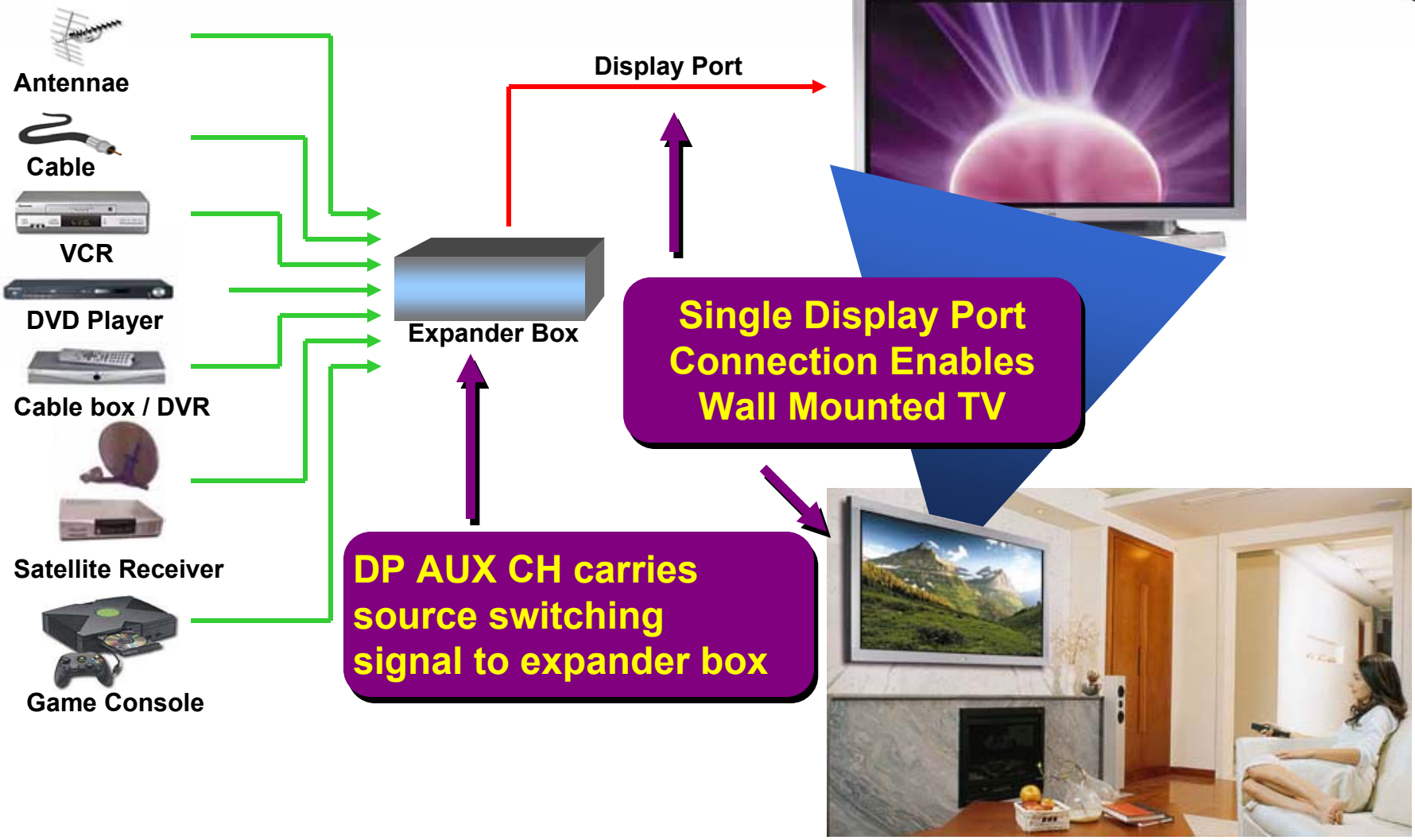
Feature Extensibility

- Micro-Packet architecture enables transport of multiple A/V streams and other data types
  - PiP and Split Screen streams over a single cable
    - » Up to 6x 1080i and 3x 1080p streams on a single connector, enabling daisy chaining in the future
  - Inclusion of meta-data packets, such as PSIP
- High Speed, robust AUX CH allows for:
  - Bi-directional audio – Microphone, audio chat, VoIP
  - Low BW video backchannel for webcam applications

Front-Plate Enhancement

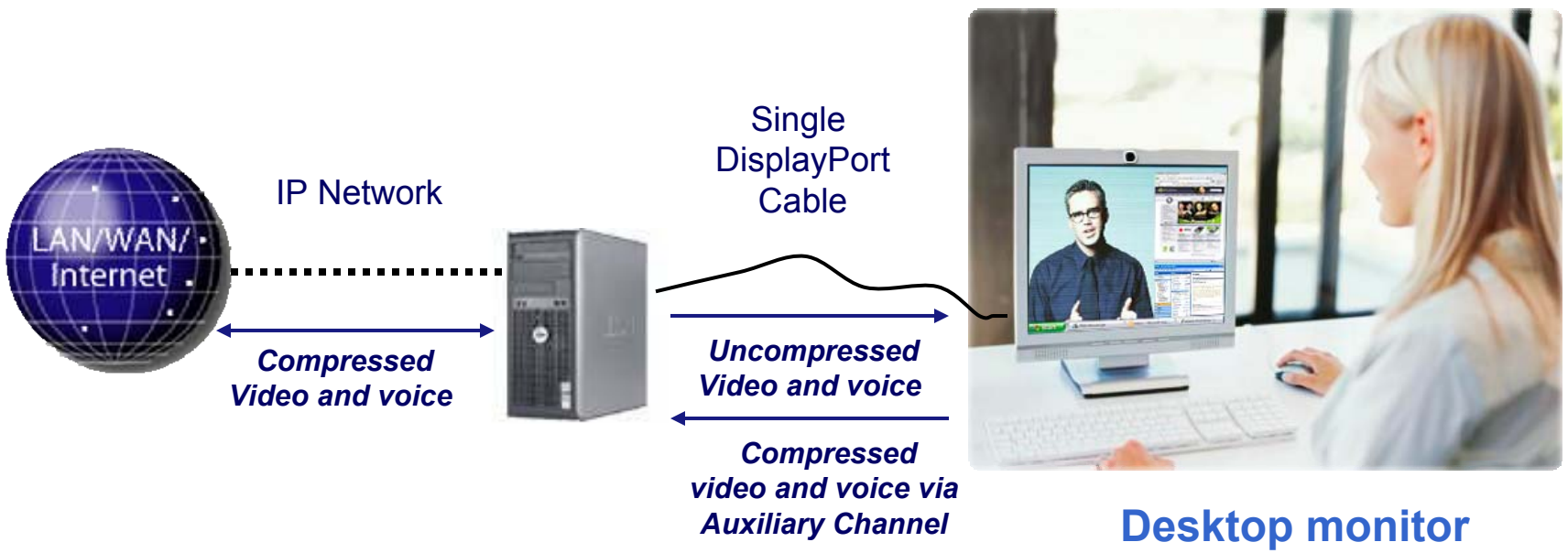


Future TV Interconnect

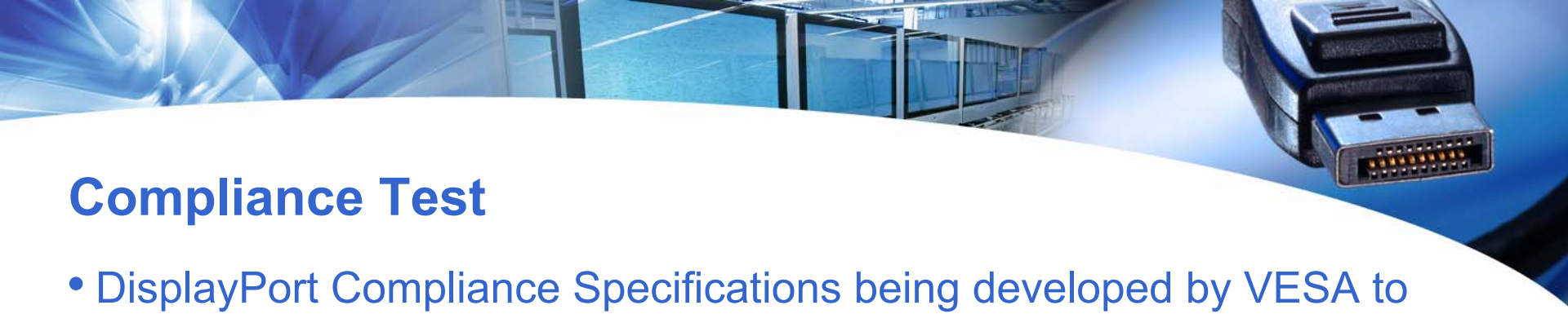


AUX CH Extensibility for Future Applications

Real-time communications may be accommodated over the same physical interface



Desktop monitor with integrated video camera and microphone



Compliance Test

- DisplayPort Compliance Specifications being developed by VESA to ensure interoperability
  - Source, Sink, Cables, and Branch devices
  - Physical Layer, Link Layer & Content Protection
  - Use of independent test centers for compliance testing and certification

DisplayPort Ver.1.0 Time-line

- VESA adoption vote concludes on 4-28-2006
- Compliance Test Program development completion in Q3 2006
- DPCP Specification Ver.1.0 and Licensing Agreement to be available in Q2 2006
- First silicon availability in 2H 2006
- First PC/monitor launch in 1H 2007
- Fist CE product (for internal connection) in 1H 2007

Summary

- Open mind to an open standard
- Unified internal and external display interface
- Addresses emerging PC requirements
  - Reduces complexity and cost in displays
- Scalable performance in terms of resolution, color depth and refresh rate over fewer wires
- Open standard development through industry participation
- No barriers to adoption by the industry – unrestricted field-of-use
- Extensible

How Can My Company Participate in VESA?

Companies interested in participating in the review of DisplayPort and future extensions are invited to participate in the DisplayPort Task Group within the VESA Display Systems Committee

VESA Contact Info:

Web Site: http://www.vesa.org

Office: Bill Lempesis - bill@vesa.org

DisplayPort Task Group:

Chair: Bruce Montag, Dell, bruce_montag@dell.com

Vice Chair: Bob Myers, HP, bmyers@hp.com

Thank you.

PC Display Landscape Backup Slides

Display Landscape of Today

DisplayPort addresses the need to scale in performance from high-volume, low bandwidth entry PC monitors and notebook panels, up to niche high-end consumer and professional displays via a single transmitter, receiver, and connector.