ASLEEP YET AWARE: NEAR-ZERO POWER RF WAKEUP RECEIVERS WITH AUTOMATIC OFFSET COMPENSATION

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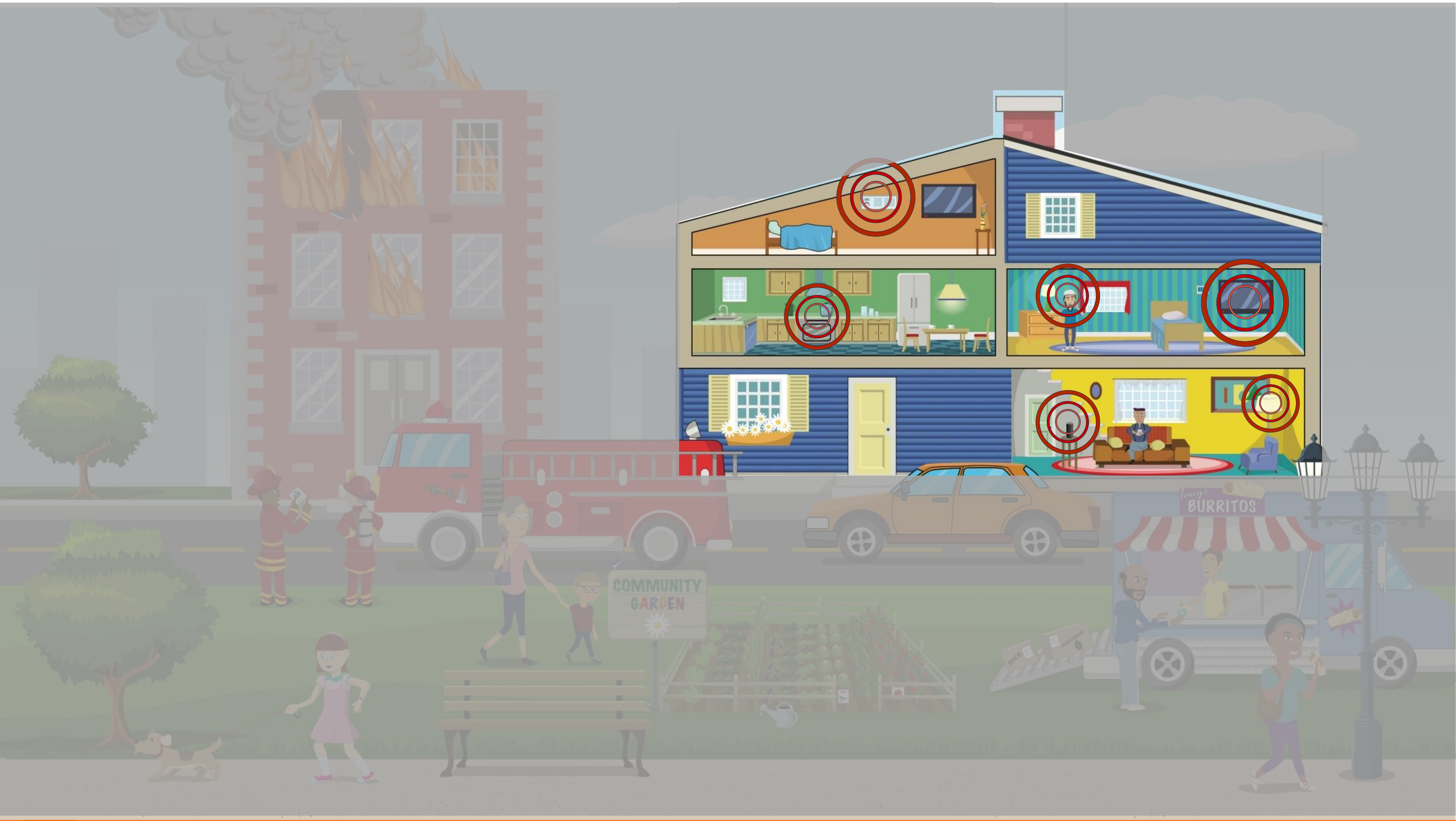
Applications of Near Zero Power Sensors

Applications: Emergency Response

Applications: Smart Homes



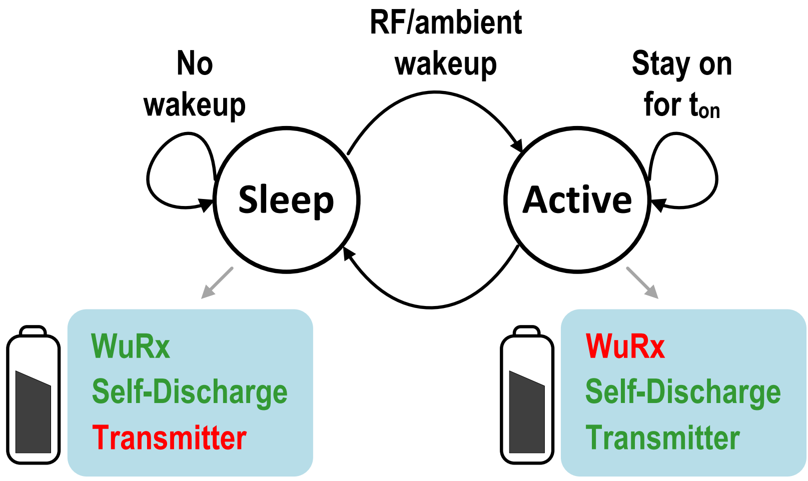
Applications: Community Resource and Personal Health Management

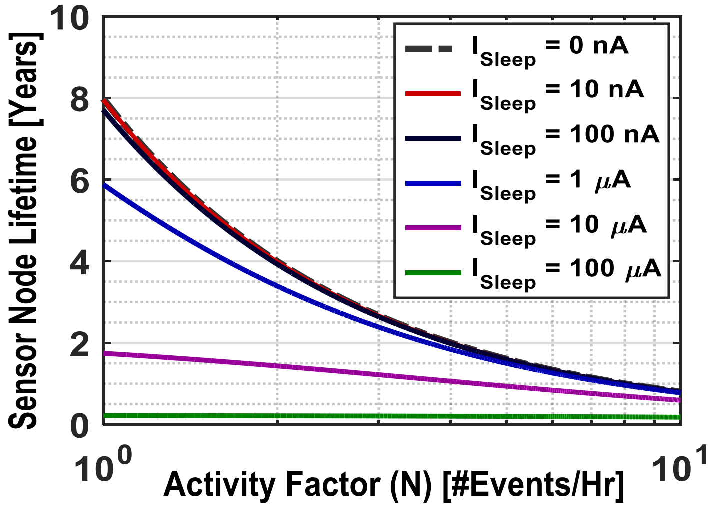
Applications: Inventory Tracking

Applications: Smart Agriculture

Applications: Autonomous Vehicles

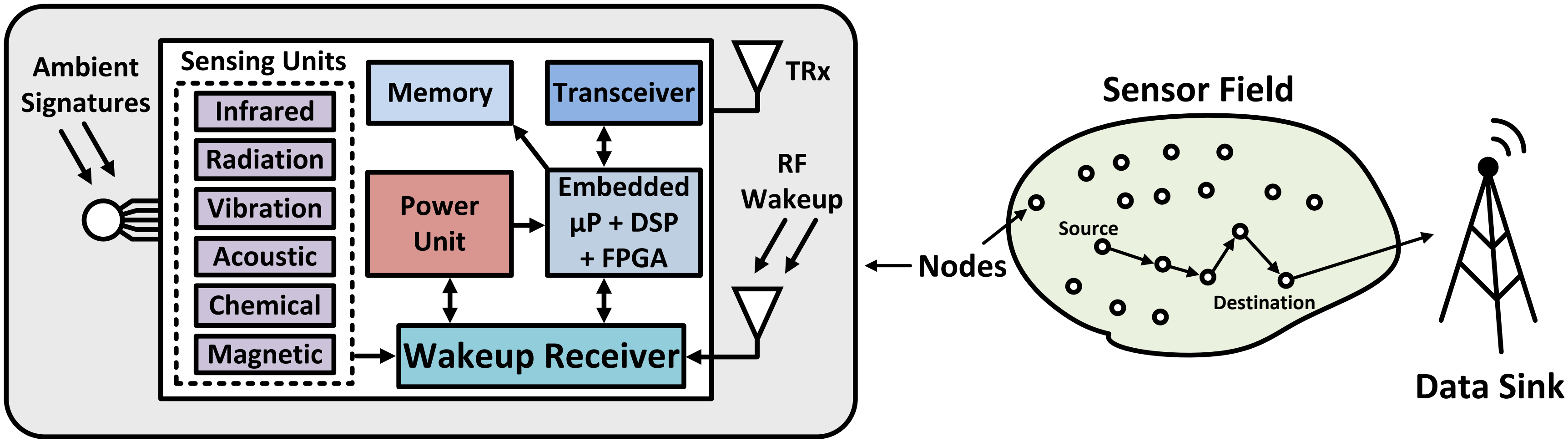
Smart sensor node lifetime





- When considering a sensor node utilizing ~10mW on power life time can be extended by years utilizing nanowatt level WuRx's

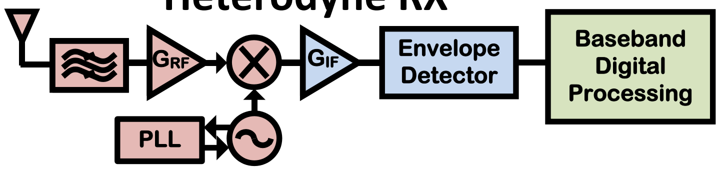
Event-driven smart sensor nodes



- Ubiquitous, persistent real time environmental monitoring
- Operation over extreme time scales and environmental conditions

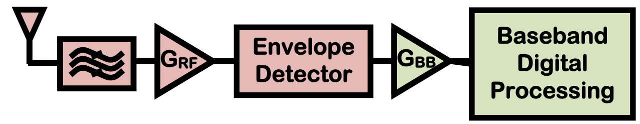
WuRx front-end architectures

Heterodyne RX



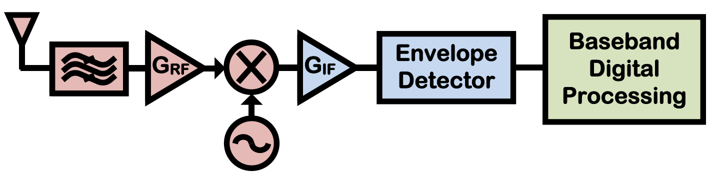
- Traditional radio reciever architecture
- Highest sensitivity
- Highest power

Tuned Front End RX



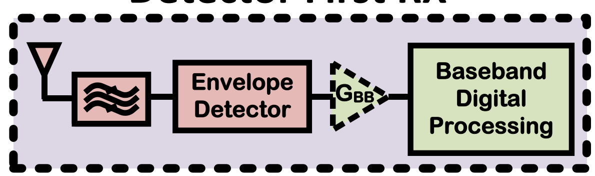
- Input LNA for increased sensitivity
- High sensitivity
- RF LNA required

“Uncertain IF” RX



- Unlocked oscillator into wideband IF
- High sensitivity
- RF Oscillator required, IF gain stages required

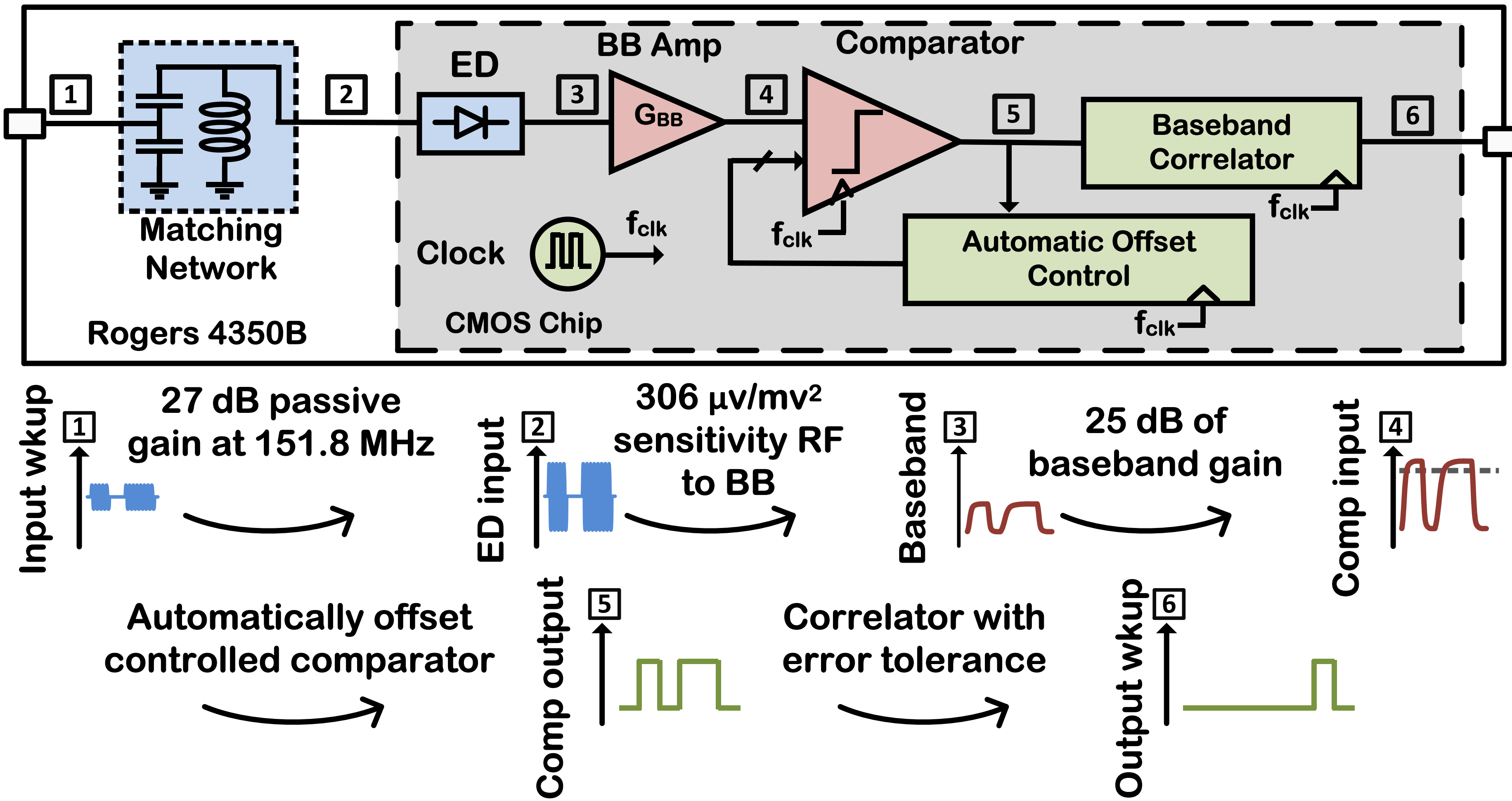
Detector First RX



- Lowest DC Power consumption
- Moderate sensitivity
- No gain required at RF frequencies

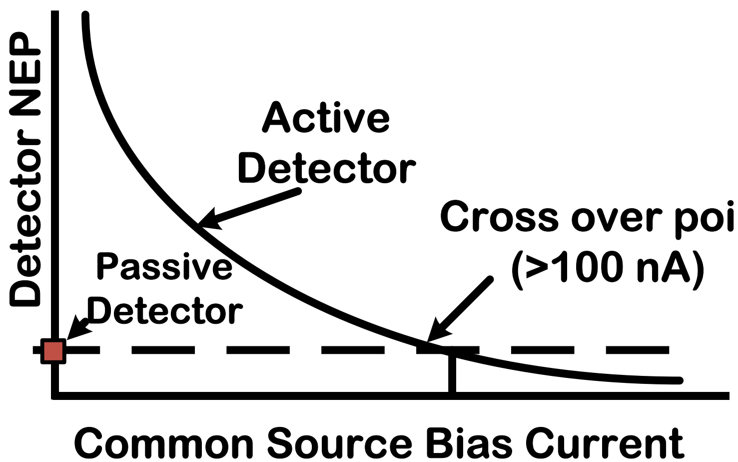
System Architecture

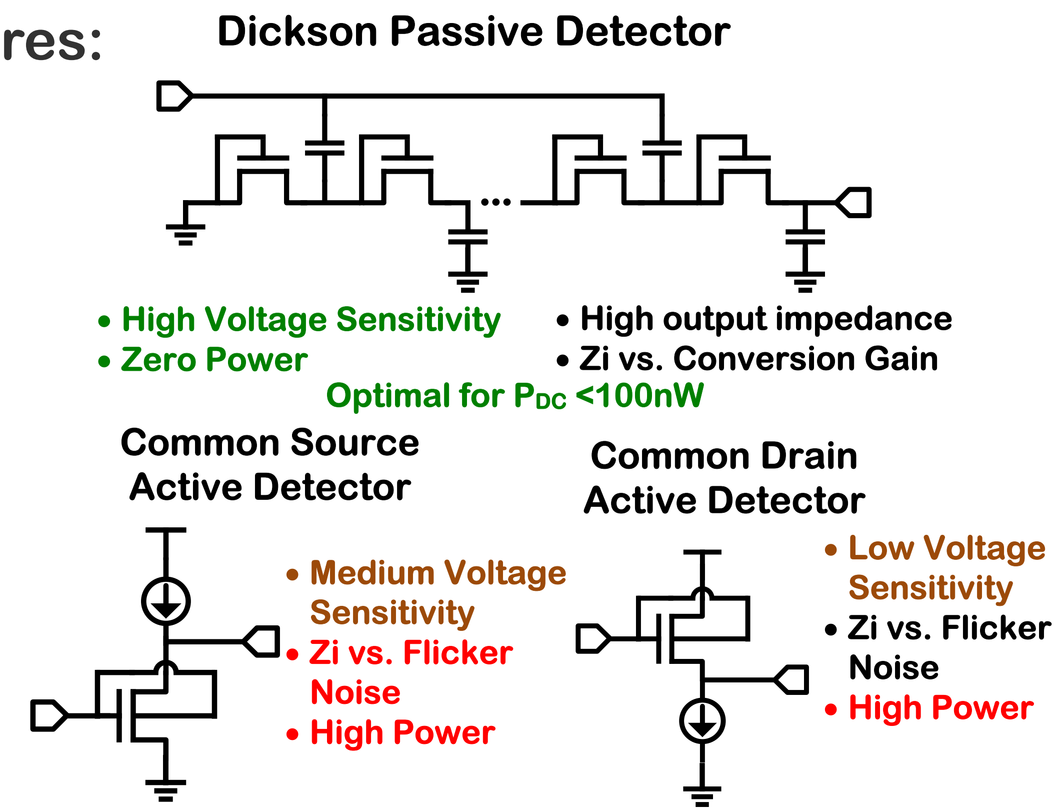
This work: Detector First RX



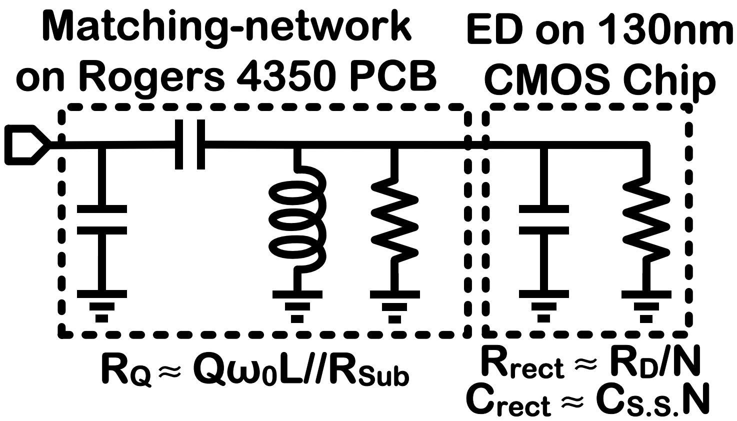
Envelope Detector comparison

- **Optimal RX sensitivity requires:**
  1. High OCVS (V_{DC}/P_{RF})
  2. Low output noise levels
  3. Low bandwidth reception





Matching-network ED codesign



$$SNR_{Out} = \frac{N\mu_D P_{in} R_D R_p}{(R_D + NR_p)\sqrt{4kTNR_D B}}$$

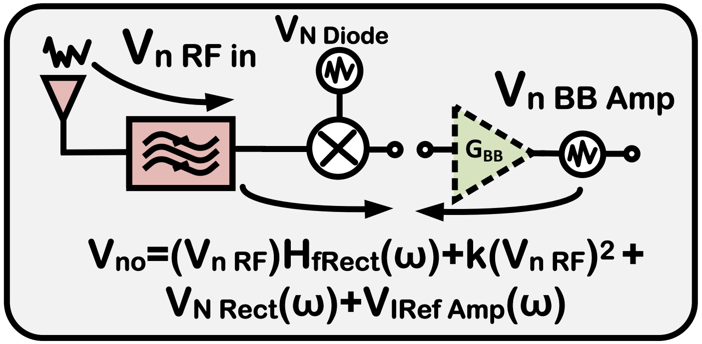
$$SNR_{Opt} \propto k\sqrt{R_p} \qquad N_{opt} = \frac{R_D}{R_p}$$

- For optimal output SNR:
  - $R_{Rect} \approx R_Q$
  - Two independent design variables available
    - R_D ~ DC channel impedance of diode
    - N ~ Number of diodes
- Output SNR is a monotonically increasing function of R_Q
  - Increase Q factor
  - Decrease capacitance

Baseband/Dickson envelope detector codesign

- In order to overcome input referred baseband noise:
  - $V_{nDet} > V_{NAmp}$
- For detector output impedance we find that:
  - $R_{ORect} \approx NR_D$
  - Or that: $R_{ORect} \approx N^2R_Q$
  - Where R_Q is the shunt resistance of RF resonator

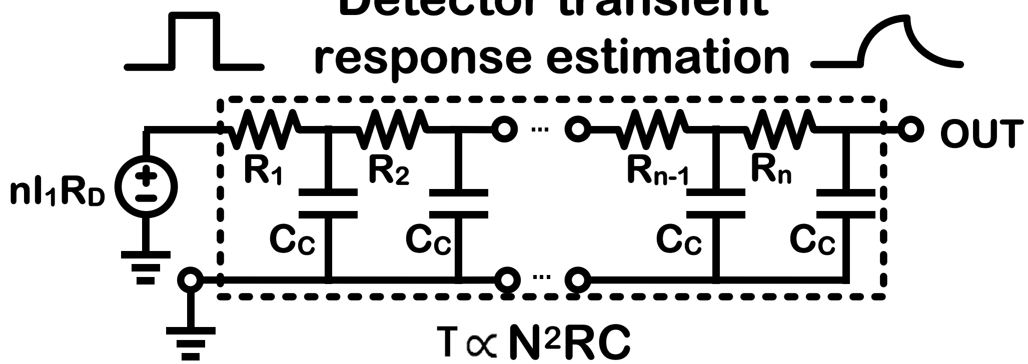
Front end noise sources



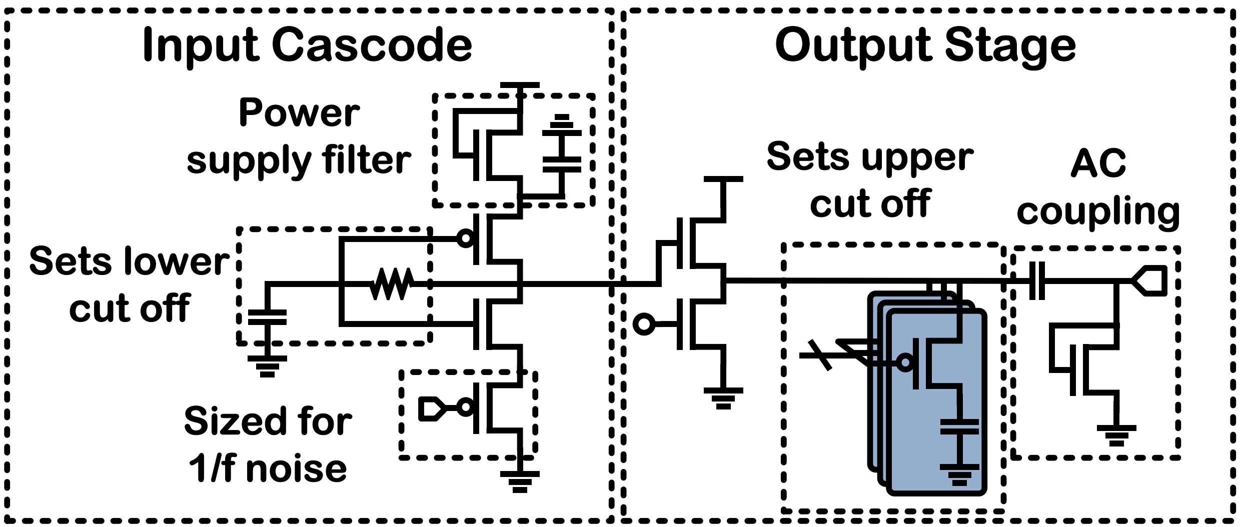
$$V_{nDET} \propto \sqrt{NR_D}$$

$$V_{nAmp} \propto \sqrt{1/I_D}$$

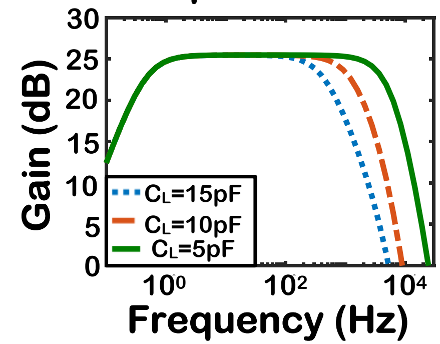
Detector transient response estimation



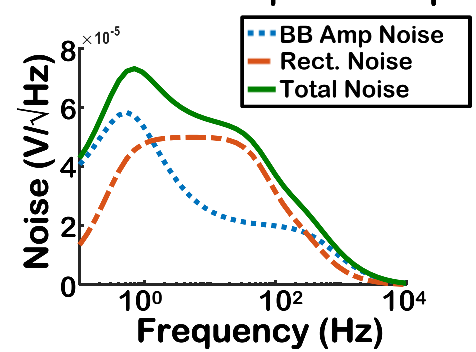
Baseband Amplifier Design



Simulated Baseband Amplifier Gain

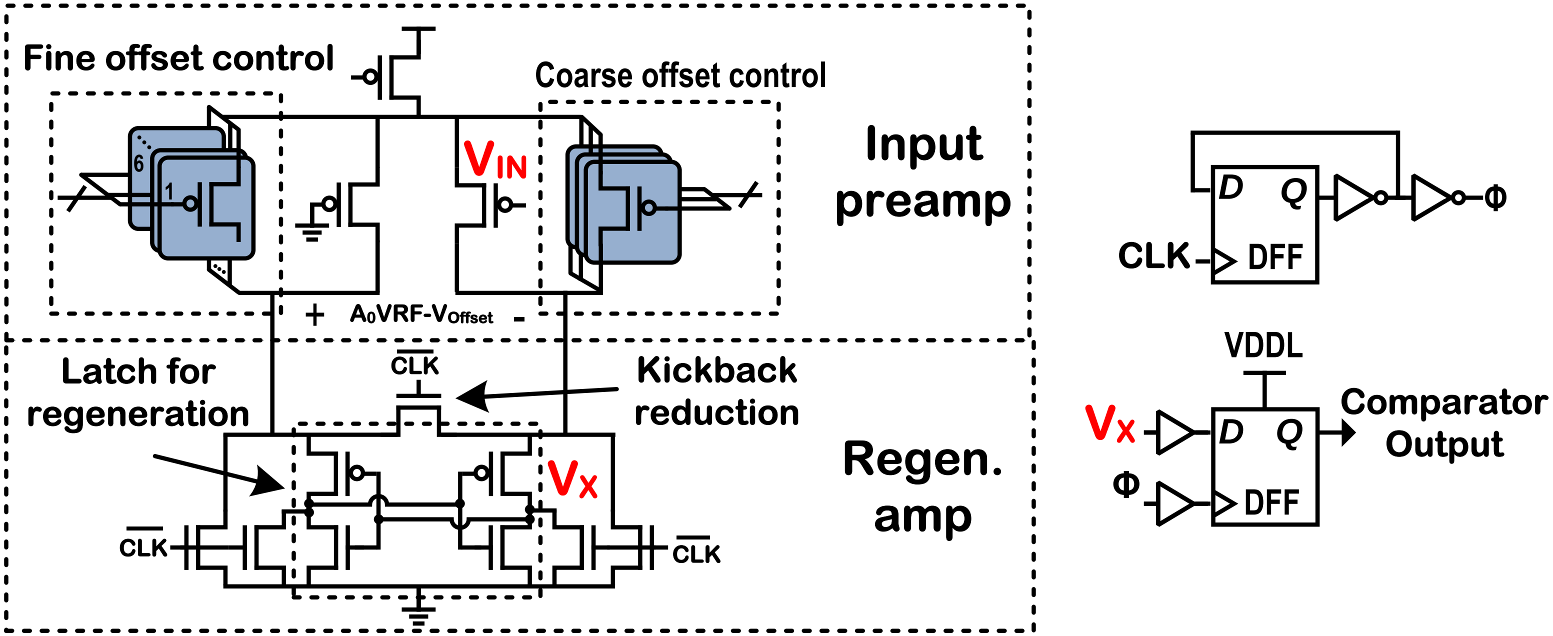


Simulated Noise Contributions Referred to Comparator Input



- Introduction of low frequency transmission zero rejects interferers
- DC power level set by output noise of rectifier

Comparator design

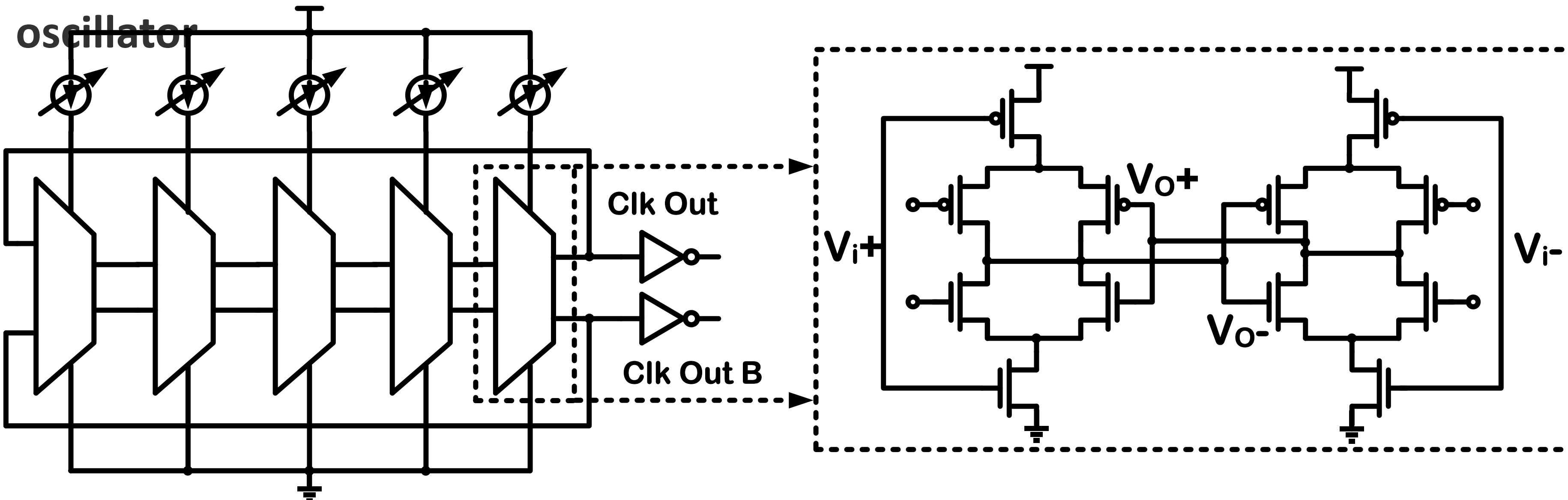


- Current reused between latching stage and preamplifier
- 9 bits of offset control allowing for ultra wide trip voltage range

Clock source

5 Stage current starved ring oscillator

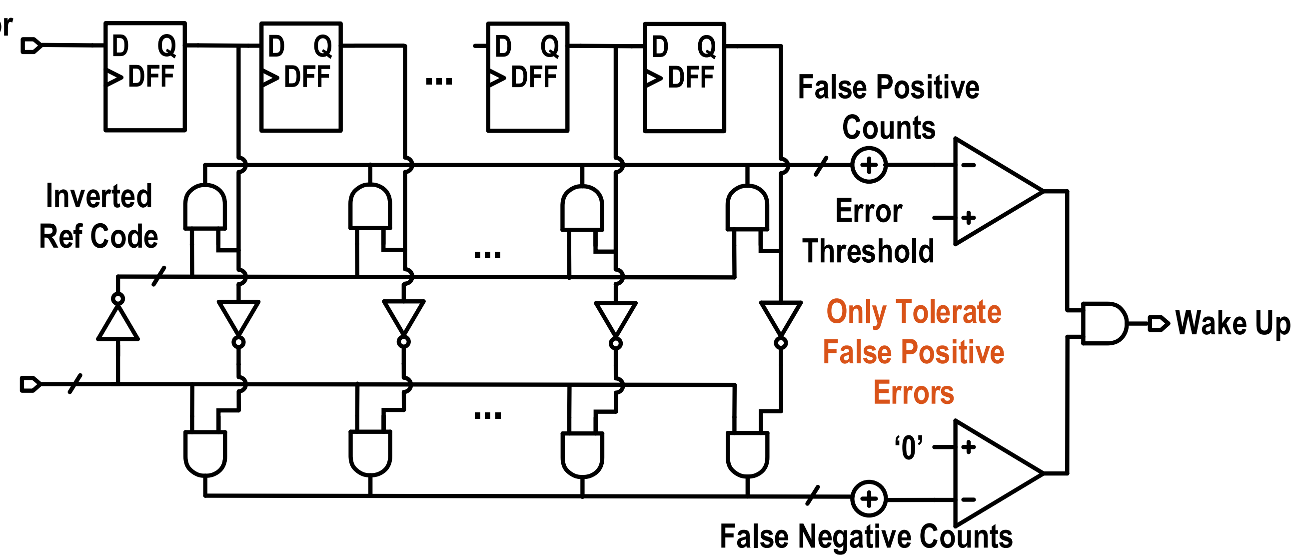
Unit gain unit cell



- External bias sets device bias and operation frequency
- Operates from 50 Hz to 10 kHz

Digital backend

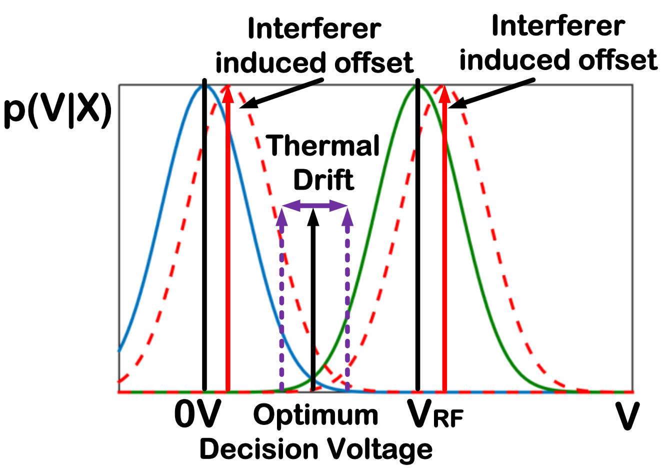
8-bit Shift Register Correlator with False Positive Error Tolerance

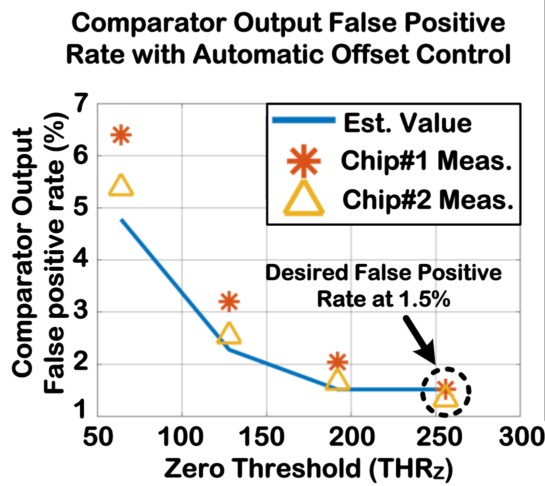


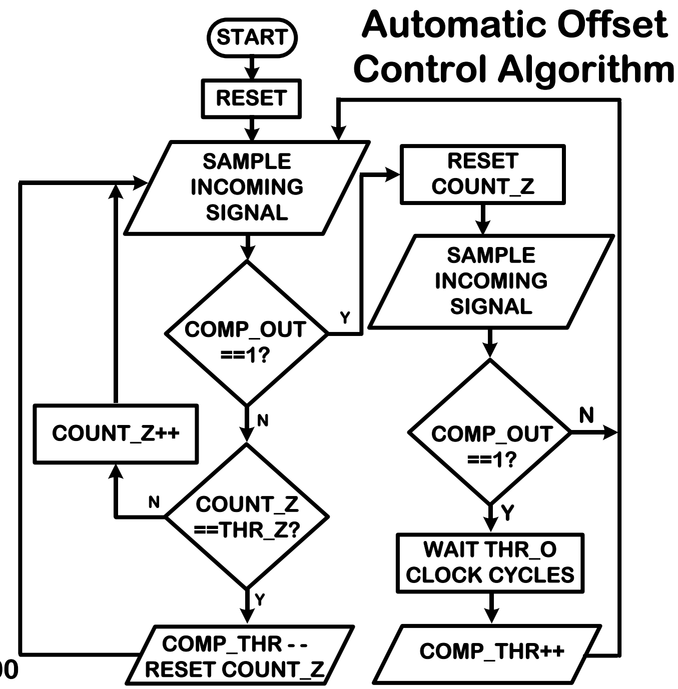
- Asymmetric error tolerance increases robustness without degrading false alarm rate
- <1 nW DC power consumption

Automatic offset control algorithm

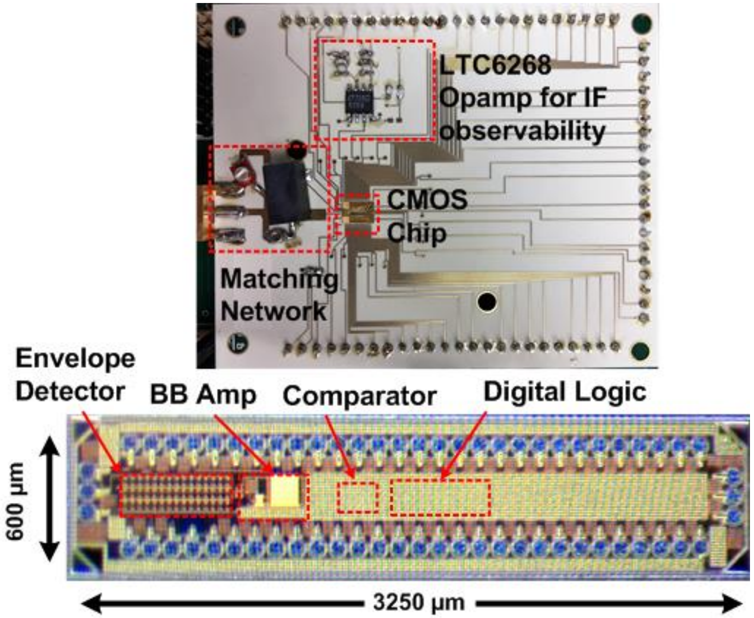
- Rejects fluctuations due to PVT variation dynamically
- No input RF signal required for calibration

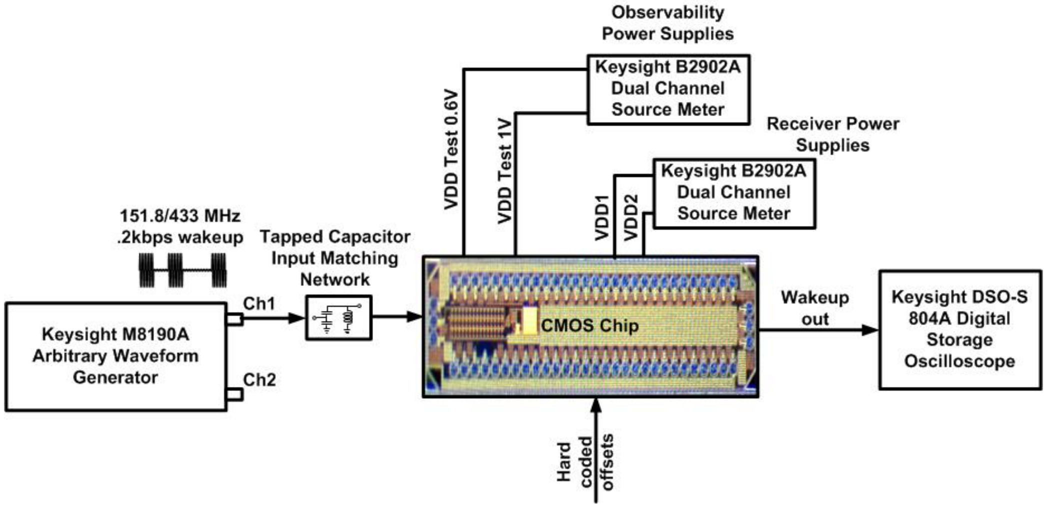






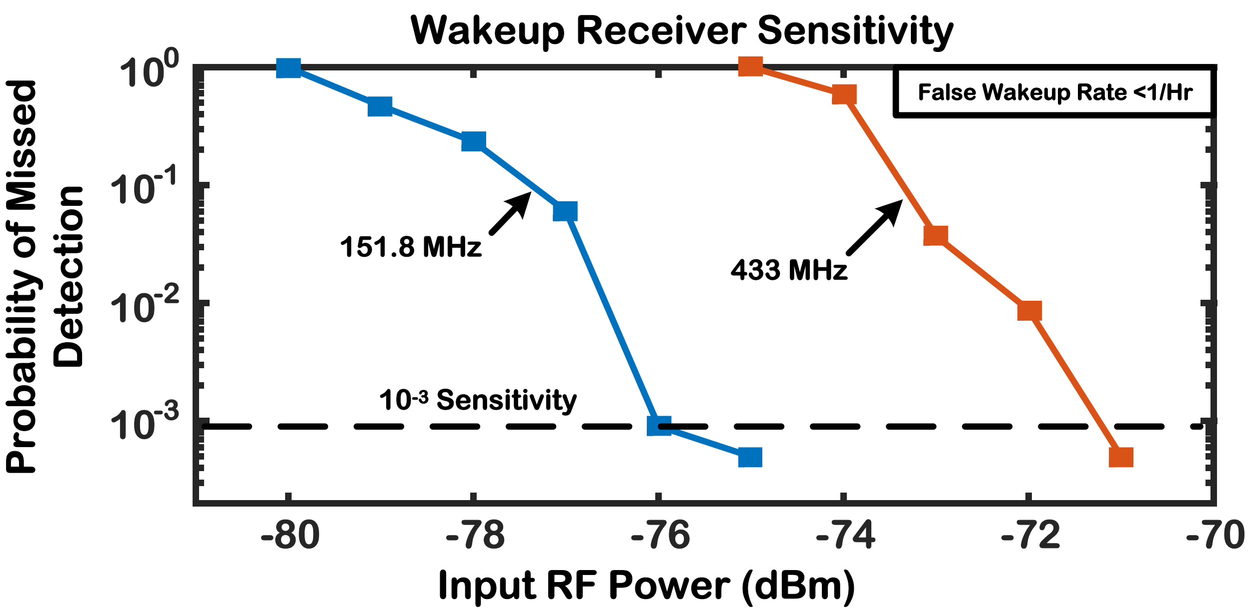
Measurement setup for power and sensitivity

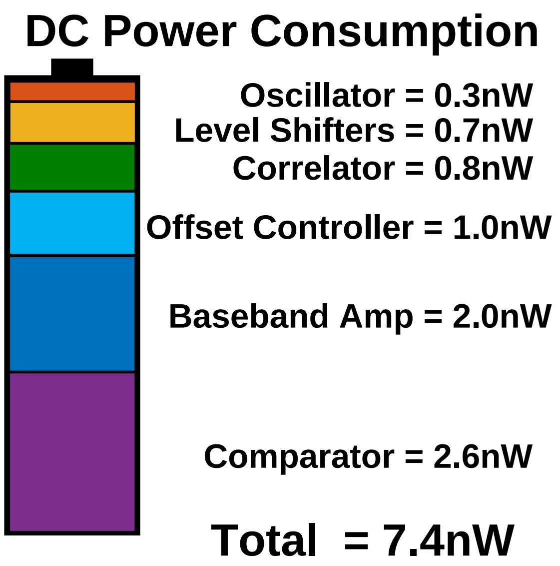




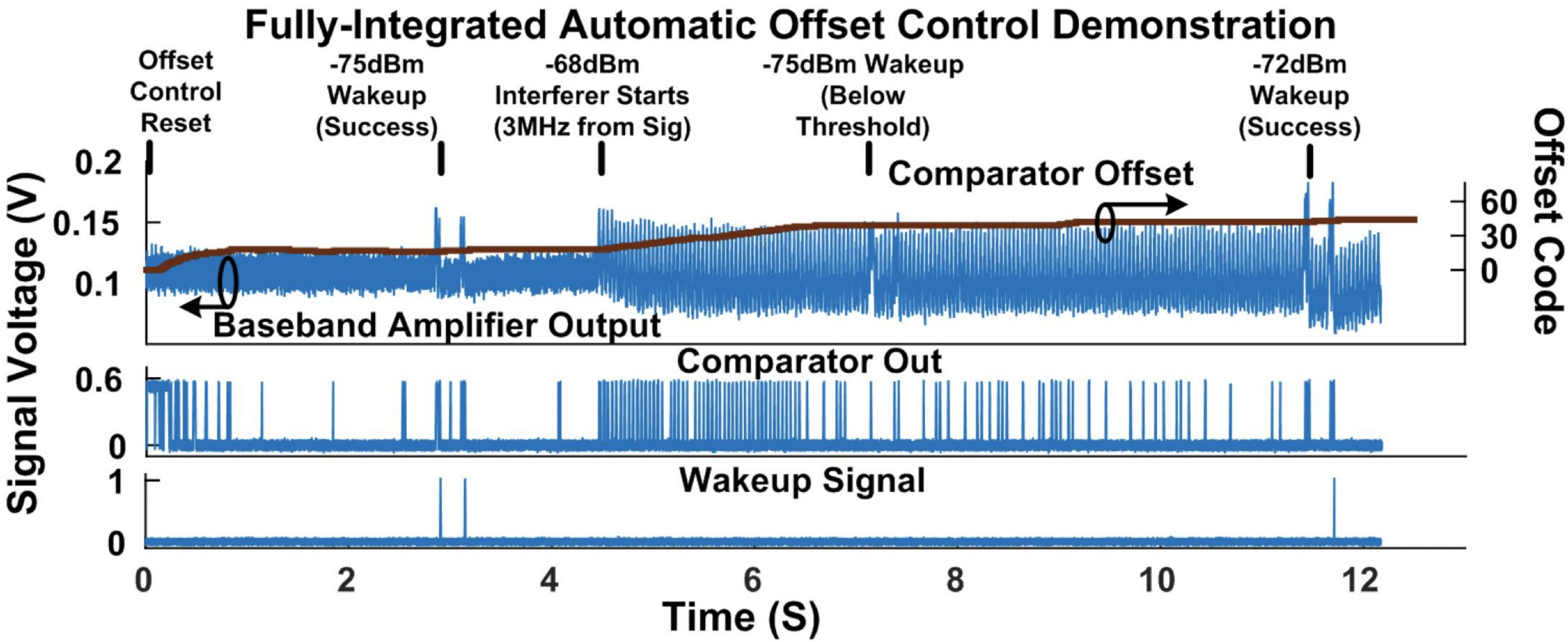
- **Chip fabricated in 130nm RF CMOS process**

Sensitivity measurement results





Automatic offset compensation and interferer rejection measurement results



Comparison to the state of the art

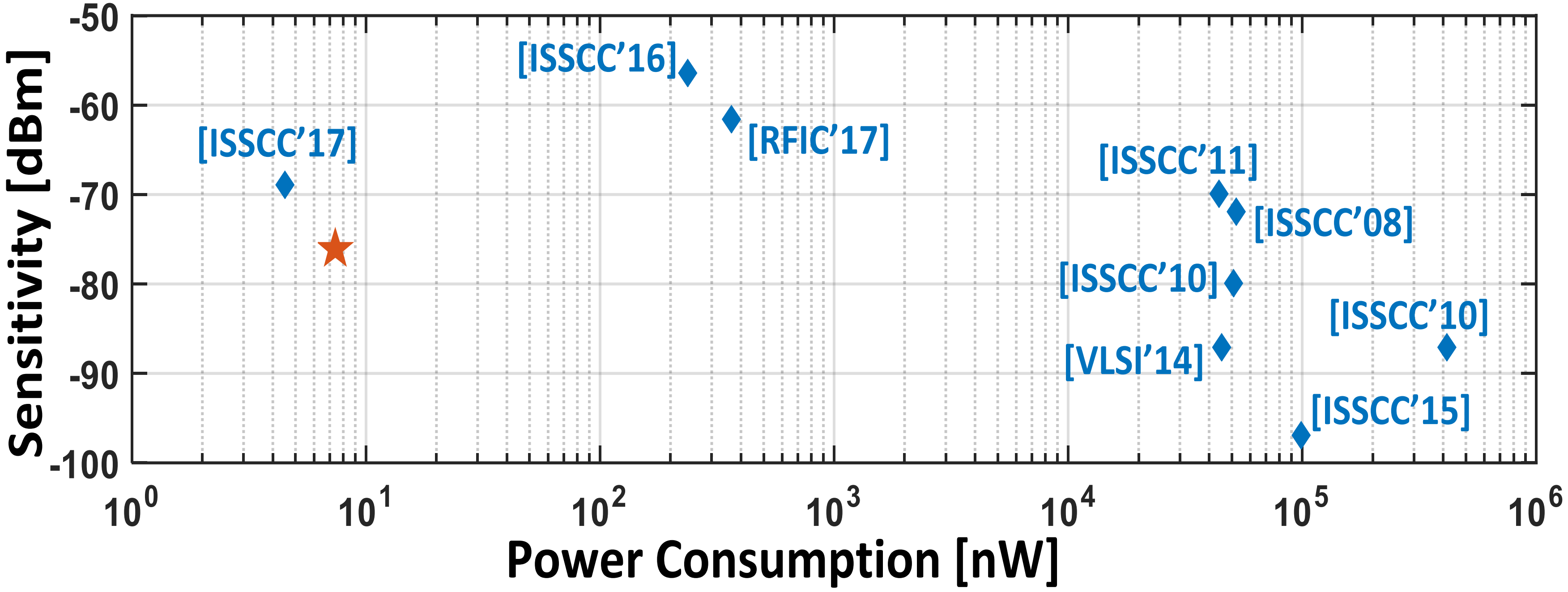
	This Work		Jiang ISSCC'17 [1]	Roberts ISSCC'16 [2]	Sadagopan RFIC'17 [3]	Salazar ISSCC'15	Abe VLSI'14	Pletcher ISSCC'08
Technology	130 nm		180 nm	65 nm	65 nm	65 nm	65 nm	90 nm
Carrier Frequency	151.8MHz	433MHz	113.5MHz	2.4GHz	2.4GHz	2.4GHz	925.4MHz	2 GHz
Power Consumption	7.4 nw	7.4 nw	4.5 nW	236 nW	365 nW	99 μW	45.5 μW	52 μW
Data Rate	200 bps	200 bps	300 bps	8.192 kbps	2.5 kbps	10 kbps	50 kbps	100 kbps
Dissipated Energy per bit	37 pJ	37 pJ	15 pJ	28.8 pJ	146 pJ	9900 pJ	910 pJ	520 pJ
Non-constant Envelope Interferer Rejection	Integrated Auto Offset Control Loop		N/A	N/A	N/A	N/A	2-Step Wakeup	N/A
Out-of-band Interferer Rejection Method	High-Q FE Transofrmer		High-Q FE Transformer	Matching Network	High-Q FE Co-Design	N-path filter	2-Step Wakeup	MEMS Filter
Sensitivity	-76 dBm [1]	-71 dBm [1]	-69 dBm [1]	-56.5 dBm [2]	-61.5 dBm [2]	-97 dBm [2]	-87 dBm [2]	-72 dBm [2]
Sensitivity with CW interference	-76 dBm [3]	N/A	N/A	N/A	-58.5 dBm [4]	-94 dBm [5]	-84 dBm [6]	N/A
Die Area	1.95 mm^2		6 mm^2	2.25 mm^2 *	1.1 mm^2 *	0.0576 mm^2 *	1.27 mm^2 *	0.1 mm^2 *

[1]10^{-3} Prob. of Missed Detection (PMD) [2]10^{-3} Bit Error Rate (BER) [3]Carrier-to-interference ratio (CIR)= -30dB @ -3MHz offset, 10^{-3} PMD [4]CIR=-20dB @ -3MHz offset, 10^{-3} BER. [5]CIR=-31dB/-27dB @ +/-5MHz offset, 10^{-3} BER [6]CIR= -40dB@ -3 MHz offset, 1% packet error ratio (PER)

* Active area

* Comparison made at initial publication of this work in February 2018

Comparison to the state of the art (cont.)



Conclusions

- Demonstration of -76 dBm sensitivity with 7.4 nW DC power consumption
- Utilizing novel offset compensation algorithms calibration can occur without power hungry RF test circuit
  - Suppresses non-envelope interference
- Front end detector choice is a critical design parameter for development of ULP WuRx
  - Achieved 15.8mV/nW OCVS at 151.8MHz and 6.3mV/nW at 433MHz
  - Total analog DC power <5 nW.
  - > 30dB envelope interference rejection

Acknowledgements

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  - Members of the University of Virginia IECS and RLP-VLSI Groups

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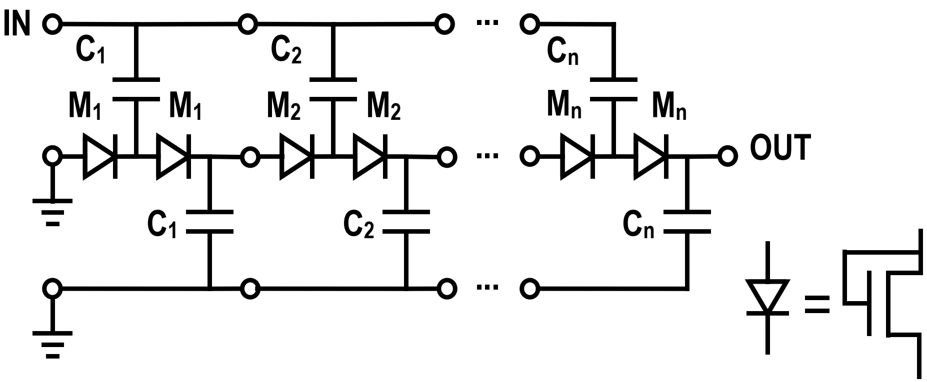
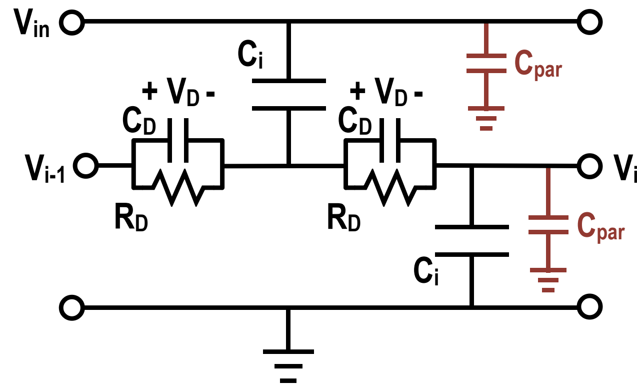
Front-end RF modeling



Detector Schematic

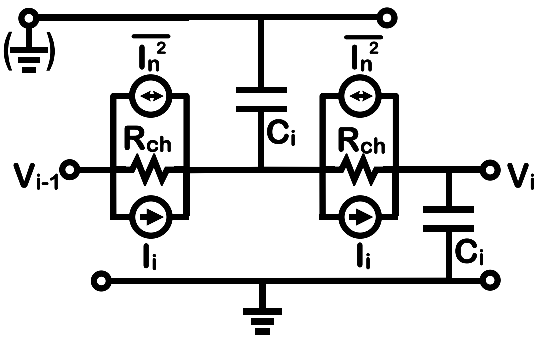


Single Stage model at RF

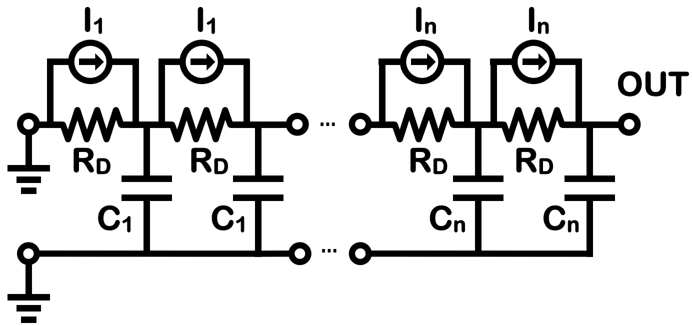
$$Y_{SS} \approx j\omega(C_{Par} + 2C_D) + {}^{2}/_{R_D} = {}^{2Y_{in}}/_{N} \qquad V_D = V_{in}\frac{C_i}{C_i + 2C_D}$$

- Parallelization of single stage diode detector
- Utilize lumped linear network theory to find Z_{in} and V_M

Detector baseband response modeling



Single Stage model at Baseband



Equivalent baseband output

Detector expressions

$$V_{OSigB.B} \approx N\mu_D \sum_{1}^{N} {V_D}^2$$

$$\overline{v_{nOut}^2} \approx 4kT\gamma_D N R_D$$

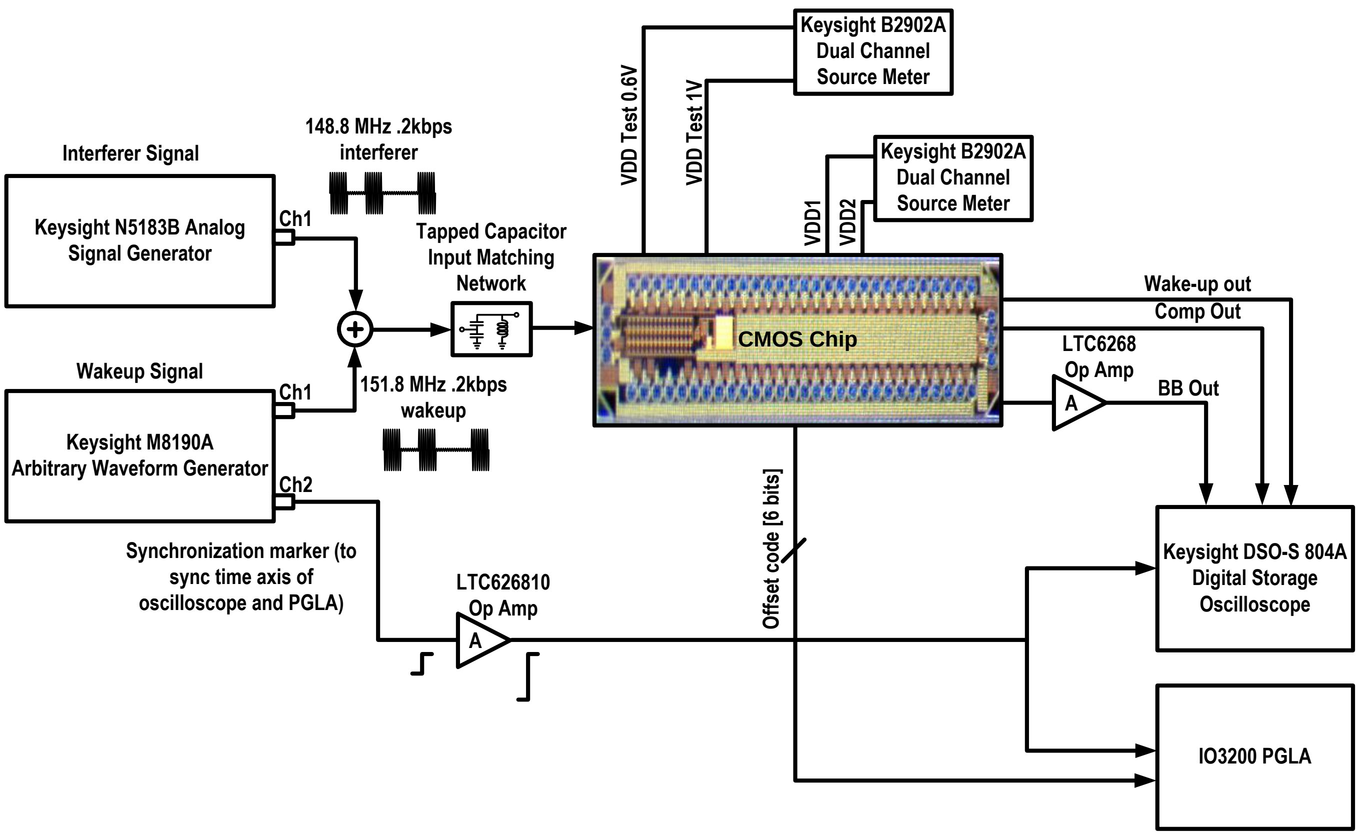
Single stage expressions

$$I_i = \mu_D G_{ch} {V_D}^2$$

$$\overline{I_n^2} = 4kT\gamma_D G_{ch}$$

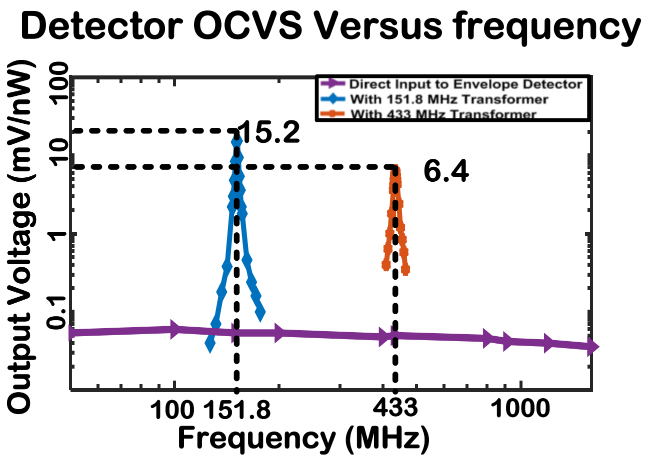
- Utilizing diode voltage found from RF models we apply a current source in parallel with each diode to find output
- Detector noise sources appear in parallel with signal sources

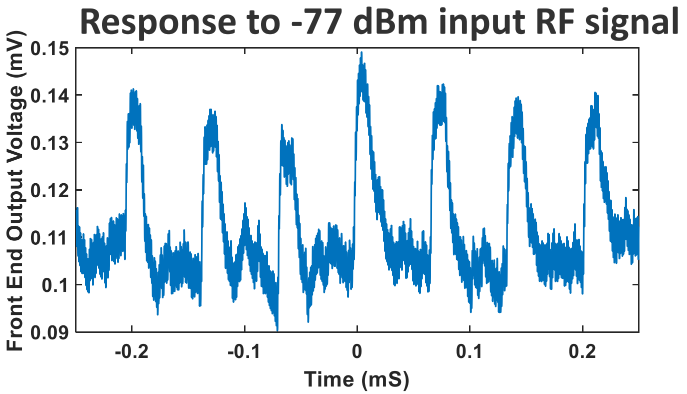
Measurement setup for interference



Measurement results for RF-FE

- **45 Stage Low VT Dickson rectifier utilized:**
  - **Utilized RSCE to decrease RD to ideal value**
  - **~ 15mV/nW sensitivity**
  - **~ 45kΩ shunt impedance**
  - **~ 650fF input capacitance**





Simplified sensitivity analysis

- Under the condition $C_{par} \gg NC_D$
- $V_{ODC} = N{V_i}^2\mu_D = \frac{N\mu_D R_D R_p P_{RF}}{R_D + NR_P}$ $where\ R_p \equiv Q_L L_{Res}\omega_0$
- $SNR_{Out} = \frac{N\mu_D R_D R_p P_{RF}}{(R_D + NR_P)\sqrt{4kTNR_DB}}$ where optimizing w.r.t N gives:
  - $N_{Opt} = \frac{R_D}{R_P}$ and $SNR_{Opt} \propto \mu_D P_{in}\sqrt{R_p}$ and SNR_{OPT} is independent of R_D at N_{OPT}

Full sensitivity expressions

- Assumption: Q_L is independent of L_{res}
- $C_i = NC_D + C_P$
- $SNR_{Opt} = \frac{\mu_D P_{in} R_D Q_{Ind}}{2\sqrt{(Q_{Ind}+Q_D)\overline{v_n}^2 Q_P}}$; $n_{opt} = \frac{Q_P}{Q_{Ind}+Q_D}$ where

  $Q_P = \omega_0 C_P R_D; Q_D = \omega_0 C_D R_D; Q_D = \omega_0 C_D R_D$