IDENTIFYING PROFESSIONAL COMPETENCIES OF THE FLIP-CHIP PACKAGING ENGINEER IN TAIWAN

Y. H. Guu
Department of Mechanical Engineering, National United University, Miaoli 360, Taiwan
yhorng@nuu.edu.tw

Kuen-Yi Lin
Department of Technology Application and Human Resource Development, National Taiwan Normal University, Taipei 106, Taiwan

Lung-Sheng Lee
Department of Technology Application and Human Resource Development, National Taiwan Normal University, Taipei 106, Taiwan

ABSTRACT
This study employed a literature review, expert interviews, and a questionnaire survey to construct a set of two-tier competencies for a flip-chip packaging engineer. The fuzzy Delphi questionnaire was sent to 12 flip-chip engineering experts to identify professional competencies that a flip-chip packaging engineer must have. Four competencies, including flip-chip technology, bumping process, stress analysis, and reliability testing, and their subordinate 15 competency indicators were developed. The results serve as a reference for designing or assessing curricula or programs for preparing a quality flip-chip packaging engineer and to be used as a guideline to recruit and select a flip-chip packaging engineer.

KEYWORDS: Professional competency, Packaging engineer, Flip-chip, Fuzzy Delphi

INTRODUCTION
Semiconductor technology has progressed from micrometers to nanometers, and wafer size has increased from 6 in. to 8 in. to 12 in. Each wafer contains several million electronic components. Environmental dust and humidity negatively affect the operation of these electronic components. Therefore, effective packaging protects the inner components. With increases in the functionality of electronic products, and the movement of integrated circuit (IC) fabrication toward high-end fields, the traditional wire bonding packaging technique is unable to satisfy the current demands of IC products. This has resulted in significant growth in the electronic packaging industry, which has subsequently generated the flip-chip packaging technology, a back-end processing in the IC manufacturing process.

In a globalized competitive environment, the life span of high-tech products has increasingly declined. Fostering the professional competencies of a flip-chip packaging engineer has become highly crucial for enabling the industry to respond to aggressive market competition and to create new fields and prospects (Williams, 2004). Ensuring that engineer and technician competencies correspond to industry requirements for innovation is the only way to respond rapidly to the following market changes, to master key production technologies, to shorten manufacturing time, to control product yield, and to reduce production cost (Cheng and Lin, 2003; Lin and Gary Hu, 2001).

Electronic devices consistently require high-density I/O connections, excellent electrical characteristics, and high transfer speeds. These demands present increasing challenges for engineers (Datta *et al.*, 2005; Lau, 2000). In globalized industrial competition, company advantages are only created through the quality of human resources contained within the enterprise (Nijkamp *et al.*, 2011). With the arrival of the knowledge and innovation economy generation, how educational institutions provide quality education to meet the demand side is a critical issue (Ministry of education, 2009). The rapid development of the electronic industry poses a simultaneous challenge for university and college education, who confront the dilemma of amending current curricula/programs to provide quality engineers for the electronic industry (Yang *et al.*, 2007). Universities and colleges must regularly update their curricula/programs to provide students with the latest knowledge and technology relevant to industry demands. This enables establishing a solid foundation for students that satisfies industry requirements (Chandran *et al.*, 2010). Mutual cooperation and exchange are required among industry, government, and universities/colleges to train quality engineers (Pan *et al.*, 2008).

Flip-chip packaging is currently used in high-end electronic devices, and its industry requires a quality engineer to ensure competitive advantage. A set of competencies can serve as a base to measure the overall balance of knowledge and skill, which a flip-chip packaging engineer must have. The professional competencies of a high-tech flip-chip packaging engineer lead industries in their future development. Establishing professional

competencies for the flip-chip packaging industry is imperative for students to acquire the knowledge and skills of the industry requisiteness and to ensure the immediate entrance of graduates into the workplace.

PURPOSE OF THIS STUDY

To reduce discrepancies between the supply side in universities/colleges and the demand side in industries requires identifying the professional competencies of a flip-chip engineer. Therefore, the purposes of this study are as follows:

- To identify professional competencies for a flip-chip packaging engineer.
- To identify competency indicators for a flip-chip packaging engineer.

The results serve as a reference among industry, government, and universities/colleges for fostering a quality flip-chip packaging engineer.

LITERATURE REVIEW

Professional competency

Professional competency (or competence) refers to substantial knowledge and skills gained following professional education or training and professionals who undertake a specific paid job or self-employment duties (Shyr, 2012; Spencer and Spencer, 1993). Professional competencies are the core of education. The goal of professional competency is to apply effectively the knowledge and skills that students learn at school to industry. The emphasis of professional education or training relates to enriching people's capabilities (Yan, 2005). Competencies are the collective learning in organizations, and involve how to coordinate diverse production skills and integrate multiple streams of technologies (Wikipedia, 2012). Competencies are identified behaviors, knowledge, skills, and abilities that definitely affect the achievement of employees and the success of industries (Chen, 2010; Rychen and Salganik, 2003).

Industrial developments change according to technological innovations, and the professional competencies acquire in universities/colleges should be updated regularly. The key to fostering quality engineers is mainly related to higher education. Therefore, training quality engineers at universities/colleges must be more actively implemented to improve the professional competencies of students, narrow the gap between academic and practical application, enhance work efficiency, and benefit the economy (Ministry of education, 2010).

Flip-chip packaging development for new products requires innovative engineering techniques. Although flip-chip packaging technology is continually evolving and the market offers unlimited business opportunities, it is also replete with challenges. The electronic packaging industry requires that students possess fundamental knowledge and professional skills in advanced packaging. Therefore, greater industry demand-oriented practical knowledge and skills should be integrated into university and college courses (Evans *et al.*, 2008).

Students with sufficient electronic packaging skills and reliability knowledge are received well by the electronic industry, and typically obtain excellent employment opportunities following graduation (Joshi *et al.*, 1997). In the rapidly developing electronic industry, flip-chip packaging technology faces new challenges. Analysis of the professional competencies required for flip-chip packaging assists in understanding industry demands and enables the planning of professional education or training curricula/programs in universities/colleges to increase competitiveness of the packaging industry.

Flip-chip packaging

Flip-chip packaging is a mainstream technology used in IC packaging that creates solder bumping on the I/O metal pad of the wafer (Orii *et al.*, 2009). The chips are cut from the wafer and rotated 180° for flux adhesion, and the substrate is aligned for die attachment. The telecommunications link is established through the reflow to join the bond pad of the substrate. Flip-chip packaging has the following three advantages, compared to the traditional wire bonding technique: (1) the ability to provide a higher I/O connection in the area array that satisfies the demands of high-end products; (2) using the solder ball to connect directly with the substrate, thereby reducing post-packaging volume; and (3) a short bonding wire in the packaged structure with low capacitance characteristics, and low inductance consequently enhances electrical characteristics and reduces signal delay or noise, achieving excellent heat dissipation performance (Lo and Tung, 1997; Yu *et al.*, 2007).

Earlier flip-chip packaging has been used primarily for packaging CPUs. Packaging technology was subsequently used for packaging high-end graphic chips, high-end chip sets, programmable logic chips, high-frequency network communication class chips, and high-speed ASIC. The coefficients of thermal expansion (CTE) of the substrate, chip, and bump differ from each other. After repeated cycles of heat expansion and cold contraction, cracks develop in proximity to the joint, thereby influencing interconnection reliability. The underfill process between the chip and the substrate is necessary. The spaces underneath the chip are filled through

capillary action, and the dispersed stress effectively strengthens the structure. The greatest difficulty for flip-chip packaging is that the chips, tin/lead bumps, and substrate cause damage or defects because of the CTE mismatch, and consequently reduce its reliability.

The design of the flip-chip packaging structure has a profound influence on reliability. Therefore, the structure design plays a critical role in flip-chip packaging (Zhang *et al.*, 2010). To accommodate market needs and improve competitiveness, the packaging structural design, raw materials, and manufacturing processes must be able to rapidly change and innovate to meet new challenges (Lay Yeap, 2010; Yang *et al.*, 2010). Flip-chip packaging industry-based education/training refers to the planning of curricula/programs according to the demands of the packaging industry. This could narrow the gap between education/training and industry, and therefore assist students in obtaining relevant professional knowledge and skills required in the workplace.

METHODOLOGY

Fuzzy Delphi technique

The Delphi technique employs a series of questionnaires in repeated surveys to collect expert opinions on specialized subjects until decision-makers agree on a unanimous conclusion and achieve an accurate, logical result. This method is an effective technique for gathering and obtaining expert opinions to solve specific issues. The primary advantage of this technique is the flexible and effective collation of opinions and perspectives from an expert panel to conclude an expert consensus for decision-making (Skulmoski *et al.*, 2007). The Delphi technique is a method for group decisions and is employed in evaluating, assessing, and predicting events and their development for decision-making consideration. Areas such as developing core competencies (Kuo *et al.*, 2011; Olson *et al.*, 2005; Shyr, 2012), engineering (Chang *et al.*, 2011; Xia and Chan, 2012), and management (Imanova, 2009; Mallen *et al.*, 2010) currently use it widely.

The Delphi method primarily employs expert knowledge as its base and collects expert perspectives on specific problems through multiple questionnaire surveys. Personal subjective prejudice is placed aside until experts reach a consensus (Okoli and Pawlowski, 2004). Expert opinions may vary when striving for conformity, producing divergent views that cannot be integrated. The convergence of topics is poor, and therefore, increased numbers of questionnaire surveys are necessary. This increases manpower consumption, and budget expenditure, and may be inconvenient for interviewees (Nworie, 2011). Dalkey (1969) showed that when employing the Delphi method to investigate a problem, if the number of experts involved is greater than 11, the group error minimizes and yields reasonable results. For statistical calculations, the Delphi method uses average values as a selection basis. This implies that the statistical results are easily influenced by outliers and potentially result in misrepresenting the original meanings of experts (Hartman and Baldwin, 1995).

Murry et al. (1985) integrated the traditional Delphi method and fuzzy theory to establish the fuzzy Delphi technique and improve the shortcomings of the traditional Delphi technique. Fuzzy expert questionnaires are designed for the investigated topic and assemble a suitable expert panel. All experts are requested to evaluate each assessment item for the topic and assign possible interval values. The smallest value from this interval represents the most conservative cognitive value of an assessment item as evaluated by the expert, whereas the largest value from this interval represents the most optimistic cognitive value. The fuzzy Delphi technique emphasizes the fuzzy processing of expert messages and adopts and integrates the opinions of individual experts.

Compared to the traditional Delphi technique, this method reaches an expert consensus in a shorter time and facilitates the group decision-making goal (Hsu *et al.*, 2010). The fuzzy Delphi method enables fewer questionnaire surveys, avoids frequent investigations, and obtains an objective and logical conclusion. This method enables participating experts to fully and completely express their views and solves the problem of linguistic fuzziness in expert opinions (Chang *et al.*, 1995). Kaufmann and Gupta (1988) confirmed that the fuzzy Delphi technique requires the participation of only 12 experts to obtain a valid analytical result. The traditional Delphi technique has the problem of experts not reaching a consensus because of diverging opinions, which leads to increased survey cost and a probable scenario where the data integrator rejects the exceptional opinion of a specific expert. Advantages of the fuzzy Delphi technique include the ease of integrating expert advice to form a consensus for decision-making (Hsu, 2011; Kuo and Chen, 2008). Therefore, this study employs the fuzzy Delphi technique to solicit and integrate the opinions of experts in the flip-chip packaging industry and to identify the required professional competencies for a flip-chip packaging engineer.

Research procedure

The study procedure involves the following steps: (1) Drafting professional competencies for a flip-chip packaging engineer. Literature related to the required professional competencies of a flip-chip packaging engineer was collected, synthesized, and summarized into a preliminary draft, which served as a blue

print for developing fuzzy Delphi questionnaires; (2) interviewing experts to assess the aforementioned professional competencies draft. Flip-chip experts were interviewed to assess the drafted professional competencies to examine their correctness and appropriateness, and to make necessary amendments, deletions, and revisions; and (3) conducting the fuzzy Delphi survey. The professional competencies and competency indicators listed on the fuzzy Delphi questionnaire were assessed and confirmed.

Survey participants

Twelve experts with practical experience were invited to participate in the fuzzy Delphi expert survey questionnaire to identify the required professional competencies for a flip-chip packaging engineer. The selection criteria for the 12 experts were as follows: (1) currently employed professional personnel specializing in in-depth understanding of the flip-chip packaging industry; (2) over 5 years of practical experience in flip-chip packaging; and (3) in possession of sufficient professional knowledge with excellent research and development results.

Research instrument

Industry technologies change rapidly, and professional knowledge is updated on a daily basis. The professional competencies for a flip-chip packaging engineer must conform to the current demands of the flip-chip packaging industry. Spencer and Spencer (1993) stated that any specific work competency should be confirmed and designated according to the following three steps: (1) recruit experts in the relevant field and establish a focus group; (2) analyze work competency content through a literature review and expert consultation; and (3) establish work competency based on the consensus of the recruited expert team.

After a literature review and industry expert interviews, the required professional competencies for a flip-chip packaging engineer are identified to include the following four domains: flip-chip technology, bump process, stress analysis, reliability testing, and 20 professional competency indicators, as shown in Table 1. The competencies in flip-chip technology contain six indicators, the bump process contains five indicators, stress analysis contains four indicators, and reliability testing contains five indicators. The fuzzy Delphi questionnaire survey of professional competencies for a flip-chip packaging engineer developed in this study conforms to academic theoretical foundations, and 12 experts verified the questionnaire items. Therefore, the questionnaire serves as the research instrument and is valid and reliable.

Table 1: Identified competencies of the flip-chip packaging engineer

Competencies Items
1. Flip-chip technology
1.1 Understand the evolutionary and developmental trends of packaging technology and the role Taiwan plays in these trends
1.2 Understand the application of flip-chip packaging technology
1.3 Possess flip-chip packaging process knowledge
1.4 Understand the structure of flip-chip packaging
1.5 Possess the ability to design a flip-chip packaging structure
1.6 Understand the items that require preparation prior to flip-chip packaging
2. Bump process
2.1 Possess knowledge on bump chemical composition and the ability to select bump configuration
2.2 Understand the influence of solder bump density and bump configuration on filling flow
2.3 Understand the characteristics and manufacturing process of different bump materials
2.4 Understand the bump quality assessment items and inspection standards
2.5 Possess the ability on the influence of bump array and density on reliability
3. Stress analysis
3.1 Understand the relationship among thermal stress, temperature distribution, and warping
3.2 Possess knowledge on the influence of different structures and materials on heat dissipation
3.3 Understand the parameters that influence packaging stress
3.4 Possess the ability to conduct a heat resistance assessment of flip-chip packaging
4. Reliability testing
4.1 Familiarity with reliability inspection methods for flip-chip packaging
4.2 Understand the reliability standard, demand, and current industry situation
4.3 Possess quality control concepts
4.4 Understand the cause of flip-chip packaging structural deformation and improvement

	strategies
4.5	Understand the characteristics of underfill and its influence on reliability

RESULTS AND DISCUSSION

The data collected from fuzzy Delphi questionnaires were analyzed primarily using triangular fuzzy numbers. The analytic process involves the following five steps: (1) establishing triangular fuzzy numbers; (2) defuzzification; (3) obtain the right boundary value; (4) obtain the left boundary value; and (5) calculate the total utility of the fuzzy numbers. During triangular fuzzy number calculation, Microsoft Excel statistical software was used to convert expert opinions to triangular fuzzy numbers. The defuzzification results are shown in Table 2. The criteria for professional competencies were as follows: If the total utility of the assessment item is greater than 0.6 (Threshold value), it is considered a required professional competency for a flip-chip packaging engineer. Conversely, if the total utility is less than or equal to 0.6, the assessment item is rejected as a professional competence for a flip-chip packaging engineer.

According to the statistical results of fuzzy Delphi analysis shown in Table 2, Items "1.1 Understand the evolutionary and developmental trends of packaging technology and the role Taiwan plays in these trends," "1.6 Understand the items that require preparation prior to flip-chip packaging," "2.5 Possess the ability on the influence of bump array and density on reliability," "3.3 Understand the parameters that influence packaging stress," and "3.4 Possess the ability to conduct heat resistance assessment of flip-chip packaging," obtained a total utility of less than 0.6, and were thus rejected and deleted. Consequently, the professional competencies for a flip-chip packaging engineer include four professional competencies and 15 indicators.

Table 2: Statistical results obtained by analyzing each item in the official questionnaire using the fuzzy Delphi method

Aspect	Item	a_k, b_k, c_k	μ_R, μ_L, μ_T	Total utility	Threshold value (0.6)
1. Flip-chip technology	1.1	(0.3, 0.63, 0.9)	(0.711, 0.524, 0.593)	0.593	×
	1.2	(0.3, 0.69, 1)	(0.766, 0.501, 0.632)	0.632	ˇ
	1.3	(0.3, 0.75, 1)	(0.801, 0.482, 0.659)	0.659	ˇ
	1.4	(0.4, 0.76, 1)	(0.810, 0.439, 0.685)	0.685	ˇ
	1.5	(0.4, 0.68, 1)	(0.763, 0.465, 0.648)	0.648	ˇ
	1.6	(0.2, 0.59, 0.9)	(0.689, 0.573, 0.557)	0.557	×
2. Bump process	2.1	(0.3, 0.66, 1)	(0.751, 0.511, 0.619)	0.619	ˇ
	2.2	(0.3, 0.66, 0.9)	(0.727, 0.513, 0.606)	0.606	ˇ
	2.3	(0.4, 0.67, 1)	(0.752, 0.472, 0.639)	0.639	ˇ
	2.4	(0.4, 0.61, 0.9)	(0.700, 0.493, 0.603)	0.603	ˇ
	2.5	(0.3, 0.64, 0.9)	(0.718, 0.519, 0.599)	0.599	×
3. Stress analysis	3.1	(0.3, 0.64, 1)	(0.736, 0.521, 0.607)	0.607	ˇ
	3.2	(0.3, 0.65, 0.9)	(0.721, 0.517, 0.602)	0.602	ˇ
	3.3	(0.3, 0.61, 1)	(0.721, 0.532, 0.594)	0.594	×
	3.4	(0.2, 0.55, 0.9)	(0.668, 0.591, 0.538)	0.538	×
4. Reliability testing	4.1	(0.2, 0.67, 1)	(0.757, 0.540, 0.608)	0.608	ˇ
	4.2	(0.4, 0.70, 1)	(0.769, 0.461, 0.653)	0.653	ˇ
	4.3	(0.4, 0.72, 1)	(0.755, 0.471, 0.641)	0.641	ˇ
	4.4	(0.4, 0.71, 1)	(0.779, 0.455, 0.661)	0.661	ˇ
	4.5	(0.5, 0.68, 0.9)	(0.740, 0.421, 0.659)	0.659	ˇ

Notes： (a_k, b_k, c_k) denote the triangular fuzzy numbers; (μ_R, μ_L, μ_T) represent the right boundary value, left boundary value, and total utility, respectively. "×" represents "should be deleted."

Competency in flip-chip technology

Flip-chip packaging technology involves the direct assembly of chips on circuit boards (COB). The solder bump where the flip-chip is connected exhibits characteristics of high-density packaging and small-signal delays. Flip-chip packaging provides an IC component with a comprehensive structure that prevents component damage caused by external forces, deters corrosion caused by environmental factors, and ensures the standard transmission of signals to enable components to perform their designated functions. The applications of flip-chip packaging are described in Section 3.2 and are thus not reiterated here.

Numerous in-depth studies (Amalu and Ekere, 2012; Jen *et al.*, 2011; Lu *et al.*, 2012) have investigated the structural design of flip-chip packaging and analyzed its characteristics. Related studies have shown that a difference in the design of flip-chip packaging alters the product characteristics. The flip-chip packaging engineer who plans to innovate and create new products should begin by understanding structure to develop competence in packaging design. Therefore, Items 1.2 to 1.5 in flip-chip technology that describe the indices of professional competence are crucial to a flip-chip packaging engineer.

Competency in bump process

The bump is a crucial element in flip-chip connection. Flip-chip packaging differs from the wire bonding process that employs metal wires to connect the chip and the substrate. The solder bumps are made on the bond pads that then connect with the substrate. As an IC component, the primary function of the solder bump is signal transmission. The solder bump creates a fine-pitch interconnection and reduces signal transmission time. Based on the type of material used, the solder bump can be divided into the following three categories: high-lead solder bump, eutectic solder bump, and lead-free solder bump.

The material used currently for bump is lead-free solder (Lee *et al.*, 2009). Tin-lead materials have been used to connect the chip to the substrate. The main advantages of tin-lead are low production cost, excellent resistance to thermal fatigue, strong mechanical properties, and good reliability. However, lead is a heavy metal that pollutes the soil and underground water systems. Lead poisoning in humans occurs when the amount of lead in the blood exceeds a certain value, eventually damaging the nervous and reproductive systems as well as the brain. Lead is a chemical that is severely hazardous to human health and the natural environment. Considering environmental awareness and human health, the European Union announced the Restriction of the Use of Hazardous Substances (RoHS) directive, which prohibits electronic products and electronic equipment that contain the following six substances from being commercially available: lead (Pb), mercury (Hg), cadmium (Cd), hexavalent chromium (Cr^{6+}), polybrominated biphenyls (PBBs), and polybrominated diphenyl ethers (PBDEs) (WEEE, 2000).

The materials used for the lead-free solder bump include Sn/Ag, Sn/Cu, and Sn/Ag/Cu. However, compared to lead-containing materials, lead-free materials have a higher Young's modulus and lower CTE, rendering lead-free materials more fragile, and increasing their reflow temperature. The packaging process produces a greater amount of thermal stress, leading to solder bump cracking that reduces electronic component effectiveness. Therefore, a flip-chip packaging engineer should have adequate knowledge of solder material composition to enable them to respond to the current environmental awareness trend while maintaining product quality.

Numerous studies have investigated optimizing various solder bump structures and materials. The results show that the choice of solder bump structure and material effectively influences the stress and quality of the eventual product (Chen and Lin, 2010; Zhang *et al.*, 2010). The solder bump is commonly damaged by thermal stress resulting from incompatible CTEs of packaging materials under TC conditions, which causes the solder bump to lose its signal transmission function. Therefore, a flip-chip packaging engineer should possess the occupational standard requirements listed in Item 2.1 to respond to bump structure changes and to develop new technologies for bump manufacturing. For the occupational standards listed in Item 2.2, numerous reports published by electronic packaging research and development personnel have investigated the influence of solder ball density and solder bump configuration on the underfill flow (Lee *et al*., 2011; Lin *et al*., 2008). Increased bump density obstructed liquid flow, which increased resistance flow of the underfill, causing liquid flow at a slower speed, and increasing the time required for filling. To reduce production time and packaging cost, a flip-chip packaging engineer must have in-depth knowledge of the influence of solder ball density and bump arrangement on underfill flow. Bump quality is determined by the competencies of a flip-chip packaging engineer in areas such as bump materials, bump geometric structure, bump density, and bump arrangement. Item 2.3 of the occupational standards is the most important step in the flip-chip packaging process for electronic components. A flip-chip packaging engineer should be aware of the required inspections and relative standards of bump height, diameter, coplanarity, shearing stress, voids, undercut of the under bump metallurgy (UBM), resistance, and leakage. The occupational standards listed in Item 2.4 must be achieved, and the most current knowledge and

technologies should be employed to ensure that solder bump quality adheres to industrial demands.

Competency in stress analysis

Increased packaging density of the IC chip has raised the working temperature of the packaged body that potentially results in failure. Heat is a main factor in causing thermal stress in electronic products. In the development of new-generation IC packages, heat-analysis is an essential technology (Yuan *et al.*, 2007; Zhang *et al.*, 2008). The incompatibility between the CTEs of materials in different structural layers produces thermal stress because of temperature changes. This stress causes deformation or warpage of the packaged structure. In severe cases, it can disrupt the packaging components and damage the chip, resulting in functional failure. Suzuki et al. (2007) stated warpage to be a problem of flip-chip packaging that urgently requires a solution. The thermal stress created by temperature loading is one of the main causes of deformation, warpage, and failure of flip-chip packaging (Tsai *et al.*, 2009).

The mechanical behavior of flip-chip packaging closely correlated with the reliability of electronic devices. Stress or deformation measurement for packaged products is difficult and cumbersome. Therefore, to gain information on the mechanical behavior of flip-chip packaging, engineers must be competent in computer-aided engineering to analyze the mechanical behavior of the packaged structure (Cho *et al.*, 2008; Tsai and Chang, 2008). The flip-chip packaging engineer must possess Items 3.1 and 3.2 of the occupational standards to alter the sizes and material properties appropriately in each layer of the packaged structure to reduce structural stress and improve packaging quality.

Competency in reliability testing

To understand product behavior in physical environments, and its stress toleration and life span, products must undergo Joint Electron Device Engineering Council (JEDEC) reliability tests. The primary tests are the moisture sensitivity level test (MSLT), the temperature cycling test (TCT), the high-temperature storage test (HTST), and the highly accelerated stress test (HAST). The flip-chip packaging engineer must be familiar with these test methods and understand their standards, requirements, and current situations to conform to the occupational standards listed in Items 4.1 and 4.2. Quality testing of the packaged product includes tests of electrical characteristics, mechanical properties, the environment, and reliability. The flip-chip packaging engineer must have the quality control occupational standards listed in Item 4.3 to produce packaged products that meet desired specifications and standards and possess excellent performances. The extent of deformation is one of the key indices in evaluating the quality of flip-chip packaged products. Therefore, Item 4.4 of the occupational standards has attracted the concern and attention of the flip-chip packaging industry. Thermal stress causes deformation of the flip-chip packaging structure.

Selecting appropriate packaging material, altering manufacturing parameters, and modifying the packaged product type achieves improved deformation of the flip-chip packaging structures. From a material selection viewpoint, reducing material shrinkage, lowering CTE, and increasing the elastic modulus mitigates deformation. Packaged product configuration, such as packaging material thickness, substrate thickness and material type, chip size, and product structure symmetry, are all critical factors that result in deformation. From a manufacturing parameter perspective, the pressure, temperature, and duration of packaged molds are important factors that cause deformation of the packaged structure when using thermosetting material or epoxy molding compounds (EMCs).

The flip-chip packaging engineer who adequately understands the relationship between the manufacturing conditions and the deformation of the packaged structure provides the most favorable packaged parameters, thus improving the reliability of flip-chip packaging. In Item 4.5 of the occupational standards, the underfill process is crucial to flip-chip packaging. This process exhibits a significant influence on the package reliability of integrated circuits (Huang *et al.*, 2011; Wan *et al.*, 2007). Underfills can also be used as a buffering layer for thermal stress to insulate the chip from the outside environment (Yang and Young, 2012). This prevents circuit corrosion caused by moisture, leading to signal interruption. Therefore, to increase the reliability of flip-chip packaging, a packaging engineer must possess Item 4.5 of the occupational standards to ensure that the products correspond to the demands of the flip-chip packaging industry.

CONCLUSION

We developed and identified the professional competencies of a flip-chip packaging engineer by using the fuzzy Delphi technique. This method was used to analyze the opinions of experts and to confirm the professional competencies for a flip-chip packaging engineer. The final results include competencies in the following four domains: flip-chip packaging technology, bump process, stress analysis, and reliability testing. Their subordinate 15 professional competency indicators were also identified.

The flip-chip packaging technology domain is composed of four necessary indicators. Indicator 1.4, "Understand the structure of flip-chip packaging," is the most necessary professional competency indicator for an engineer in the flip-chip packaging technology domain. The bump process domain consists of four necessary indicators. Indicator 2.3, "Understand the characteristics and manufacturing process of different bump materials," is the most important professional competence indicator for a flip-chip packaging engineer in the bump process domain. The stress analysis domain is composed of two necessary indicators, and the reliability testing aspect consists of six necessary indicators. Indicator 4.4, "Understand the cause of flip-chip packaging structural deformation and improvement strategies," is the most vital professional competency indicator for a flip-chip packaging engineer in the reliability testing domain.

Selecting appropriate materials, optimizing the packaged structure design, environmental testing, and reliability assessments are critical aspects of flip-chip packaging. The flip-chip packaging engineer who possesses the competencies identified in this study will be able to explore the causes of problems and find solutions to solve these problems. The packaging engineer can also propose prevention strategies and improve production capacity and the quality of flip-chip packaged products.

The required professional competencies of a flip-chip packaging engineer include knowledge and skills. Professional competencies can be attained through professional education and training to enable engineers to resolve difficulties encountered at work. Related curricular or programs should include the four domains and 15 professional competency indictors for a flip-chip packaging engineer, to provide students with clear learning goals, increase their employment competitiveness, and cultivate talented people who can satisfy the demands of the flip-chip packaging industry.

ACKNOWLEDGMENTS

We would like to express our sincere thanks to the National Science Council of Taiwan, Republic of China, for funding support under grant NSC 100-2511-S-239 -002.

REFERENCES

Amalu, E.H., & Ekere, N.N. (2012). High temperature reliability of lead-free solder joints in a flip chip assembly. *Journal of Materials Processing Technology*, 212(2), 471-483.

Chandran, D.P.K., Sow, Y.K., Harizan, M.H.M., Kooi, C.C., Hoy, T.T., & Foong, C.K. (2010). Success story of collaboration between Intel and Malaysian universities to establish and enhance teaching and research in electronic packaging. *34th International Electronics Manufacturing Technology Conference*, Melaka, Malaysia.

Chang, I.S., Tsujimura, Y., Gen, M., & Tozawa, T. (1995). Efficient approach for large scale project planning based on fuzzy Delphi method. *Fuzzy Sets and Systems*, 76(3), 277-288.

Chang, P.L., Hsu, C.W., & Chang, P.C. (2011). Fuzzy Delphi method for evaluating hydrogen production technologies. *International Journal of Hydrogen Energy*, 36, 14172-14179.

Chen, C.T. (2010). Exploring an industry-based basic technological competence indicator system of electrical technology for students at a technological institute. *World Transactions on Engineering and Technology Education*, 8(4), 542-551.

Chen, K.M., & Lin, T.S. (2010). Copper pillar bump design optimization for lead free flip-chip packaging. *Journal of Materials Science: Materials in Electronics*, 21(3), 278-284.

Cheng, K.C., & Lin, F.L. (2003). *A study on the analysis of competitive strategy of flip chip packaging insdustry in Taiwan*. Master Thesis of the National Sun Yat-Sen University, Kaohsiung, Taiwan.

Cho, S., Cho, S., & Lee, J.Y. (2008). Estimation of warpage and thermal stress of IVHs in flip-chip ball grid arrays package by FEM. *Microelectronics Reliability*, 48(2), 300-309.

Dalkey, N.C. (1969). *The Delphi method: an experimental study of group opinion*. The Rand Corporation, RM-5888-PR, Santa Monica, California.

Datta, M., Osaka, T., & Schultze, J.W. (2005). *Microelectronic packaging*. CRC Press.

Evans, R.J., Scearce, S., & Hsieh, M. (2008). An industry-oriented curriculum in the design and performance of electrical packaging and interconnect. *17th Conference on Electrical Performance of Electronic Packaging* (pp.353-56), San Jose, CA, United States.

Hartman, F.T., & Baldwin, A. (1995). Using technology to improve Delphi method. *Journal of Computing in Civil Engineering*, 9(4), 244-249.

Hsu, L. (2011). Indicators of English communicative competence for EFL learners in Taiwan-a fuzzy Delphi method. *International Journal of Current Research*, 3(4), 223-230.

Hsu, Y.L., Lee, C.H., & Kreng, V.B. (2010). The application of fuzzy Delphi method and fuzzy AHP in lubricant regenerative technology selection. *Expert Systems with Applications*, 37(1), 419-425.

Huang, H.N., Liao, Y.C., Tseng, W.T., Lin, C.T., & Chiu, C.H. (2011). Study of underfill material for fine pitch Cu pillar bump. *6th International Microsystems, Packaging, Assembly and Circuits Technology Conference* (pp.150-52), Taipei, Taiwan.

Imanova, S.N. (2009). Service quality evaluation by fuzzy Deplhi method. *2009 International Conference on Application of Information and Communication Technologies*, Baku, Azerbaijan.

Jen, Y.M., Chiou, Y.C., & Yu, C.L. (2011). Fracture mechanics study on the intermetallic compound cracks for the solder joints of electronic packages. *Engineering Failure Analysis*, 18(2), 797-810.

Joshi, Y., Pecht, M., & Nakayama, W. (1997). Electronic packaging and reliability education for the 21st century: The University of Maryland CALCE EPRC program. *Proceedings of the 1997 47th IEEE Electronic Components* (pp.585-88), San Jose, CA, USA.

Kaufmann, A., & Gupta, M.M. (1988). *Fuzzy mathematical models in engineering and management science*. New York: North-Holland.

Kuo C.G., Huang, C.H., & Tsay, H.J. (2011). The study of construction of the core competencies in the precision casting industry. *International Journal of Technology and Engineering Education*, 8(1), 9-15.

Kuo, Y.F., & Chen, P.C. (2008). Constructing performance appraisal indicators for mobility of the service industries using fuzzy Delphi method. *Expert Systems with Applications*, 35(4), 1930-1939.

Lau, J.H. (2000). *Low cost flip chip technologies*. New York: McGraw-Hill.

Lay Yeap, L. (2010). Meeting the assembly challenges in new semiconductor packaging trend. *34th International Electronics Manufacturing Technology Conference*, Melaka, Malaysia.

Lee, S.H., Lee, H.J., Kim, J.M., & Shin, Y.E. (2011). Dynamic filling characteristics of a capillary driven underfill process in flip-chip packaging. *Materials Transactions*, 52(10), 1998-2003.

Lee, T.K., Zhang, S., Wong, C.C., & Tan, A.C. (2009). Assessment of fluxless solid liquid interdiffusion bonding by compressive force of Au-PbSn and Au-SAC for flip chip packaging. *IEEE Transactions on Advanced Packaging*, 32(1), 116-122.

Lin, C.M., Chu, C.Y., & Chang, W.L. (2008). Underfill injection molding in flip-chip packaging with different bumps array arrangements. *2007 SME International Conference on Advanced Manufacture* (pp.163-68), Tainan, Taiwan.

Lin, S.T., & Gary Hu, G. (2001). *IC packaging core competence constructed model*. Master Thesis of the National Sun Yat-Sen University, Kaohsiung, Taiwan.

Lo, C.L., & Tung, L.R. (1997). Integrated circuit packaging industry in Taiwan. IEEE Transactions on Components. *Packaging and Manufacturing Technology: Part C Manufacturing*, 20(4), 243-255.

Mallen, C., Adams, L., Stevens, J., & Thompson, L. (2010). Environmental sustainability in sport facility management: a Delphi study. *European Sport Management Quarterly*, 10(3), 367-389.

Ministry of Education (2009). *Project of excellent manpower cultivation to improve employment*. Taipei: Ministry of Education.

Ministry of Education (2010). *Implement ideas of education and polices*. Taipei: Ministry of Education.

Murry, T.J., Pipino, L.L., & Gigch, J.P. (1985). A pilot study of fuzzy set modification of Delphi. *Human Systems Management*, 5(1), 76-80.

Nijkamp, P., Siedschlag, I., & Smith, D. (2011). *Economic growth, innovation and competitiveness in a knowledge-based world economy: introduction*. Berlin Heidelberg: Springer-Verlag.

Nworie, J. (2011). Using the Delphi technique in educational technology research. *TechTrends*, 55(5), 24-30.

Okoli, C., & Pawlowski, S.D. (2004). The Delphi method as a research tool: an example, design considerations and applications. *Information and Management*, 42(1), 15-29.

Olson, C.A., Tooman, T.R., & Leist, J.C. (2005). Contents of a core library in continuing medical education: a Delphi study. *The Journal of Continuing Education in the Health Professions*, 25, 278-288.

Orii, Y., Toriyama, K., Noma, H., Oyama, Y., Nishiwaki, H., Ishida, M., Nishio, T., C.labianca, N., & Feger, C. (2009). Ultrafine-pitch C2 flip chip interconnections with solder-capped Cu pillar bumps. *59th Electronic Components and Technology Conference* (pp.948-53), San Diego, CA, United States.

Pan, K., Yang, D., Kai, Q., Zhang, K., & Yang, L. (2008). Introduction of microelectronics manufacturing engineering into professional education: a joint effort among industry, government and universities. *2008 International Conference on Electronic Packaging Technology and High Density Packaging*, Shanghai, China.

Rychen, D.S., & Salganik, L.H. (2003). *Key competencies for a successful life and a well-functioning society*. Gtingen: Hogrefe & Huber Publishers.

Syyr, W.J. (2012). Development of working competence items for mechatronics with graphical monitoring and control.. *Computer Applications in Engineering Education*, 20(1), 88-99.

Shyr, W.J. (2012). Industry-oriented competency requirements for mechatronics technology in Taiwan. *The Turkish Online Journal of Educational Technology*, 11(4), 195-203.

Skulmoski, G.J., Hartman, F.T., & Krahn, J. (2007). The Delphi method for graduate research. *Journal of Information Technology Education*, 6, 1-21.

Spencer, L.M., & Spencer, S. (1993). *Competence at work: models for superior performance*. New York: John Wiley & Sons.

Suzuki, Y., Kayashima, Y., Maeda, T., Matsuura, Y., Sekiguchi, T., & Watanabe, A. (2007). Development of thin flip-chip BGA for package on package. *57th Electronic Components and Technology Conference* (pp.8-14), Sparks, NV, United States.

Tsai, M.Y., Chang, H.Y., & Pecht, M. (2009). Warpage analysis of flip-chip PBGA packages subject to thermal loading. *IEEE Transactions on Device and Materials Reliability*, 9(3), 419-424.

Tsai, M.Y., & Chang, H.Y. (2008). Warpage measurement and simulation of flip-chip PBGA package under thermal loading. *10th International Conference on Electronic Materials and Packaging* (pp.145-48), Taipei, Taiwan.

Wan, J.W., Zhang, W.J., & Bergstrom, D.J. (2007). Recent advances in modeling the underfill process in flip-chip packaging. *Microelectronics Journal*, 38(1), 67-75.

WEEE (2002). European Union Waste in Electrical and Electronic Equipment Directive. *WEEE Directive*. http://en.wikipedia.org/wiki/Restriction_of_Hazardous_Substances_Directive.

Wikipedia (2012). *Core competency*. http://en.wikipedia.org/wiki/Core_competency#Core_Competence.

Williams, K.L. (2004). Delivering innovative solutions to the growing and changing needs of the packaging industry. *International Conference on Polyolefins 2004* (pp.317-29), Houston, TX, United States.

Xia, B., & Chan, A.P.C. (2012). Measuring complexity for building projects: a Delphi study. *Engineering, Construction and Architectural Management*, 19(1), 7-24.

Yan, K.L. (2005). Higher continuing education for professionals in electronics industry. *6th International Conference on Information Technology Based Higher Education and Training* (pp.8-16), Juan Dolio, Dominican Republic.

Yang, C., & Young, W.B. (2012). The effective permeability of the underfill flow domain in flip-chip packaging. *Applied Mathematical Modelling* (in press).

Yang, D.G., Pan, K.L., Ma, X.S., & Wei, L.P. (2007). University education program on microelectronics packaging and assembly: facing the challenging of fast developing electronics industry. *7th International Conference on Electronics Packaging Technology*, Shanghai, China.

Yang, X., Soh, Y.C., & Wu, H. (2010). Packaging challenges on shrink chip technology. *China Semiconductor Technology International Conference 2010* (pp.915-21), Shanghai, China.

Yuan, X.Z., Lihua, L., Yangjian, X., Yong, L., Irving, S., & Timwah, L. (2007). Highly efficient modeling automation for electronic package thermal analysis. *57th Electronic Components and Technology Conference* (pp.1931-35), Sparks, NV, United States.

Zhang, X.R., Zhu, W.H., Liew, B.P., Gaurav, M., Yeo, A., & Chan, K.C. (2010). Copper pillar bump structure optimization for flip chip packaging with Cu/Low-K stack. *11th International Conference on Thermal, Mechanical and Multi-Physics Simulation, and Experiments in Microelectronics and Microsystems*, Bordeaux, France.

Zhang, Y., Liang, L., Xia, Y., Liu, Y., Irving, S., & Luk, T. (2008). Thermal analysis automation system for semiconductor package. *International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Micro-Systems*, Freiburg im Breisgau, Germany.