DOCUMENT RESUME

ED 246 222 CE 039 207

TITLE	Electronic Principles VII, 7-11. Military Curriculum Materials for Vocational and Technical Education.
INSTITUTION	Air Force Training Command, Keesler AFB, Miss.; Ohio State Univ., Columbus. National Center for Research in Vocational Education.
SPONS AGENCY	Department of Education, Washington, DC.
PUB DATE	75
NOTE	170p.; For related documents, see CE 039 201-210.
PUB TYPE	Guides - Classroom Use - Materials (For Learner) (051) -- Guides - Classroom Use - Guides (For Teachers) (052)
EDRS PRICE	MF01/PC07 Plus Postage.
DESCRIPTORS	Behavioral Objectives; *Computation; *Computers; Course Content; Course Descriptions; *Data Processing; *Electric Circuits; *Electronic Equipment; *Electronics; Individualized Instruction; Learning Activities; Learning Modules; Mathematics; Number Systems; Pacing; Postsecondary Education; Programed Instructional Materials; Secondary Education; *Technical Education
IDENTIFIERS	Military Curriculum Project

ABSTRACT

This seventh of 10 blocks of student and teacher materials for a secondary/postsecondary level course in electronic principles comprises one of a number of military-developed curriculum packages selected for adaptation to vocational instruction and curriculum development in a civilian setting. Prerequisites are the previous blocks. This block on digital techniques contains five modules covering 35 hours of instruction on numbering systems and mathematical computations (7 hours); logic functions and boolean equations (7); logic circuits and diagrams (8); counters, registers, and storage devices (7); and digital/analog converters (6). Printed instructor materials include a plan of instruction detailing the units of instruction, duration of the lessons, criterion objectives, and support materials needed. Student materials include a student text and five guidance packages containing objectives, assignments, review exercises, and answers for each module. A digest of the modules in the block is provided for students who need only to review the material. Designed for self- or group-paced instruction, the material can be adapted for individualized instruction. Additional print and audiovisual materials are recommended but not provided. (YLB)

MILITARY CURRICULUM MATERIALS

The military-developed curriculum materials in this course package were selected by the National Center for Research in Vocational Education Military Curriculum Project for dissemination to the six regional Curriculum Coordination Centers and other instructional materials agencies. The purpose of disseminating these courses was to make curriculum materials developed by the military more accessible to vocational educators in the civilian setting.

The course materials were acquired, evaluated by project staff and practitioners in the field, and prepared for dissemination. Materials which were specific to the military were deleted, copyrighted materials were either omitted or approval for their use was obtained. These course packages contain curriculum resource materials which can be adapted to support vocational instruction and curriculum development.

The National Center Mission Statement

The National Center for Research in Vocational Education's mission is to increase the ability of diverse agencies, institutions, and organizations to solve educational problems relating to individual career planning, preparation, and progression. The National Center fulfills its mission by:

- Generating knowledge through research
- Developing educational programs and products
- Evaluating individual program needs and outcomes
- Installing educational programs and products
- Operating information systems and services
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FOR FURTHER INFORMATION ABOUT
Military Curriculum Materials
WRITE OR CALL

Program Information Office
The National Center for Research in Vocational Education
The Ohio State University
1960 Kenny Road, Columbus, Ohio 43210
Telephone: 614/486-3655 or Toll Free 800/848-4815 within the continental U.S. (except Ohio)

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Tel: (614) 486-3655
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Military Curriculum Materials for Vocational and Technical Education

Information and Field Services Division

The National Center for Research in Vocational Education

Military Curriculum Materials Dissemination Is . . .

an activity to increase the accessibility of military-developed curriculum materials to vocational and technical educators.

This project, funded by the U.S. Office of Education, includes the identification and acquisition of curriculum materials in print form from the Coast Guard, Air Force, Army, Marine Corps and Navy.

Access to military curriculum materials is provided through a "Joint Memorandum of Understanding" between the U.S. Office of Education and the Department of Defense.

The acquired materials are reviewed by staff and subject matter specialists, and courses deemed applicable to vocational and technical education are selected for dissemination.

The National Center for Research in Vocational Education is the U.S. Office of Education's designated representative to acquire the materials and conduct the project activities.

Project Staff:

Wesley E. Budke, Ph.D., Director
National Center Clearinghouse

Shirley A. Chase, Ph.D.
Project Director

What Materials Are Available?

One hundred twenty courses on microfiche (thirteen in paper form) and descriptions of each have been provided to the vocational Curriculum Coordination Centers and other instructional materials agencies for dissemination.

Course materials include programmed instruction, curriculum outlines, instructor guides, student workbooks and technical manuals.

The 120 courses represent the following sixteen vocational subject areas:

- Agriculture
- Aviation
- Building & Construction Trades
- Clerical Occupations
- Communications
- Drafting
- Electronics
- Engine Mechanics
- Food Service
- Health
- Heating & Air Conditioning
- Machine Shop
- Management & Supervision
- Meteorology & Navigation
- Photography
- Public Service

The number of courses and the subject areas represented will expand as additional materials with application to vocational and technical education are identified and selected for dissemination.

How Can These Materials Be Obtained?

Contact the Curriculum Coordination Center in your region for information on obtaining materials (e.g., availability and cost). They will respond to your request directly or refer you to an instructional materials agency closer to you.

CURRICULUM COORDINATION CENTERS

EAST CENTRAL
Rebecca S. Douglass
Director
100 North First Street
Springfield, IL 62777
217/782-0759

NORTHWEST
William Daniels
Director
Building 17
Airdustrial Park
Olympia, WA 98504
206/753-0879

MIDWEST
Robert Patton
Director
1515 West Sixth Ave.
Stillwater, OK 74704
405/377-2000

SOUTHEAST
James F. Shill, Ph.D.
Director
Mississippi State University
Drawer DX
Mississippi State, MS 39762
601/325-2510

NORTHEAST
Joseph F. Kelly, Ph.D.
Director
225 West State Street
Trenton, NJ 08625
609/292-6562

WESTERN
Lawrence F. H. Zane, Ph.D.
Director
1776 University Ave.
Honolulu, HI 96822
808/948-7834

ELECTRONICS PRINCIPLES VII

Table of Contents

ELETRONIC PRINCIPLES VII

Classroom Course

Developed by:

United States Air Force

Development and Review Dates

November 7, 1975

D.O.T. No.:
003.081

Occupational Area:
Electronics

Target Audiences:
Grades 11-adult

Print Pages:
160

Cost:
$3.25

Availability:
Military Curriculum Project, The Center for Vocational Education, 1960 Kenny Rd., Columbus, OH 43210

Contents:	Type of Materials: Lesson Plans:	Programmed Text:	Student Workbook:	Handouts:	Text Materials:	Audio-Visuals:	Instructional Design: Performance Objectives:	Tests:	Review Exercises:	Additional Materials Required:	Type of Instruction: Group Instruction:	Individualized:
			No. of pages									
Block VII — *Digital Techniques*												
Module 51 — Numbering Systems and Mathematical Computations	•		15		•		•	★	•		•	•
Module 52 — Logic Functions and Boolean Equations	•		14		•	★	•	★	•		•	•
Module 53 — Logic Circuits and Diagrams	•		10		•		•	★	•		•	•
Module 54 — Counters, Registers, and Storage Devices	•		13		•		•	★	•		•	•
Module 55 — Digital/Analog Converters	•		8		•		•	★	•		•	•

★ Materials are recommended but not provided.

Expires July 1, 1978

Course Description

This block is the seventh in a ten-block course providing training in electronic principles, use of basic test equipment, safety practices, circuit analysis, soldering, digital techniques, microwave principles and troubleshooting basic circuits. Prerequisites to this block are Blocks I through VI covering DC circuits, AC circuits, RCL circuits, solid state principles, solid state power supplies and amplifiers, and solid state wave generating and wave shaping circuits. Block VII—*Digital Techniques* contains five modules covering 35 hours of instruction over numbering systems, mathematical computations, logic functions, boolean equations, logic circuits and diagrams, counters, registers, and digital/analog converters. The module topics and respective hours follow:

Module 51 – **Numbering Systems and Mathematical Computations** (7 hours)
Module 52 – **Logic Functions and Boolean Equations** (7 hours)
Module 53 – **Logic Circuits and Diagrams** (8 hours)
Module 54 – **Counters, Registers, and Storage Devices** (7 hours)
Module 55 – **Digital/Analog Converters** (6 hours)

This block contains both teacher and student materials. Printed instructor materials include a plan of instruction detailing the units of instruction, duration of the lessons, criterion objectives, and support materials needed. Student materials consist of a student text used for all the modules; five guidance packages containing objectives, assignments, review exercises and answers for each module; and a digest of modules 51 through 55 for students who have background in these topics and only need to review the major points of instruction.

This material is designed for self- or group-paced instruction to be used with the remaining nine blocks. Most of the materials can be adapted for individualized instruction. Some additional military manuals and commercially produced texts are recommended for reference, but are not provided. Audiovisuals suggested for use with the entire course consit of 143 videotapes which are not provided.

ROI 3AQR30020-1

PLAN OF INSTRUCTION
(Technical Training)

ELECTRONIC PRINCIPLES

(Modular Self-Paced)

KEESLER TECHNICAL TRAINING CENTER

4 December 1975 - Effective 6 January 1976 with Class 760106

Volume 7

7-11

ATC Keesler 4-2148

DEPARTMENT OF THE AIR FORCE
USAF Sch of Applied Aerosp Sci (ATC)
Keesler Air Force Base, Mississippi 39534

PLAN OF INSTRUCTION 3AQR30020-1
4 December 1975

FOREWORD

1. PURPOSE: This publication is the plan of instruction (POI) when the pages shown on Page A are bound into a single document. The POI prescribes the qualitative requirements for Course Number 3AQR30020-1, Electronic Principles (Modular self-paced) in terms of criterion objectives and teaching steps presented by modules of instruction and shows duration, correlation with the training standard, and support materials and guidance. When separated into modules of instruction, it becomes Part I of the lesson plan. This POI was developed under the provisions of ATCR 50-5, Instructional System Development, and ATCR 52-7, Plans of Instruction and Lesson Plans.

2. COURSE DESIGN/DESCRIPTION. The instructional design for this course is Modular Scheduling and Self-Pacing; however, this POI can also be used for Group Pacing. The course trains both non-prior service airmen personnel and selected re-enlistees for subsequent entry into the equipment oriented phase of basic courses supporting 303XX, 304XX, 305XX, 307XX, 309XX and 328XX AFSCs. Technical Training includes electronic principles, use of basic test equipment, safety practices, circuit analysis, soldering, digital techniques, microwave principles, and troubleshooting of basic circuits. Students assigned to any one course will receive training only in those modules needed to complement the training program in the equipment phase. Related training includes traffic safety, commander's calls/briefings and end of course appointments.

3. TRAINING EQUIPMENT. The number shown in parentheses after equipment listed as Training Equipment under SUPPORT MATERIALS AND GUIDANCE is the planned number of students assigned to each equipment unit.

4. REFERENCES: This plan of instruction is based on Course Training Standard KE52-3AQR30020-1, 27 June 1975 and Course Chart 3AQR30020-1, 27 June 1975.

FOR THE COMMANDER

W. H. HORNE, Colonel, USAF
Commander
Tech Tng Gp Prov, 3395

OPR: Tech Tng Gp Prov, 3395
DISTRIBUTION: Listed on Page A

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PLAN OF INSTRUCTION/LESSON PLAN PART I

NAME OF INSTRUCTOR	COURSE TITLE
	Electronic Principles

BLOCK NUMBER	BLOCK TITLE
VII	Digital Techniques

1 COURSE CONTENT	2 DURATION (Hours)
1. Numbering Systems and Mathematical Computations (Module 51)	7 (5/2)

a. Given a decimal number (not to exceed four digits), convert to its equivalent octal and binary value. CTS: 7a Meas: W

(1) Applications in functional areas.

(2) Basic differences between analog and digital data equipment.

(3) Use of decimal, binary, and octal numbers.

(4) Given a number in the decimal, binary, or octal system identify the

(a) integral portion.

(b) place holder.

(c) point.

(d) LSD.

(e) MSD.

(f) radix.

(g) value of each digit.

(5) Given the conversion rules and examples, convert a decimal number to its equivalent

(a) octal value.

(b) binary value.

SUPERVISOR APPROVAL OF LESSON PLAN (PART II)

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ATC FORM APR 75 133 ATC Kessler 6-1029 REPLACES ATC FORMS 337, MAR 73, AND 770, AUG 72, WHICH WILL BE USED.

PLAN OF INSTRUCTION/LESSON PLAN PART I (Continuation Sheet)

COURSE CONTENT

b. Given an octal number (not to exceed four digits), convert to its equivalent decimal and binary value. CTS: 7a Meas: W

(1) Given the rules of conversion and examples, convert an octal number to its equivalent

(a) decimal value.

(b) binary value.

c. Given a binary number (not to exceed four digits), convert to its equivalent octal and decimal value. CTS: 7a Meas: W

(1) Given the rules of conversion and examples, convert a binary number to its equivalent

(a) decimal value.

(b) octal value.

d. Given an octal addition problem (not to exceed two rows of four digit numbers), solve for the sum. CTS: 7a Meas: W

(1) Given the rules for octal addition and examples, solve problems for the sum.

e. Given an octal subtraction problem (not to exceed four digits per line), solve for the difference. CTS: 7a Meas: W

(1) Given the rules for octal subtraction and examples, solve problems for the difference.

f. Given a binary addition problem (not to exceed three rows of five digits), solve for the sum. CTS: 7a Meas: W

(1) Given the rules for binary addition and examples, solve problems for the sum.

g. Given a binary subtraction problem (not to exceed two rows of five digits), solve for the difference using the direct method or by complementing and adding. CTS: 7a Meas: W

(1) Given the rules for binary subtraction and examples, solve problems for the difference.

SUPPORT MATERIALS AND GUIDANCE

Student Instructional Materials
KEP-GP-51, Numbering Systems and Mathematical Computations
KEP-ST-VII, Digital Techniques
KEP-110, Electronics Handbook
KEP-ST/Digest VII, Digests (Modules 51-55)

Training Methods
Discussion (5 hrs) and/or Programmed Self Instruction
CTT Assignments (2 hrs)

Instructional Guidance
Assign specific objectives to be completed during CTT time in KEP-GP-51. Students identified as being deficient in mathematical ability need special attention and should be given additional practice on the objectives.

PLAN OF INSTRUCTION/LESSON PLAN PART I

NAME OF INSTRUCTOR	COURSE TITLE
	Electronic Principles

BLOCK NUMBER	BLOCK TITLE
VII	Digital Techniques

1 COURSE CONTENT	2 DURATION (Hours)
2. Logic Functions and Boolean Equations (Module 52)	7 (5/2)

a. Given the AND logic symbol with two inputs, construct the truth table. CTS: 7b Meas: W

(1) Define LOGIC and explain in terms of

(a) digital pulse trains.

(b) logic gates.

(c) processing data flow by the use of logic gates.

(2) Define AND logic and explain in terms of

(a) AND gate.

(b) AND logic symbol.

(c) diode circuitry.

(d) truth table.

b. Given the OR logic symbol with two inputs, construct the truth table. CTS: 7b Meas: W

(1) Define OR logic and explain in terms of

(a) OR gate.

(b) OR logic symbol.

(c) diode circuitry.

(d) truth table.

SUPERVISOR APPROVAL OF LESSON PLAN (PART II)

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PLAN OF INSTRUCTION/LESSON PLAN PART I (Continuation Sheet)

COURSE CONTENT

c. Given the AND or OR logic symbols with state indicators, construct the truth table. CTS: 7b Meas: W

(1) Define "state indicator."

(2) Explain NOT logic.

(3) Explain NOT AND (NAND) gate operation in terms of

(a) NAND logic symbol.

(b) diode and transistor circuitry.

(c) truth table.

(4) Explain NOT OR (NOR) gate operation in terms of

(a) NOR logic symbol.

(b) diode and transistor circuitry.

(c) truth table.

d. Given the exclusive OR logic symbol with two inputs, construct the truth table. CTS: 7b Meas: W

(1) Define "exclusive OR."

(2) Explain operation in terms of

(a) logic symbols.

(b) truth table.

e. Given the direct coupled transistor logic (DCTL) circuitry of a series and parallel logic gate (not to exceed three inputs), draw the logic symbol for each gate. CTS: 7c Meas: W

(1) Define the term "DCTL."

(2) Explain operation of a series DCTL circuit in terms of

(a) logic symbol.

(b) transistor circuitry.

(c) truth table.

(3) Explain operation of a parallel DCTL circuit in terms of

(a) logic symbol.

COURSE CONTENT

(b) transistor circuitry.

(c) truth table.

f. Given a current mode logic circuit (CML), construct the truth table. CTS: 7b Meas: W

(1) Define the term CML.

(2) Explain operation in terms of

(a) logic symbol.

(b) transistor circuitry.

(c) truth table.

g. Given a Boolean equation, draw the logic diagram (consisting of three to six gates). CTS: 7c Meas: W

(1) Define Boolean algebra.

(2) Give the symbols used in Boolean algebra.

(3) Explain the rules and give examples of how to write a Boolean equation, given a logic diagram of three to six gates.

(4) Explain the rules and give examples of how to draw the logic diagram, given a Boolean expression.

SUPPORT MATERIALS AND GUIDANCE

Student Instructional Materials
KEP-GP-52, Logic Functions and Boolean Equations
KEP-ST-VII
KEP-110

Audio Visual Aids
TVK-30-15, Two Input AND Gate

Training Methods
Discussion (5 hrs), and/or Programmed Self Instruction
CTT Assignments (2 hrs)

Instructional Guidance

Assign specific objectives to be completed during CTT time in KEP-GP-52. Students recognize the symbol for a state indicator, but few really know what it signifies. Students should be aware that a state indicator does exactly what its name implies - it signifies a low level or state. Do not teach the state indicator as always signifying inversion. Students experience considerable difficulty satisfying the requirements for objectives 2e and 2f. Special attention from the instructor is required in these areas. Teach the student to first consider the logic operation and then the input and output level.

PLAN OF INSTRUCTION/LESSON PLAN PART I

NAME OF INSTRUCTOR	COURSE TITLE
	Electronic Principles
BLOCK NUMBER	**BLOCK TITLE**
VII	Digital Techniques

1 COURSE CONTENT	2 DURATION (Hours)
3. Logic Circuits and Diagrams (Module 53)	8 (6/2)

a. Given a logic diagram of a serial half or full adder, write all possible sum and carry expressions. CTS: 7e Meas: W

(1) Review binary addition.

(2) Explain the purpose and need for binary adders.

(3) Explain the operation of a serial half adder in terms of

(a) logic diagram.

(b) sum expressions

(c) carry expressions.

(4) Explain the operation of a serial full adder in terms of

(a) logic diagram.

(b) sum expressions.

(c) carry expressions.

b. Given a logic diagram of a 4-bit input parallel full adder, trace data flow and write the state of each sum and carry output. CTS: 7e Meas: W

(1) Explain operation in terms of

(a) inputs.

(b) logic diagram.

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(c) data flow.

(d) state of each sum output for a given input.

(e) state of carry output for a given input.

c. Given a schematic diagram containing a two input AND gate, differentiating network, clipping diode, and set or clear input, identify the correct output waveshape for a given input. CTS: 7e Meas: W

(1) Explain the purpose of the circuit.

(2) Explain operation in terms of the

(a) AND gate.

(b) clipping diode.

(c) differentiating network.

(d) set and clear network.

(e) output waveforms.

d. Given schematic diagram of a flip-flop, and Schmitt Trigger; identify the logic symbols and trace data flow. CTS: 7e Meas: W

(1) Review and give main uses for the

(a) astable multivibrator.

(b) bistable multivibrator.

(c) monostable multivibrator.

(2) Give logic symbols for the monostable (single shot) and bistable (flip-flop) multivibrator.

(3) Define flip-flop and explain operation in terms of

(a) logic symbol.

(b) inputs.

(c) transistor circuitry.

(d) outputs when flip-flop is in the 1 state.

(e) outputs when flip-flop is in the 0 state.

COURSE CONTENT

(4) Identify the schematic diagram of a Schmitt trigger and explain operation in terms of

(a) uses.

(b) stable states.

(c) biasing.

(d) transistor circuitry.

(e) output waveform for a given input.

(f) logic symbol.

e. Given a logic symbol of a J-K flip-flop, construct the truth table. CTS: 7b Meas: W

(1) Define J-K flip-flop and give the logic symbol.

(2) Explain operation in terms of

(a) uses.

(b) state of the flip-flop for a J input.

(c) state the flip-flop for a K input.

(d) state of the flip-flop with trigger but no J or K input.

(e) truth table.

SUPPORT MATERIALS AND GUIDANCE

Student Instructional Materials
KEP-GP-53, Logic Circuits and Diagrams
KEP-ST-VII
KEP-110

Training Methods
Discussion (6 hrs) and/or Programmed Self Instruction
CTT Assignments (2 hrs)

Instructional Guidance
Insure that students are assigned specific objectives in KEP-GP-53 to be completed during CTT time. Students have difficulty writing the sum and carry expressions for the output of a full adder. They should be shown how to derive a truth table for a full adder, and from the truth table how to extract the sum and carry expressions. This procedure is discussed in the student text. For students experiencing difficulty with objective 3b show them the shortcut method. Emphasize the study of the J-K flip-flop since it is used extensively in digital circuitry.

PLAN OF INSTRUCTION/LESSON PLAN PART I

NAME OF INSTRUCTOR	COURSE TITLE
	Electronic Principles

BLOCK NUMBER	BLOCK TITLE
VII	Digital Techniques

1 COURSE CONTENT	2 DURATION (Hours)
4. Counter, Registers, and Storage Devices (Module 54)	7 (5/2)

a. Given a four-stage upcounter or downcounter logic diagram, trace data flow and write in the binary count after a clear pulse and a given clock pulse has passed. CTS: 7e Meas: W

(1) Review the logic symbol for a flip-flop.

(2) Explain the operation of a flip-flop in terms of

(a) state of flip-flop with SET input.

(b) state of flip-flop with RESET input.

(c) state of flip-flop with CLOCK PULSE or TRIGGER input.

(d) outputs in ONE state and ZERO state.

(3) Trace data flow in a four-stage upcounter or down-counter.

(4) Write in the binary count after a CLEAR PULSE and a given CLOCK PULSE has passed.

b. Given the logic diagram of a decade counter, trace data flow to construct the truth table. CTS: 7b, 7e Meas: W

c. Given a logic diagram of a four-stage ring counter and a number of input pulses, write the correct state of each flip-flop. CTS: 7e Meas: W

d. Given the logic diagram of a count detect circuit, select the AND gate connections to indicate a required count. CTS: 7e Meas: W

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PLAN OF INSTRUCTION/LESSON PLAN PART I (Continuation Sheet)

COURSE CONTENT

e. Given the logic diagram of a serial upcounter with a given count feeding a parallel storage register, trace data flow and write the binary count stored in the register after a read-in pulse has passed. CTS: 7e Meas: W

f. Given a three-stage shift register diagram and a given count, trace data flow and write the state of each flip-flop after a specified number of shift pulses have passed. CTS: 7e Meas: W

g. Given the logic symbols of an amplifier, a time delay, a shift register, and a storage register, identify each symbol. CTS: 7e Meas: W

h. Match the following list of magnetic storage devices to the statement which describes their functional characteristics: Tape; Drum; Core. CTS: 7e Meas: W

SUPPORT MATERIALS AND GUIDANCE

Student Instructional Materials
KEP-CP-54, Counters, Registers, and Storage Devices
KEP-ST-VII
KEP-110

Training Methods
Discussion (5 hrs) and/or Programmed Self Instruction
CTT Assignments (2 hrs)

Instructional Guidance
Have students complete necessary objectives during CTT time. Some students have problems in determining the LSD position of a counter. They also have difficulty in identifying the various types of counter circuits and understanding why a serial register is needed.

PLAN OF INSTRUCTION/LESSON PLAN PART I

NAME OF INSTRUCTOR	COURSE TITLE
	Electronic Principles

BLOCK NUMBER	BLOCK TITLE
VII	Digital Techniques

1 COURSE CONTENT	2 DURATION (Hours)
5. Digital/Analog Converters (Module 55)	6 (5/1)

a. Given a circuit diagram of an electromechanical digital-to-analog converter, write the output voltage for a specified count in the counter. CTS: 7d Meas: W

(1) Explain the need and purpose of a digital-to-analog conversion.

(2) Explain operation of an electromechanical digital-to-analog converter in terms of

(a) ladder control circuit.

(b) buffer relays.

(c) counter connections.

(d) converting the count in the counter (digital) to an output voltage (analog).

b. Given a circuit diagram of an analog-to-digital converter using variable time conversion, select the portions of the circuit that perform the sample, hold, compare and digitize functions. CTS: 7d Meas: W

(1) Explain the need and purpose of an analog-to-digital converter

(2) Explain operation in terms of

(a) schematic and logic diagram

(b) variable time conversion

(c) sample function

SUPERVISOR APPROVAL OF LESSON PLAN (PART II)

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ATC FORM APR 75 133 ATC Keesler 6-1029 REPLACES ATC FORMS 337, MAR 73, AND 770, AUG 72, WHICH WILL BE USED.

(d) hold function

(e) compare function

(f) digitize function

6. Measurement and Critique 1

a. Measurement test

b. Test critique

SUPPORT MATERIALS AND GUIDANCE

Student Instructional Materials
KEP-GP-55, Digital/Analog Converters
KEP-ST-VII
KEP-110

Training Methods
Discussion (5 hrs) and/or Programmed Self Instruction
CTT Assignments (1 hr)

Instructional Guidance
Assign specific objectives to be completed during CTT time for the next module each student will enter. Make certain the student knows how to use the formula

$$\frac{\text{COUNT IN COUNTER}}{\text{MAXIMUM POSSIBLE COUNT}} \times \text{SUPPLY VOLTAGE} = \text{OUTPUT VOLTAGE.}$$

Some students rush through objective 5b because it is the last one for this measurement unit. Insure that the student is familiar with the analog-to-digital converter circuit shown in the text.

Prepared by Keesler ITC
KEP-ST-VII

Technical Training

Electronic Principles (Modular Self-Paced)

Volume VII

DIGITAL TECHNIQUES

March 1976

AIR TRAINING COMMAND

7-11

Designed For ATC Course Use

DO NOT USE ON THE JOB

Radar Principles Branch
Keesler Air Force Base, Mississippi

ATC ST 3AQR3X020-X
KEP-ST-VII
March 1976

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ELECTRONIC PRINCIPLES

VOLUME VII

DIGITAL TECHNIQUES

This student text is the prime source of information for achieving the objectives of this block of instruction. This training publication is designed for training purposes only and should not be used as a basis for job performance in the field.

CONTENTS

Supersedes KEP-ST-VII, October 1975; stock on hand will be used.

CHAPTER 1

NUMBERING SYSTEMS AND MATHEMATICAL COMPUTATIONS

1-1. Introduction

1-2. The modern Air Force needs fast and efficient methods of processing information. How does it handle records and statistics and analyze data with such speed and accuracy? Electronic data processing equipment is the answer. Electronic computers use digital techniques to improve data flow.

1-3. There are two major classifications of computers or data processing equipment: analog and digital.

1-4. The analog data processing device operates on the principle of converting a voltage, current, resistance value, or certain increments of an angular change into an integrated result. For example, a specific voltage value can be used to deflect a needle in a calibrated movement, through generator action, which will indicate resultant speed, fuel level, or light intensity. The basic principle is simple. In an automobile, the speedometer is actually a tiny generator which is driven by a cable connected to a drive gear in the car's transmission. A needle connected to the armature of this tiny generator moves to indicate miles (or kilometers) per hour. Thus, the indicated speed is proportional to the number of revolutions per unit of time of the cable and the overall accuracy of the entire system. Another example of an analog computer is the slide rule. Since an analog computer can perform only that function for which it is designed, the slide rule like other analog computers is only as accurate as the exactness of the measurement of its scale. Thus, it is ideally suited for certain engineering applications, but is unsuitable for many of the calculations performed in this new space age. Therefore, it is rapidly being replaced by the more sophisticated electronic calculator.

1-5. The digital computer, on the other hand, processes "digits" of information. By digits we mean small increments or units of information. The digital computer accepts information in the form of coded alphabetical and numerical characters and processes this information according to a predetermined instruction sequence that can be varied as required.

1-6. Examples of simple digital processing devices are found in automobiles that have telltale oil pressure and engine temperature warning systems. A sensor unit is used in each system to monitor the oil pressure and the engine temperature. If the oil pressure or the temperature is normal, the sensors act like open switches and the circuits of both telltale lamps are open. When the oil pressure is low, the sensor switch closes and the oil pressure lamp comes on. If the temperature is high, the temperature sensor closes and the temperature light comes on. A secondary alert system, found on some cars, activates a buzzer when the engine temperature has exceeded an undesired degree to warn the driver if he does not notice the lamp or if the lamp is defective. Notice that in these examples, a lamp (or buzzer) is either inactive or active. This analogy is discussed later in this chapter under the binary numbering system, and is the basis of digital computer operation.

1-7. Only the digital computer is discussed in this text, since it represents the most versatile machine in the electronic computer family. There are various types of digital computers. These include special-purpose, scientific and business-logistical computers.

1-8. Special-purpose computers are designed for a special operation. An example is the computer used in our air defense network. This computer accepts inputs from radar and other information sources, makes extensive computations, then launches and controls guided missiles to intercept and destroy enemy aircraft.

1-9. The scientific digital computer accepts small quantities of information, performs vast amounts of mathematical and logistical operations, and provides an answer which is usually short. An example is the computer used in tracking earth satellites.

1-10. The business-logistical computer accepts vast quantities of data, performs relatively small amounts of processing, and supplies large quantities of data. This computer is used in data processing equipment; it stores large volumes of data and uses stored and new data for calculations at a relatively high speed.

1-11. Electronic data processing equipment has 5 basic components . . . input, storage, processing, control, and output, as shown in figure 1-1.

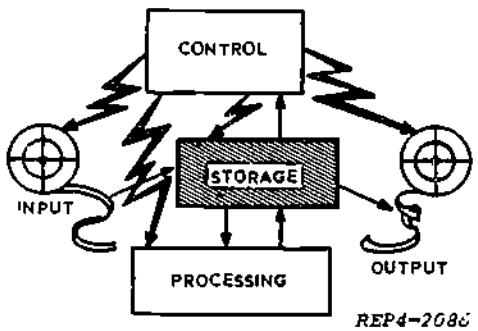

Figure 1-1. Basic Computer Block Diagram

1-12. Let's use an analogy and examine what is involved when a clerical worker does a routine job consisting of a simple sequence of operations:

1-13. The clerk receives a piece of data in a standard form. This data could be called INPUT and might be received through an in-basket on the clerk's desk.

1-14. The next operation involves transferring data from the input standard form to a data worksheet. The worksheet could be called STORAGE, since it is an organized means of storing data and instructions for use in subsequent operations.

1-15. Next, the clerk might feed data from the worksheet into a desk calculator for arithmetic PROCESSING. The desk calculator is an arithmetic processing unit used at the command of the clerk (CONTROL). Answers from the calculators are always returned to the worksheet (storage), where they will be available for subsequent operations.

1-16. When all necessary steps are completed, new data has been created. The last operation is to place this newly created data in the out basket (OUTPUT).

1-17. The clerk in this example is the control unit. The clerk reads instructions on the data sheet, interprets each instruction, performs the specified operation, and proceeds in this manner, performing each instruction in sequence, as prescribed on the data sheet. In performing these operations, the clerk uses input, processing, storage, control, and output, as directed.

1-18. Thus, in a clerical data processing system, we have the same five components shown in figure 1-1.

1-19. Let's put together a simple computer that performs the same routine jobs as the clerk, but with greatly increased speed and accuracy.

1-20. First, as before, we must have input. In our example, the computer will read input data from a prescribed format just as the clerk reads input data from a prescribed format placed in the in-basket.

1-21. In place of the clerk's data worksheet, the computer will use a storage device so both instructions and data can be copied into storage, and referred to as often as desired.

1-22. Where the clerk had a manually-operated mechanical desk calculator for the processing unit, the computer has an electronic version that is capable of performing all the arithmetic functions in microseconds. The answers are always transferred to storage (memory) after the specific arithmetic operation is completed. Just as the clerk copies the answers from the desk calculator onto her worksheet to avoid losing

them, the computer must always copy the answers into storage.

1-23. When all the steps in a problem are completed, the computer produces the final answer or required output. Thus, the computer input and output replace the in-out data sheets and the in-out baskets of the manual clerk system.

1-24. The remaining component is control, which consists of electronic circuits somewhat similar to a high-speed telephone exchange. In the telephone system of today, you dial a number (which is an instruction), and the switching network selects and sets up the necessary circuits to connect you with the correct telephone. Similarly, the electronic circuits in the control unit of a computer obtain instructions from storage and set up the circuits necessary to perform the operations requested. Thus, the control unit of the computer reads instructions from storage, then proceeds to set up the circuits necessary to perform the desired operations.

1-25. Since a digital computer deals directly with numbers as numbers, we must study numbering systems. The decimal system, using 10 different symbols, is the most common system in use today.

1-26. Many different numbering systems are possible and are available for use. The number of different symbols or digits used in a number system is called the base, or radix, of the system. In addition to the 10-digit decimal system, digital techniques use the binary, with a base of two, and the octal, with a base of eight. This chapter presents some important facts about decimal, binary, and octal numbering systems, with their arithmetic operations.

1-27. Computers can be designed to operate with any numbering system. However, only the decimal, octal, and binary systems are commonly used. Each system has its own advantages, and each is used in a different type of computer. Sometimes two or more number systems are used in the same equipment. When this is done, a facility is incorporated to convert from one number system to the other.

1-28. Decimal and Binary Numbering Systems

1-29. The decimal numbering system uses ten different basic symbols: 0, 1, 2, 3, 4, 5, 6, 7, 8, and 9. These symbols are called digits. In order to represent a number larger than 9, PLACE VALUE must be used. PLACE, in this case, is the position of the symbol with respect to the decimal point. It determines the power of 10 by which the digit in the place will be multiplied.

1-30. In figure 1-2, the 3 written in the units column stands for three, but the 3 written in the tens column stands for 30. Thus, in a number system the VALUE of a digit depends upon its PLACE in the number.

1-31. In figure 1-2, moving a digit to the left from one column to the next has the effect of multiplying the number by 10. The digit 3 in the units column stands for three. Moving 3 one column to the left signifies 30. If moved one more column, it indicates 300. You can see that in the decimal system, PLACE represents the power of 10 by which the digit must be multiplied.

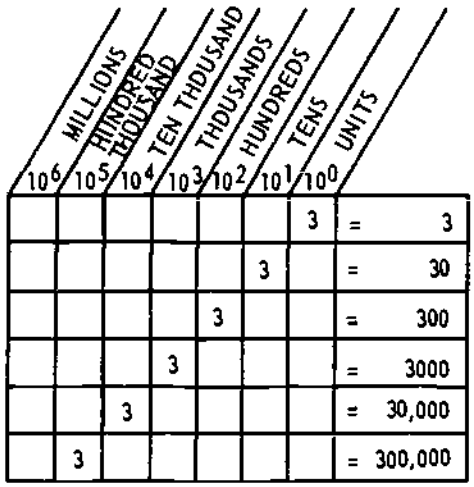

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Figure 1-2. Decimal Place Values

1-32. When the system of using place value was first developed, a space was used to indicate that no number appeared in that position. For example, 106 was written 1 6 and 1006 was written 1 6. It is easy to see that this system led to confusion. Does 1 6 represent 10006 or 100006? It is difficult to decide with certainty. This difficulty led to the development of a PLACE HOLDER or the use of the zero.

1-33. You have learned how to write numbers as powers of 10. Recall that 10^4 is 10 x 10 x 10 x 10. The number 4 tells how many times to use 10 as a factor. In the equality $10^4 = 10{,}000$, 10 is the BASE and 4 is the EXPONENT. The number 10^4 can be read as "10 to the fourth power." Therefore, in the decimal system one speaks of the POWERS of 10. Other systems use a different base. For example, the binary system uses powers of two: 2^4 is 2x2x2x2, or 16.

1-34. The decimal number $305.84_{(10)}$ consists of seven different parts. The following shows the name and relationship of each part:

Integral Portion	305
Fractional Portion	84
Place Holder	0
Decimal Point	.
LSD (Least Significant Digit)	4
MSD (Most Significant Digit)	3
Radix	(10)

1-35. The INTEGRAL PORTION (305) is left of the decimal point, while the FRACTIONAL PORTION (84) is to the right of the decimal point. The LSD (4) has the smallest value, and the MSD (3) has the greatest value, due to their relative positions in the number. The RADIX indicates which numbering system is being used and is written as a subscript to a number. Normally the radix is omitted in decimal numbers. Because binary numbers consist of only two digits, the radix 2 is often omitted. If any possible confusion may arise, the radix should be included. Usually the base and subscript are the same and showing both is unnecessary. In case both are indicated, e.g., $4^3{}_{(10)} = 64$, the 4 is the base and the (10) is called the radix.

1-36. Six of the seven different parts of a number listed above apply to any numbering system that uses the place value concept. The exception is the term DECIMAL POINT. Octal numbers have an OCTAL POINT and binary numbers have a BINARY POINT. In the number $320.61_{(8)}$ the point (.) is referred to as the OCTAL POINT. When working with a number such as $1101.11_{(2)}$, the point (.) is referred to as the BINARY POINT.

1-37. Three important features of numbering systems are:

- Place value for the symbols positioned in the number.
- A point (.) which is used to separate the fractional part of a number from the whole part.
- A radix, or base, of a number system.

1-38. Most present day digital computers use the binary numbering system. One advantage of this binary numbering system is that it uses only two symbols. These symbols are 0 and 1. Since only two symbols are used, a computer using the binary system needs only two different conditions to represent them. This simplifies computer design and improves its accuracy. Many electronic components can be operated as two state (on-off) devices; for example, each digit of a binary number can represent a logic situation of yes or no, a relay energized or deenergized, a transistor conducting or cut off, a switch open or closed. To express numbers other than 0 and 1 in the binary system, the symbols are arranged in sequence. The PLACE of each symbol in the sequence has a designated VALUE based on the binary numbering system.

1-39. The binary system uses the radix two (2). It has only two symbols - zero and one. You can write any number using these two symbols. Zero stands for NOTHING and is the PLACE-HOLDER for the system. One stands for I, unity, or a single unit.

2^5	2^4	2^3	2^2	2^1	2^0	=	BASE WITH EXPONENT
32	16	8	4	2	1	=	DECIMAL VALUE OF EACH PLACE
					1	=	$1_{(10)}$
				1	0	=	$2_{(10)}$
			1	0	0	=	$4_{(10)}$
		1	0	0	0	=	$8_{(10)}$
	1	0	0	0	0	=	$16_{(10)}$
1	0	0	0	0	0	=	$32_{(10)}$

Figure 1-3. Binary Place Values

Compare the decimal system with the binary system to clarify the idea of place values.

PLACE	BINARY	DECIMAL
1	2^0 or 1	10^0 or 1
10	2^1 or 2	10^1 or 10
100	2^2 or 4	10^2 or 100
1000	2^3 or 8	10^3 or 1000
10000	2^4 or 16	10^4 or 10000

Figure 1-4. Binary to Decimal Conversion

Note carefully the following facts:

1. In both systems, 1 indicates the place has value.

2. In both systems, 0 is a place-holder.

3. The number of zeros following 1 is the exponent of the base. Thus, in the decimal system $1000 = 10^3$, and in the binary system $1000 = 2^3$.

1-40. Binary equivalents for decimal numbers from 1 to 10 are shown in figure 1-5. Compare this with figure 1-3 to observe how place holders and 1's determine the numerical values.

1-41. One of the most important mathematical operations is the conversion of a number from one number system to another.

DECIMAL NO.	BINARY NO.
1	1
2	10
3	11
4	100
5	101
6	110
7	111
8	1000
9	1001
10	1010

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Figure 1-5. Binary Equivalents

1-42. Decimal to Binary Conversion

1-43. We use the multiplication-division method to convert from a decimal number to a binary number. This method of conversion has two parts, treating the integral and fractional parts of the number separately. The integral portion uses a dividing process; the fractional portion uses a multiplying process. We will work with integral numbers only.

1-44. To convert the integral portion of a decimal number, follow these rules:

1. Divide the integral number by 2 (the radix).

2. Write the remainder of the first division, whether a zero or a one, as the LSD of the binary number.

3. Divide the quotient of the first division by 2 and the remainder becomes the next digit of the binary number.

4. Write the remainder of the final division as the MSD.

PROBLEM: Convert $30_{(10)}$ to a binary number.

Decimal Number	÷	Binary Radix	=	Quotient	Remainder (Binary Digit)	
30	÷	2	=	15	0	= LSD
15	÷	2	=	7	1	
7	÷	2	=	3	1	
3	÷	2	=	1	1	
1	÷	2	=	0	1	= MSD

$30_{(10)} = 11110_{(2)}$

1-45. A short method for converting small decimal numbers to binary is to use the powers of two, as follows:

1. Find the largest power of two in the number; e.g., 30 = 16 + 14, 16 is 2^4, so the MSD is 1 in the 2^4 place; 1XXXX.

2. Use the remainder (14) and find the highest power of 2; e.g., 14 = 8 + 6. The 8 is 2^3, so place a 1 in the 2^3 place, and the binary number becomes 11XXX.

3. Continue this procedure to complete the conversion: 6 = 4 + 2, giving a 1 in the 2^2 and 2^1 positions with 0 in the 2^0 position. Thus, $30_{(10)} = 11110_{(2)}$.

Let us work one more problem: Convert $131_{(10)}$ to binary.

Decimal Number	÷	Binary Radix	=	Quotient	Remainder (Binary Digit)	
131	÷	2	=	65	1	LSD
65	÷	2	=	32	1	
32	÷	2	=	16	0	
16	÷	2	=	8	0	
8	÷	2	=	4	0	
4	÷	2	=	2	0	
2	÷	2	=	1	0	
1	÷	2	=	0	1	MSD

$131_{(10)} = 10000011_{(2)}$

1-46. Binary to Decimal Conversion

1-47. It is often necessary to convert binary to decimal. To accomplish this conversion, multiply each digit by its place-value and add the products. Figure 1-6 indicates some of the place values for binary numbers and three conversion problems. The chart may be extended as required.

1-48. Another method to convert a number of any base to a decimal number is similar to synthetic division used in algebra. Use the following rules to convert the binary number to a decimal number:

1. Multiply the MSD by the radix of the number being converted (2 for binary).

2. Add this product to the next lower digit of the number being converted.

ETC--	2^4	2^3	2^2	2^1	2^0	= BASE WITH EXPONENT
	16	8	4	2	1	= DECIMAL VALUE OF EACH PLACE
					1	= 1
			1	0	1	= 5
	1	1	0	1	1	= 27

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Figure 1-6. Binary to Decimal Conversions

3. Multiply their sum by the radix (2).

4. Repeat steps 2 and 3 for all the digits of the number being converted, except for the LSD. For LSD, repeat only step 2.

5. The final sum is the decimal number. For example: Convert $1011_{(2)}$ to a decimal number. The circled number is the converted result.

$$\begin{array}{r} 1\ 0\ 1\ 1 \\ \searrow \\ 2\ 4\ 10 \\ \hline \nearrow\ \nearrow \\ 2\ 5\ \textcircled{11} \end{array}$$

$$1011_{(2)} = 11_{(10)}$$

1-49. Octal Numbering System

1-50. The computer uses the binary numbering system to do its calculations. The binary system, however, has the disadvantage of requiring 3 to 4 times as many digits in a row to represent a number as does the decimal system. Chances for human error are much greater with an increase in the number of digits.

1-51. To reduce human errors, the octal numbering system is often used in digital computer input and output units. The octal system requires only one-third as many digits as the binary system. The octal system is more convenient than decimal for representing binary numbers because it is very easy to convert from binary to octal and octal to binary.

1-52. The octal numbering system, sometimes called the octonary system is similar to the decimal and binary systems. They differ in the radix; the radix of the octal system is 8. The octal numbering system uses eight (8) digits: 0, 1, 2, 3, 4, 5, 6, and 7.

1-53. Octal counting proceeds from 0 to 7 just as in the decimal system. At 7 in the octal system, however, there are no more symbols available. To progress from 7 to 8 requires a carry operation and the use of place values. The following shows decimal numbers and their octal equivalents.

Decimal No.	Octal No.	Decimal No.	Octal No.
0	0	6	6
1	1	7	7
2	2	8	10
3	3	9	11
4	4	10	12
5	5		

1-54. In the octal system, the place-value of a digit is determined by its position relative to the octal point. See figure 1-7.

1-55. An octal number may also be expressed according to the "general expression" for a number, which is its decimal equivalent.

$$210_{(8)} = (2x8^2) + (1x8^1) + (0x8^0)_{(10)}$$

8^5	8^4	8^3	8^2	8^1	8^0	= POWER OF RADIX
32768	4096	512	64	8	1	= PLACE VALUE
					1	$= 1_{(10)}$
			1	0	0	$= 64_{(10)}$
1	0	0	0	0	1	$= 32769_{(10)}$

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Figure 1-7. Octal Place Values

1-56. Decimal to Octal Conversion

1-57. We use the multiplication-division method to convert from a decimal number to an octal number. The same rules apply as in converting decimal to binary, except use 8 instead of 2.

1-58. This method of conversion has two parts, treating the integral and fractional parts of the number separately. The integral portion uses a dividing process, and the fractional portion uses a multiplying process. We will work with whole numbers only.

1-59. To convert the integral portion of the decimal number to octal, follow these rules:

1. Divide the integral number by 8.

2. Write the remainder of the first division as the LSD of the octal number.

3. Divide the quotient of the first division by 8 and use the remainder or zero as the next digit of the octal number.

4. Continue division by 8 until the quotient is zero.

5. Write the remainders as the digits of the octal number, and the MSD is generated last.

Problem: Convert $3844_{(10)}$ to its octal equivalent.

Decimal Number	÷	Octal Radix	=	Quotient	+	Remainder (Octal Digit)
3844	÷	8	=	480	+	4 LSD
480	÷	8	=	60	+	0
60	÷	8	=	7	+	4
7	÷	8	=	0	+	7 MSD

$3844_{(10)} = 7404_{(8)}$

1-60. Let us work one more problem: Convert $204_{(10)}$ to its octal equivalent.

Decimal Number	÷	Octal Radix	=	Quotient	+	Remainder (Octal Digit)
204	÷	8	=	25	+	4 LSD
25	÷	8	=	3	+	1
3	÷	8	=	0	+	3 MSD

1-61. Octal to Decimal Conversion

1-62. Accomplish octal to decimal conversion in the following manner: Convert the octal number $227_{(8)}$ to a decimal number. Use figure 1-7 for place values:

$$227_{(8)} = (2x8^2) + (2x8^1) + (7x8^0)_{(10)}$$

$$= (2x64) + (2x8) + (7x1)_{(10)}$$

$$= 128 + 16 + 7_{(10)}$$

$$= 151_{(10)}$$

1-63. Another method which may be used to convert a number of any base to a decimal number is similar to synthetic division used in algebra. Convert the integral portion of the octal number to a decimal using the following rules:

1. Multiply the MSD by the radix (8 for octal).

2. Add the product to the next lower digit of the number being converted.

3. Multiply the sum of the two numbers in step 2 by the radix.

4. Repeat steps 2 and 3 for all digits of the number being converted except for the LSD. For the LSD, repeat only step 2.

5. The final sum is the converted number. For example: Convert $234_{(8)}$ to decimal; the circled number is the converted result.

MSD 2 → 3 4
16 152
19 (156)

$234_{(8)} = 156_{(10)}$

1-64. Octal to Binary Conversion

1-65. A requirement often exists for octal to binary conversion. The substitution method of conversion takes advantage of a natural relationship beteween octal and binary numbers. The base of the octal system is 8; the base of the binary system is 2, and 2^3 equals 8. One octal digit may be expressed by three binary digits (bits); for example, count to 7 in each system:

Octal No.	Binary No.	Octal No.	Binary No.
0	000	4	100
1	001	5	101
2	010	6	110
3	011	7	111

1-66. Convert an octal number to its binary equivalent by direct substitution. Replace each octal digit by its corresponding three binary digits. By substitution, for example, the number $23_{(8)}$ equals $010011_{(2)}$. For another example, convert $56,473_{(8)}$ to binary:

5	6	4	7	3	(8)
101	110	100	111	011	(2)

1-67. In the last example, the groupings are separated to call attention to the equivalence. In actual practice, there is no spacing between groups. To check for equivalence, convert both the binary and octal numbers to decimal numbers. Both equal $23,867_{(10)}$.

1-68. Binary to Octal Conversion

1-69. Binary to octal conversion also uses substitution. To make this conversion, arrange the binary digits in groups of three, proceeding to the left and to the right from the binary point. Fill out the extreme left or right group with 0's if necessary. Then directly substitute for each binary group its octal digit equivalent. For example, convert $11100_{(2)}$ to an octal number:

11100 = 011 100

= 011 100

3 4

$11100_{(2)} = 34_{(8)}$

1-70. Arithmetic Operations

1-71. You can add, subtract, multiply and divide using binary and octal numbers. This text discusses only addition and subtraction.

1-72. Binary Addition

1-73. To determine the sum of two binary numbers, follow these rules for addition:

1. 0 + 0 = 0
2. 0 + 1 = 1
3. 1 + 0 = 1
4. 1 + 1 = 0 with 1 to carry to the next higher column.

1-74. Let us apply these rules to a binary addition problem. Add 1110 to 1011.

E	D	C	B	A	
1	1	1			= Carry
	1	0	1	1	
	1	1	1	0	
1	1	0	0	1	= SUM

Steps: (Begin at the right hand column and work to the left).

A. 0 + 1 = 1, with no carry.

B. 1 + 1 = 0, with a carry of 1 to the C column.

C. 1 + 0 + 1 (the carry from B) = 0, with a carry of 1 to D.

D. 1 + 1 + 1 (the carry from C) = 1, with a carry of 1 to E.

Bring the carry of 1 in E down, and it becomes the MSD of the final sum. Practice problems and solutions:

		10011	
1010	111	0010	1011101010
0101	11	1001	1000111001
1111	1010	11110	10100100011

1-75. For an even number of 1's (including carries) in each column, the sum will always be 0. For an odd number of 1's (including carries) in each column, the sum will always be 1. For every two 1's in a column (including carries), 1 is carried to the next column.

Example:

```
    1 1 1 1  <------ carries
  1 1 1 1 1 1
      1 1 1 1 1
        1 0 1 0
      1 0 1 0 1
      1 1 1 1 1
  ---------------
  1 0 1 1 1 0 1
```

1-76. Binary Subtraction

1-77. We will discuss two methods of subtracting binary numbers. The subtraction methods are:

1. End-around-carry.
2. Direct subtraction.

1-78. The end-around-carry method is the most frequently used in computers because of the ease with which it can be accomplished.

End-around-carry uses the "ones complement," which corresponds to the nines complement used in the decimal system. A one's complement can be written by just putting 1 for 0 and 0 for 1. To subtract using the end-around-carry method, follow these rules.

1. Complement the subtrahend.
2. Add.
3. End-around-carry.
4. Add.

Example: Subtract 0101 from 1110.

```
 1110 minuend
-0101 subtrahend
 ---- difference or remainder
```

1. Complement the subtrahend.

```
 1110
 1010
```

2. Add complemented subtrahend to minuend.

```
  1110
 +1010
 11000
```

3. End-Around-Carry.

```
  1110
  1010
 (1)1000
     -> 1
```

4. Add.

```
  1110
  1010
  1000
 +   1
  1001
```

5. Check.

```
  1001
 +0101
  1110
```

NOTE: The end-around-carry method does not work when two equal numbers are to be subtracted.

1-79. Direct subtraction is the second method. Follow these four rules:

1. 0 - 0 = 0 with no borrow.

2. 1 - 1 = 0 with no borrow.

3. 1 - 0 = 1 with no borrow.

4. 0 - 1 = 1 with a borrow of 1.

Example:

```
      1
    0 1
  1 Ø 1 1 0
- 1 0 1 0
---------
  1 1 0 0
```

1-80. Since the MSD of the minuend is worth 16, two binary ones must be used to represent it in the next lower position, which represents 8. Thus, there is a remainder of 1.

1-81. Perhaps the simplest way to perform binary subtraction is to subtract as in decimal subtraction. That is, by treating the bits as decimal digits. When a borrow is necessary in any number system, its value is equal to the radix of that system. The borrow is then added decimally to the minuend bit of that particular column and the subtrahend is subtracted decimally.

Example:

```
    0 2   Borrow
  1 Ø     Minuend
- 1       Subtrahend
-----
  1
```

1-82. Octal Addition

1-83. Octal addition also uses the sum and carry technique. A carry to the next higher order column is produced each time a sum equals or exceeds the radix.

Follow these rules step-by-step:

1. Add the digits in the LSD column as in decimal addition.

2. Divide the sum of the added column by the radix (8 for octal).

3. Write the remainder under the column added and carry the quotient to the next higher-order column.

4. Add the digits in the next higher-order column along with any carry.

5. Repeat steps 2, 3, and 4 until all columns have been added. For example, add $476_{(8)}$ to $673_{(8)}$.

```
Step 1 -  673          Step 2 -   1  Quotient
         +476                   8) 9
          ---                     8
            9                     -
                                  1  Remainder

Step 3 -  1  Carry     Step 4 -   1
          673                    6 73
          476                    4 76
          ---                    ----
           Ø                     15Ø
          ---                    ---
          1  Sum                  1

Step 2 -    1          Step 3 - 1 1
          8) 15                  6 73
             8                   4 76
             -                   ----
             7                   15Ø
                                 ---
                                 71

Step 4 -  1  1         Step 2 -    1
          6  7 3                 8) 11
          4  7 6                    8
          ------                    -
          11 15 Ø                   3
             7 1

Step 3 - 1  1  1       Step 4 - 1  1  1
           6  7 3                 6  7 3
           4  7 6                 4  7 6
           -------                -------
           11 15 Ø                11 15 Ø
           3  7 1                 1  3  7 1
```

or

```
  673
 +476
 ----
 1371(8)
```

1-84. Briefly, whenever the column added exceeds the radix, the number of times it exceeds the radix is a carry, and the remainder is the sum digit.

1-85. Octal Subtraction

1-86. Octal subtraction is performed in much the same manner as decimal and binary direct subtraction. See binary direct subtraction in paragraphs 1-79 through 1-81. When a borrow is necessary in any number system, its value is equal to the radix of that system. The borrow is then added to the minuend digit of that particular column and the subtrahend is subtracted. For example, subtract $45_{(8)}$ from $54_{(8)}$:

Borrow: 8 + 4

	4 12	
	5 4	minuend
-	4 5	subtrahend
	7	difference

Proof:

$$\begin{array}{r} 45_{(8)} \\ +\ 7_{(8)} \\ \hline 54_{(8)} \end{array}$$

1-87. Another example of octal subtraction using three digits is shown in the following example: Subtract $565_{(8)}$ from $704_{(8)}$.

		7		
	6	8	12	
	7	0	4	(8)
-	5	6	5	(8)
	1	1	7	(8)

Borrow one 8 from the 7 (MSD of $704_{(8)}$). Then borrow one 8 from column two's minuend. Thus, the minuend becomes:

6 7 12 (8)

The answer $117_{(8)}$ is now apparent.

CHAPTER 2

LOGIC FUNCTIONS AND BOOLEAN EQUATIONS

2-1. Logic gating circuits are employed in digital equipment to combine continuous trains of pulse information. To understand these circuits, it is necessary to become familiar with their theory of operation as well as their applications.

2-2. This chapter introduces simple logic gating circuits, including descriptive definitions, logic gating symbols, circuits, and truth tables. The chapter concludes with an analysis of logic circuits, showing how Boolean Algebra applies to these circuits.

2-3. Logic Functions

2-4. A computer is no more than a combination of simple devices which perform a few basic operations. The complexity of a computer arises only from the large number of simple devices and the way they are interconnected. The interaction of signals as they process through a computer is called "logic"; the circuits involved are called "logic circuits."

2-5. Outputs of logic circuits have two voltage values, called "logic levels." One level represents binary 1 and the other represents binary 0. If the more positive of the two voltage values represents 1, the circuit uses "positive logic." If the more negative logic value represents 1, the circuit uses "negative logic." This chapter uses positive logic.

2-6. It is possible to design logic circuits using just two kinds of components: GATES, which transmit signals only when input signals are present in specified combinations, and STORAGE ELEMENTS, which store or remember a signal so that it may be used at a later time.

2-7. A gate is a device having two or more inputs and one output. Some of the inputs may be called "signal" inputs and others may be designated as "control" or "selector" inputs, although the inputs are often indistinguishable from one another.

2-8. AND Logic

2-9. One of the common logic operations is called the AND function. It requires that all inputs be present in order to obtain the specified output. As an example: pigment, lead, and linseed oil make an oil base paint. All three are required at the same time to produce the result. With one or more of the three inputs missing, the specified result is not produced. The logic can be written: Pigment AND Lead AND Linseed Oil = Paint.

2-10. This same situation can also be represented in diagram form as shown in figure 2-1.

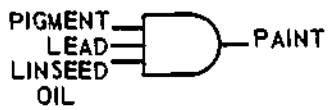


Figure 2-1. AND Situation Symbolized

2-11. The symbol in figure 2-1 represents the AND function. The symbol indicates that AND is the relationship between its "inputs" which are, of course, the arrival of pigment, lead, and linseed oil. Another way of thinking of it - more accurately when dealing with equipment – is that the symbol applies the AND function to its inputs. The circuit produces an "output" only when the inputs meet the AND requirements – that is, when all of the inputs appear at the same time.

2-12. Figure 2-1 can be altered, as in figure 2-2, to illustrate the general case, any AND situation. Four inputs are shown (A, B, C, and D), although any number of inputs (two or more) is possible.

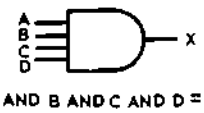


Figure 2-2. Four-Input AND Gate

2-13. Circuits which perform the AND function are called AND gates. AND gates may use diodes as shown in figure 2-3. The circuit has one output, at which a pulse appears if, and only if, pulses are applied simultaneously to BOTH inputs. If the inputs are not of the same time duration, the output will appear only during the time interval that the input pulses overlap.

2-14. When both diodes have a high input, the output is "high". When either diode has a low input, or if both diodes have low inputs, the output is "low". A low output is considered NO output and represents binary 0.

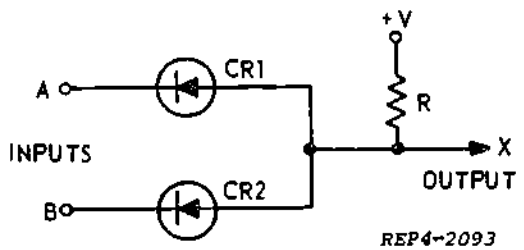


Figure 2-3. Diode AND Gate

2-15. In the explanation of AND circuits the logic levels are the numeric values of the high or low outputs. If the output levels are 0 V and -6 V, 0 volts represents a high and -6 volts represents a low. The most positive value is high and the most negative value is low. The high represents binary 1; and the low represents binary 0.

2-16. Time T0 to T1 in figure 2-4A shows -6 volts being applied to both diode inputs. Both diodes are conducting heavily, and the output is -6 volts (low). Figure 2-4B shows the equivalent circuit with the diodes shorted.

2-17. Time T1 to T2, figure 2-4A, shows the A input at 0 volts (high) and the B input at -6 volts (low). CR2 is conducting heavily and the output and the anode of CR1 is -6 volts. CR1 is reverse biased and does not conduct. Figure 2-5 shows the equivalent circuit with CR2 shorted. The -6 volt (low) output is identified as "no output."

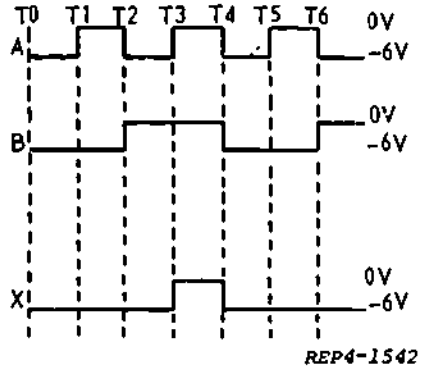


Figure 2-4A. AND Gate Waveforms

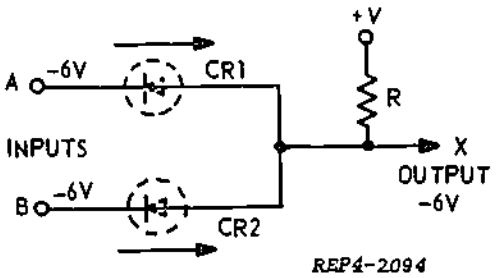


Figure 2-4B. AND Gate (Equivalent Circuit of Two Low Inputs)

2-18. During time T2 to T3, CR1 conducts heavily and CR2 is cut off. The output remains at -6 V.

2-19. Time T3 to T4, figure 2-4A and figure 2-6, shows inputs at zero volts. Both diodes conduct and clamp the output to zero. This 0 volt output is a high and is identified as an "output".

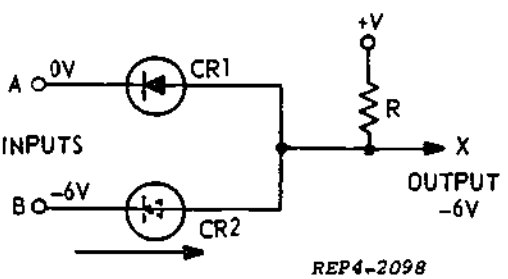


Figure 2-5. AND Gate (Equivalent Circuit One High Input)

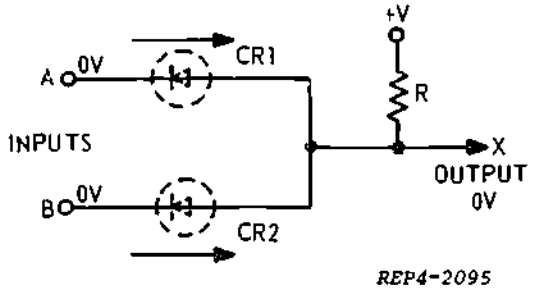


Figure 2-6. AND Gate (Two High Inputs)

2-20. A TRUTH TABLE shows all the possible input conditions, and the output of each case. Figure 2-8 has a truth table which relates all the conditions of the AND gate. Compare each line of the truth table with specific circuitry as follows:

In figure 2-4, when both diodes have a -6 volt input (L), the output is -6V (L). Figure 2-5 shows one diode input as -6 volts (L) with the other diode input 0 volts (H); the output is -6 volts (L). Figure 2-6 shows 0 volts (H) on both diodes; this is the AND condition which provides an output (H).

2-21. The important feature to remember about an AND gate (figure 2-8) is that all inputs must be high (H) before output X will be high.

2-22. OR Logic

2-23. One of the common logic operations is called the OR function. This comes into play when any one of two or more alternate possibilities can bring about a specified result. For example, "We'll go to the movies if George, Pete, or Joe shows up." In this case, the arrival of George OR Pete OR Joe leads to the result, go to the movies. This situation can be written in short form:

GEORGE OR PETE OR JOE = MOVIES

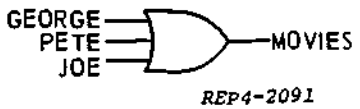
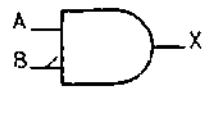


Figure 2-7. OR Situation Symbolized



A	B	X
L	L	L
L	H	L
H	L	L
H	H	H

TRUTH TABLE

REP4-1540

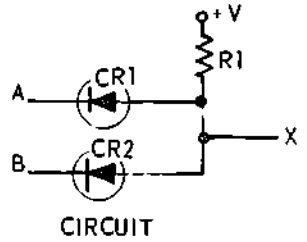


Figure 2-8. AND Gate Features

George OR Pete OR Joe = Movies

2-24. This same situation can also be represented in diagram form. as shown in figure 2-7. The symbol (shield) indicates that OR is the relationship between its INPUTS which are, of course, the arrival of George OR Pete OR Joe. This symbol indicates the OR function is applied to the circuit inputs. The function produces an output only when the inputs meet the OR requirements; in other words, when at least one input appears, there is an output. Figure 2-9 illustrates the general case, any OR situation. Four inputs are shown (A, B, C, and D) although any number of inputs is possible.

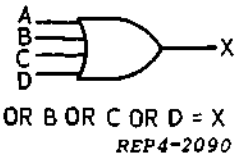


Figure 2-9. OR Function

2-25. The OR function produces a specified result at X, when any one of its input conditions (A OR B OR C OR D) is satisfied. Notice that if any one, two, three, or even all of its inputs appear together, the output at X is produced. The OR in this case includes all combinations as well as one-at-a-time inputs, so it is called an "Inclusive OR." In digital circuits, the OR function is always "inclusive" unless otherwise specified.

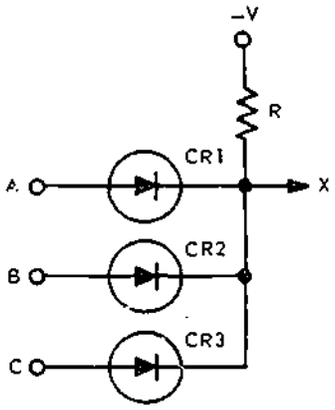


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Figure 2-10. OR Circuit

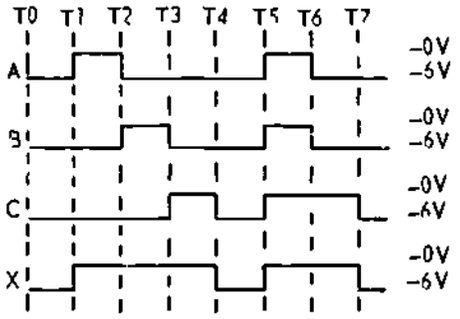

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Figure 2-11. OR Circuit Waveforms

2-26. Circuits which perform the OR function are called OR gates. OR gates may use two or more diodes connected in the manner shown in figure 2-10. The load resistor is connected to a negative potential. The presence of information is represented by a high, while the absence of information is represented by a low.

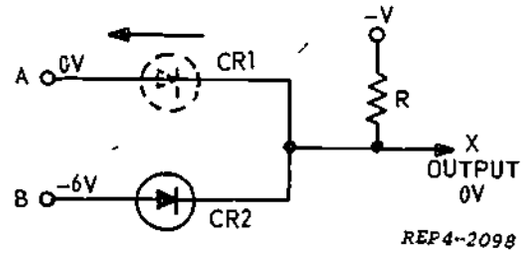

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Figure 2-12. OR Circuit (One High Input)

2-27. Figure 2-11 shows waveforms of the OR circuit. At time T0 to T1 all diode inputs are low (-6V), and the output is low (-6V). At time T1 to T2, the input to CR1 is high (0V), so CR1 conducts and the output goes high (0V). At time T2 to T3, CR2 conducts, so the output remains high. From T3 to T4, CR3 conducts, and the output is high. All inputs must be low to have a low output; one or more diodes conducting makes a high output.

2-28. Figure 2-12 shows a two-diode OR circuit. With one diode anode at 0 volts (H), and the other diode anode at -6 volts (L), the output is high (0V).

2-29. Assume no voltage drop across conducting CR1, the output is clamped to 0 volts. This clamping action causes zero volts to be felt on the cathode of CR2. Thus, the cathode of CR2 is positive with respect to its anode, causing CR2 to be reverse biased and the diode will not conduct. This operation occurs when one input is high and the other is low; the output is high.

2-30. If both inputs are at zero volts (H), then both diodes will conduct, and the output is high, as can be seen in figure 2-13.

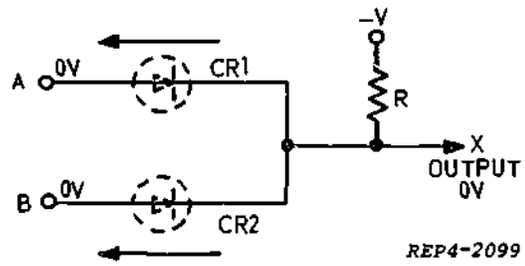

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Figure 2-13. OR Circuit (Two High Inputs)

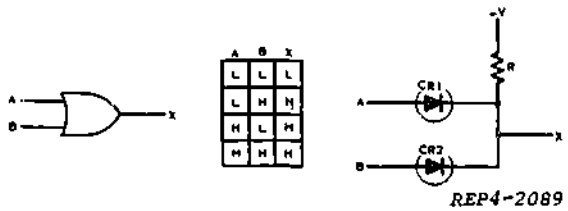


Figure 2-14. OR Gate Features

2-31. Figure 2-14 is the truth table which relates all of the conditions of the OR gate. In this truth table, the low (L) represents -6 volts while the high (H) represents 0 volts. Verify the truth table which indicates the following:

All inputs low gives a low output.

Any one input high gives a high output.

All inputs high gives a high output.

2-32. The important feature to remember from figure 2-14 is that any or all high (H) inputs will produce a high (H) output.

2-33. NOT Logic

2-34. Another logic operation of importance is the NOT function, which denotes an "inversion". When inverted, every high becomes a low. Similarly, an inverted low becomes a high.

2-35. A line drawn over a letter in a logic expression indicates a NOT function. "NOT A" is written as "$\overline{A}$". If A equals 1, then $\overline{A}$ equals 0. If A equals 0 then $\overline{A}$ equals 1.

2-36. An amplifier can be used to obtain the inversion necessary for a NOT function. For example, the common emitter amplifier inverts its input signal: a positive-going input gives a negative-going output. Common base and common collector amplifiers develop outputs with the same waveforms as their inputs; they are non-inverting amplifiers, and can not be used for a NOT function.

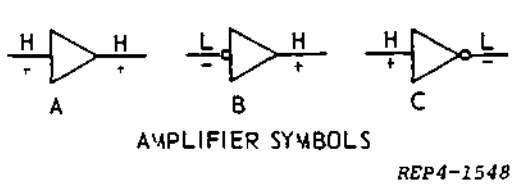


Figure 2-15. Amplifier Symbols

2-37. Figure 2-15 shows amplifier symbols. Figure 2-15A is a noninverting amplifier. A high input produces a high output. The small circle at the input or output (figure 2-15B or C) is called a STATE INDICATOR.

2-38. The state indicator at the input to the amplifier indicates that a LOW input activates the amplifier and produces a HIGH output.

2-39. The state indicator at the output of the amplifier indicates that a HIGH input activates the amplifier and produces a LOW output.

2-40. The output of an AND or OR circuit can become a NOT function by adding an inverting amplifier, as shown in figure 2-16. Recall that the AND function requires all inputs to be HIGH to get a HIGH output. Two HIGH inputs to a two-input AND function produce a HIGH at point X, which activates the amplifier, and the output at point $\overline{X}$ is LOW; at all other times the output remains HIGH. Observe this in the truth table.

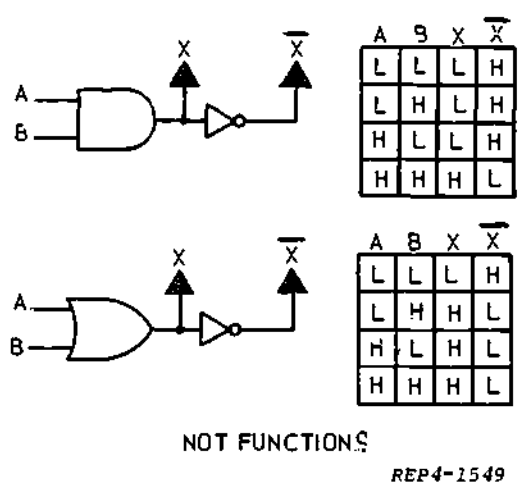


Figure 2-16. NOT Function

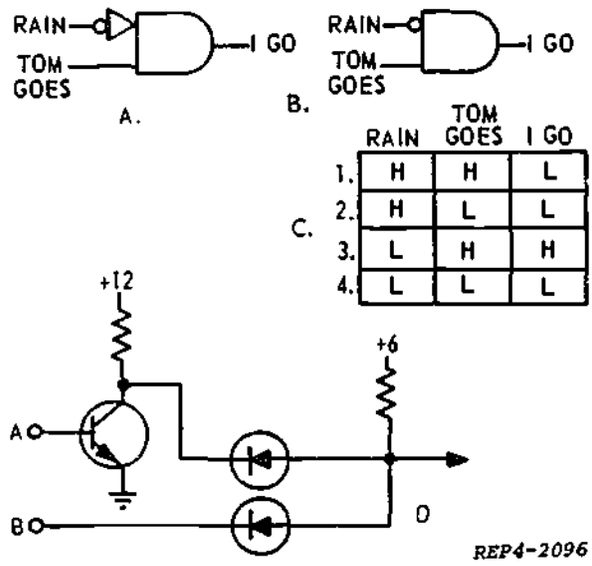


Figure 2-17. Inhibit Gate

2-41. INHIBIT GATE. The NOT function is often used in conjunction with the input to an OR or AND circuit. For example, someone might say, "I"ll go if TOM does and it does NOT rain." Examination shows that this involves an AND function and a NOT function. This situation can be diagrammed as shown in figure 2-17A. A more common method of diagramming is to omit the amplifier symbol and show only the state indicator in conjunction with the AND symbol as in figure 2-17B. The circuitry for the inhibit gate is shown in figure 2-17D.

2-42. If rain is present (H), it prevents the AND circuit from producing an output. This prevention of the AND operation is called INHIBITING. When a state indicator is used at the input of an AND circuit, the function is termed an INHIBIT FUNCTION. The circuit which provides the inhibit function is called an INHIBITOR or INHIBIT GATE.

2-43. The truth table for the inhibit gate is shown in figure 2-17C. The truth table simply means:

1. It is raining and Tom is going but I am not going.

2. It is raining and Tom is not going so I am not going.

3. It is not raining and Tom is going so I will go.

4. It is not raining and Tom is not going so I am not going.

2-44. NAND GATE. An AND symbol with a state indicator at its output, figure 2-18A, makes a NOT-AND (NAND) symbol. The state indicator on the output of the AND

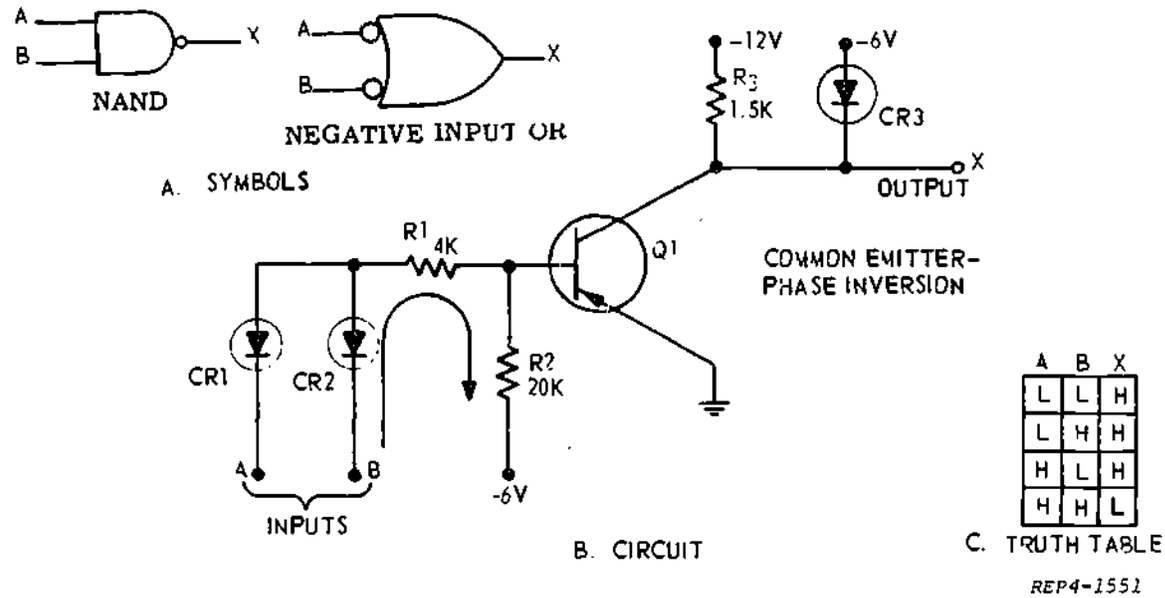


Figure 2-18. NAND Gate or Negative Input OR

symbol indicates a low voltage out. Thus, with two HIGH inputs the output will be LOW. An OR symbol with state indicators at each input is also shown in figure 2-18A. This logic symbol represents the NEGATIVE INPUT OR circuit. The circuit and the truth table in figure 2-18 applies to either logic symbol.

2-45. Figure 2-18B shows the NAND circuit. An AND gate at inputs A and B controls the bias on the base of amplifier Q1. The potentials applied at A and B are either 0 volts, representing a high, or -6 volts, representing a low.

2-46. Operation. When a low (-6V) input is applied to A or B, or to both A and B, the resistive network made up of R1 and R2 will have a total of 12 volts applied. The voltage drop across R2 will be -10V (top with respect to bottom) and the base to emitter voltage of Q1 will be -4V (+6V -10V). Thus, a forward bias is developed for Q1 and Q1 conducts. The collector voltage will be very near 0V and this value represents a high (H) output. Observe the TRUTH TABLE and note that when any input is low (L) the output (X) is high (H). When a high (0V) input is applied to A and B simultaneously, the resistive network has only 6 volts applied. The voltage drop across R2 will decrease to -5V and the resultant base to emitter voltage becomes +1V. Q1 is reverse biased and cuts off. As the collector voltage goes from near 0V toward -Vcc, a clamping diode becomes forward biased. This action occurs because the cathode of CR3 is connected to the collector of Q1 and it clamps the output voltage of Q1 at -6 volts which represents a low (L) output. Thus, when the inputs A and B are high (H), the output from X is low (L).

2-47. Figure 2-18C shows the truth table for the NAND circuit which you can verify. Keep in mind that the low is -6 volts and the high is 0 volts. When Q1 conducts, the output is high (0V); with Q1 cut off the output is low (-6V). An AND function output is HIGH, but a NAND function output is LOW.

2-48. NOR GATE. An OR symbol with a state indicator at its output, figure 2-19A, makes a NOT-OR (NOR) symbol. Notice that this state indicator on the output of the NOR symbol indicates a relatively low voltage out. Recall the normal output of an OR gate is HIGH with either input HIGH. This symbol indicates the output will be LOW. The other logic symbol shown in figure 2-19A is a NEGATIVE INPUT AND symbol. It consists of an AND logic symbol with state indicators at each input (A and B). The circuit and the truth table in figure 2-19 apply to either logic symbol.

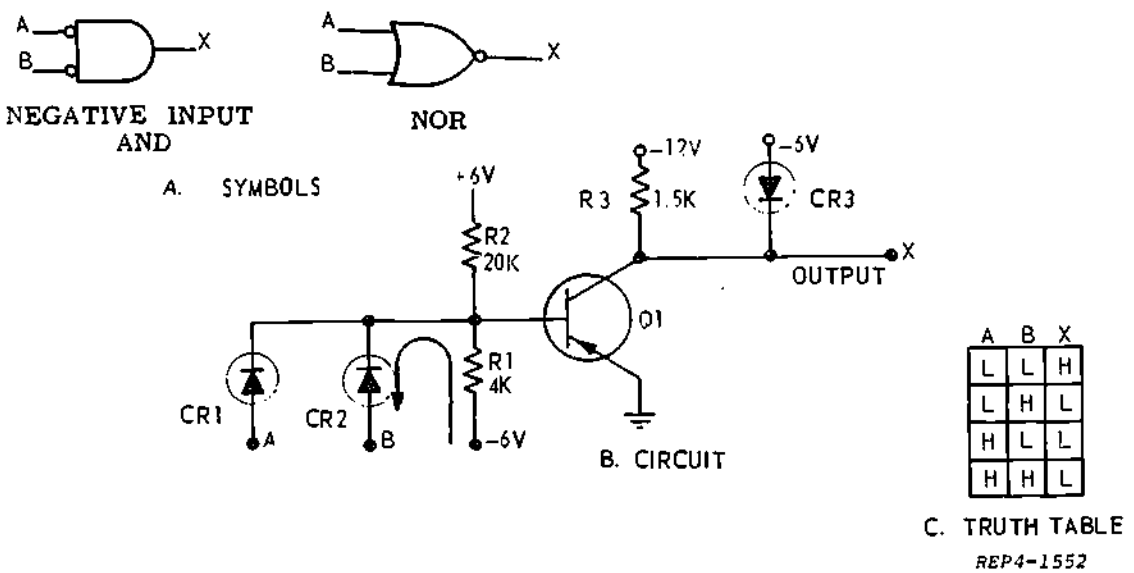


Figure 2-19. NOR Gate or Negative Input AND

2-49. Compare the NOR circuit in figure 2-19B to the NAND circuit of figure 2-18B. Note that the input diodes have been reversed and the base bias circuit has been changed.

2-50. Applying a high (0V) input to either diode or both will cause the corresponding diodes to conduct. The voltage drop across R1 will equal 6V, making the base and emitter of Q1 at the same potential, which cuts the transistor off. The cutoff condition gives a low (-6V clamped) output. Diode CR3 at the output establishes the low logic level; saturation conduction of Q1 establishes the high logic level. A high input to either A or B will produce a low output.

2-51. When both input diodes have -6V (low) applied at the same time, the voltage drop across R1 decreases to 2 volts and Q1 becomes forward biased (-6 +2 = -4V). The transistor conducts and the output is near 0 volts. Therefore, both inputs must be low (L) to give a high (H) output at X in a NOR circuit.

2-52. Figure 2-19C shows the truth table for the NOR circuit which you can verify. Notice that the two input diodes with resistors (R1 and R2) make up the OR-gate circuit. The common-emitter amplifier provides phase inversion. Any HIGH input (A or B or both) causes a LOW output as represented by the NOR symbol.

2-53. Exclusive OR Logic

2-54. Another logic function of importance is the "Exclusive OR". Figure 2-20A shows the symbol. An Exclusive OR will develop an output pulse when either input A or B is present, but not when BOTH inputs are present.

2-55. Figure 2-20B shows the exclusive OR logic diagram. Notice that the exclusive OR is a combination of two inhibited ANDs and an OR gate.

2-56. Figure 2-20C shows the truth table which you can verify. Refer to paragraph 2-43 to review the inhibit function condition for a HIGH output. Then compare the truth table with the logic diagram of figure 2-20.

2-57. Direct Coupled Transistor Logic

2-58. Logic systems are classified by the components used. Direct coupled transistor logic (DCTL) has the output of one amplifier stage directly coupled to the input of a following stage. Figure 2-21 illustrates a two stage DCTL amplifier.

2-59. Deleted.

2-60. Deleted.

2-61. Deleted.

2-62. The -0.1V input applied to the base of Q1 will not turn Q1 on. The base of Q2 is returned to -3V, so Q2 conducts. Base current of Q2 causes a 2.7V drop across R1, and clamps the collector of Q1 and the base of Q2 to -0.3 volt. This is the LOW logic level. With Q2 conducting (saturated), its collector will be at -0.1 volt; this is the HIGH logic level.

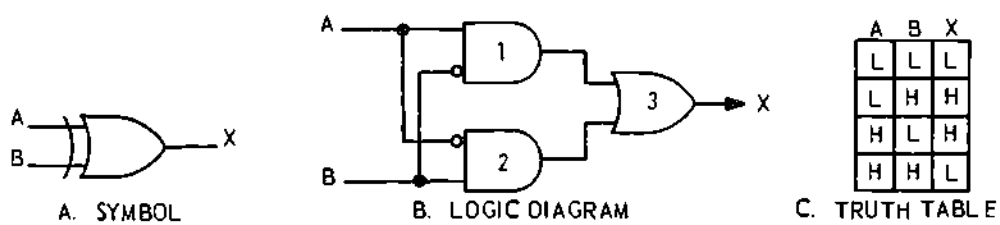


Figure 2-20. Exclusive OR Logic

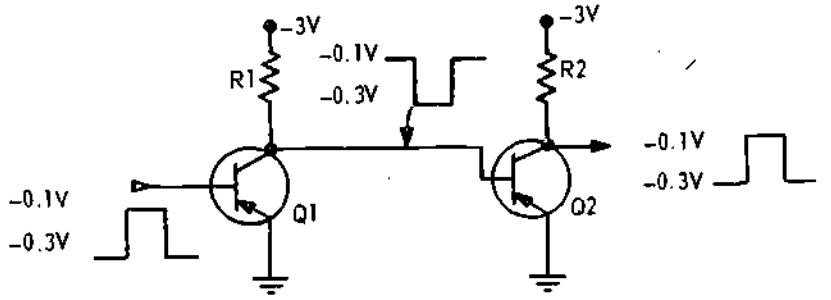


Figure 2-21. Two Stages of DCTL Amplifier

2-63. When the input to Q1 goes to -0.3 V, Q1 saturates, and its collector changes to -0.1 V. This change, applied to the base of Q2, cuts Q2 off. With Q2 cut off, its collector goes to -0.3 V (assuming that the output is connected to the base of another transistor).

2-64. This method of obtaining the logic levels simplifies the circuitry by eliminating the logic-level establishing components, such as the output diodes in figure 2-18 and 2-19.

2-65. PARALLEL GATE. Figure 2-22 shows a parallel gate. This gate consists of two parallel transistors connected in a common emitter configuration. This gate is capable of NAND and negative input OR operations.

2-66. If both inputs A and B are high (0.1V), the output at X will be low (-0.3V), assuming the gate is feeding another circuit. However, if either is low (-0.3V), the output at X is high (-0.1V). If both inputs are low (-0.3V), the output will be high (0.1V). Use these facts to check the truth table. Also compare this truth table with the table in figure 2-18. You should conclude that this circuit can be used as a NAND or a negative input OR gate.

2-67. Deleted.

2-68. Deleted.

2-69. The standard symbols are illustrated in figure 2-22B. Note the use of the state indicators.

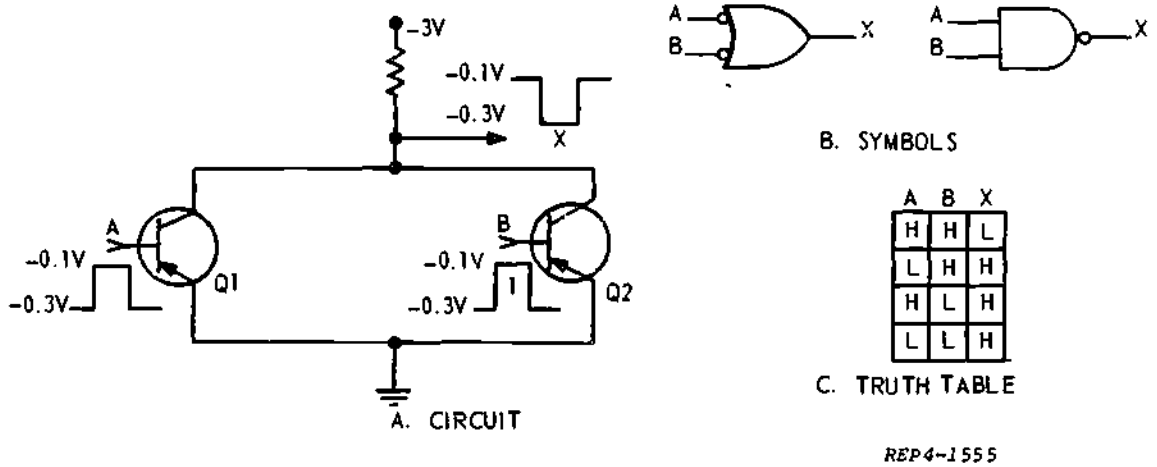


Figure 2-22. Parallel Gate

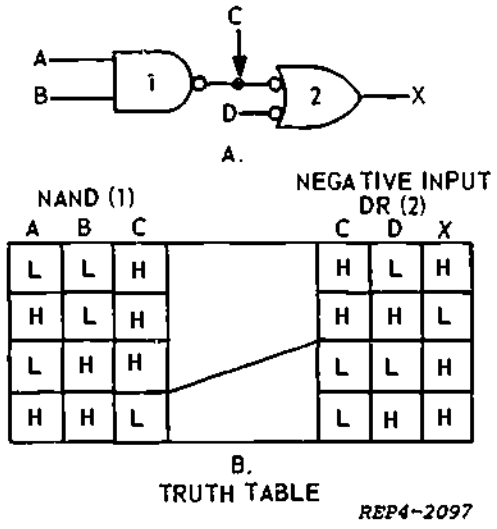


Figure 2-23. Combination of NAND and Negative Input OR Gates

2-70. Figure 2-23 shows the output of a NAND gate as one input to a negative input OR gate. If two highs are fed to the NAND gate, the gate provides a low output. This low will be inverted by the negative input OR gate and become a high at output X. A low input at D will also be inverted and become a high output at X.

2-71. The truth table, figure 2-23B, shows the NAND and negative input OR functions separately. Compare the truth table with the symbol (figure 2-23A) and you will see that an H or L output from the NAND gate (C) can combine with either an H or L input (D) to the negative OR gate.

2-72. SERIES GATE. The circuit of a series gate is illustrated in figure 2-24A. The transistors conduct with -0.3V on both bases.

2-73. If the inputs at A and B are both low, the output is high. If either input is high, the output is low. If both inputs are high, the output is low.

2-74. From these facts we can conclude that a series gate can be a negative input AND gate or a NOR gate.

2-75. Figure 2-24C shows the series gate truth table. Verify the truth table by analyzing circuit operation with -0.3V as L and -0.1V as H. An H input puts reverse bias on the transistor. When both transistors conduct (two low inputs), the potential at X is -0.1V.

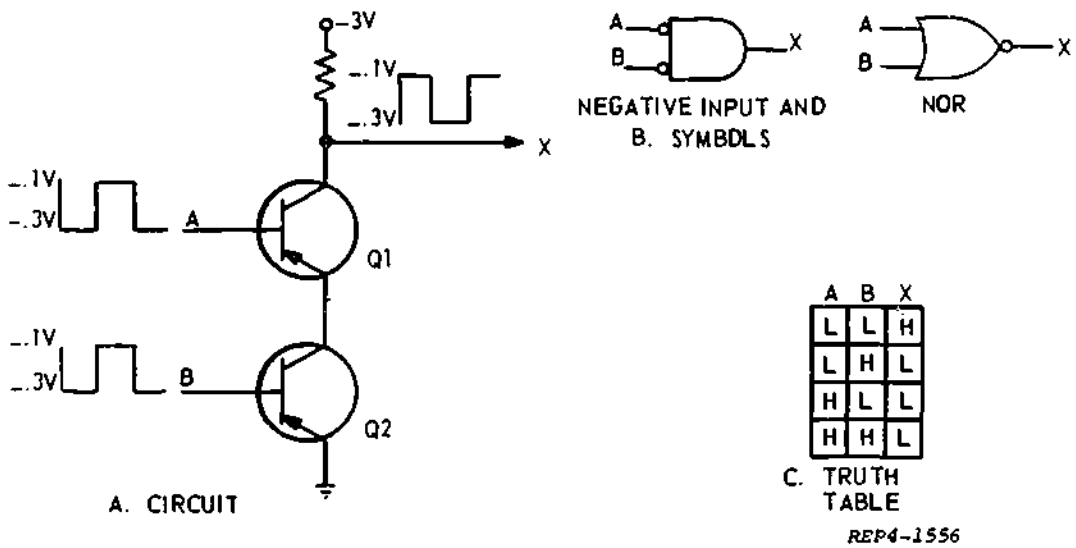


Figure 2-24. Series Gate

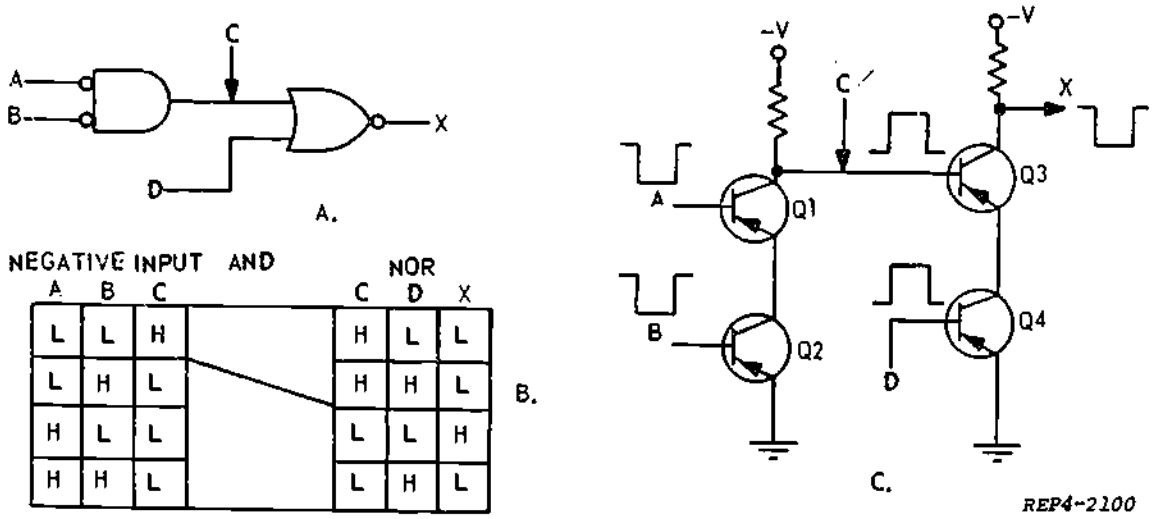


Figure 2-25. Combination of Negative AND and Positive NOR Gates

2-76. Series gates can be combined to illustrate both positive and negative inputs in one diagram, as in figure 2-25. Verify the truth table by comparing it with the symbols and circuit. Observe that there are eight possible combinations for four possible outputs at X in the truth table.

2-77. NPN DCTL Gates

2-78. NPN transistors can also be used in parallel and serial DCTL gates; however, it should be pointed out that when NPN transistors are used the gate will function as a different logic circuit than when using PNP transistors. When NPN transistors are used in DCTL gates the logic levels will be as follows:

HIGH = + 0.3V

LOW = + 0.1V

2-79. Figure 2-26 shows a parallel DCTL gate using NPN transistors with its corresponding truth table and logic symbols. When both inputs are low (0.1V), both transistors will be cut off and the output (X) will be high (0.3V). For any other input condition one or the other or both transistors will be conducting and the output will be low (0.1V). These conditions are shown in the truth table.

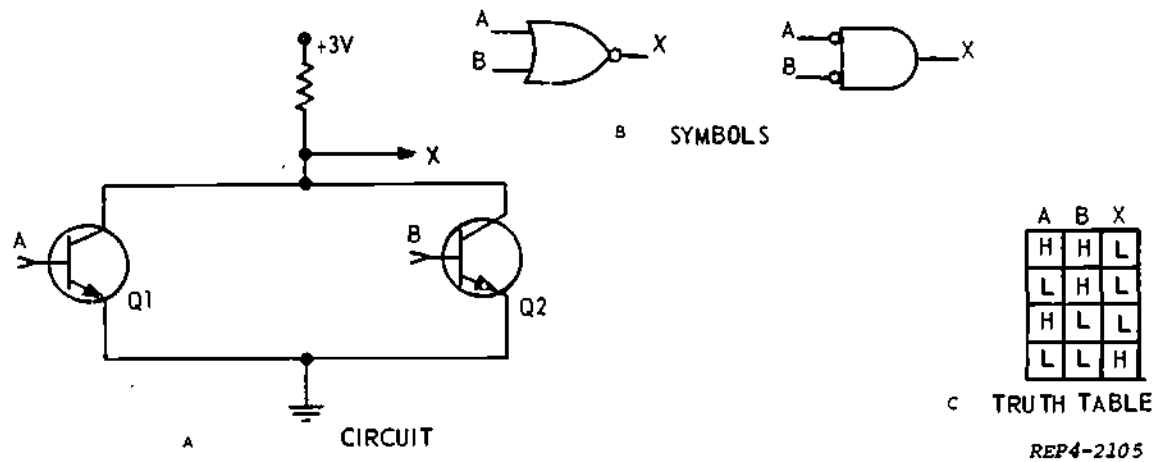
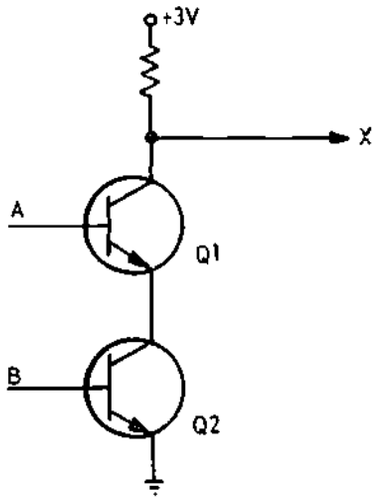


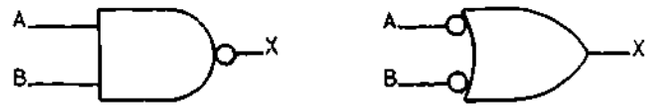
Figure 2-26. Parallel DCTL Gate



CIRCUIT

A	B	X
H	H	L
L	H	H
H	L	H
L	L	H

TRUTH TABLE



SYMBOLS

Figure 2-27. Series DCTL Gate

Notice that logically this circuit functions as a NOR gate or a negative input AND gate.

2-80. Figure 2-27 shows a series DCTL gate using NPN transistors with its corresponding truth and logic symbols. Notice that the transistors are connected in series; therefore, the only time there is a logic low at the output is when both inputs are high. For any other input condition one or both transistors will be cut off (not conducting) and the output will be high. The series DCTL gate using NPN transistors functions as a NAND gate or a negative input OR gate.

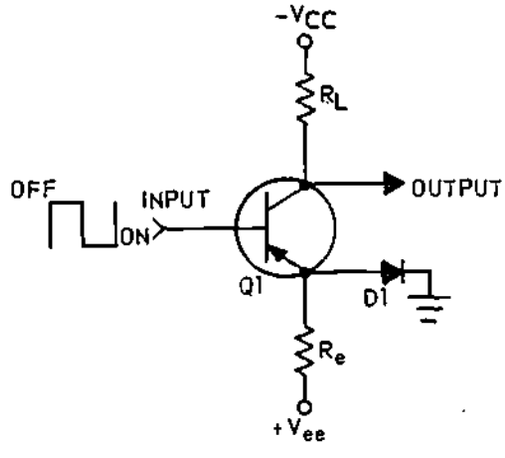


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Figure 2-28. Current Mode Logic Gate

2-81. Current Mode Logic (CML)

2-82. Another transistor logic circuit is shown in figure 2-28. The circuit is a form of emitter coupled logic, and is called Current Mode Logic. It is a nonsaturating current mode gate. The transistor does NOT operate at or near saturation. This eliminates a problem known as base storage and allows high speed operation. Base storage is a buildup of carriers in the base, and when the forward bias signal is removed the carriers continue to forward bias the transistor for a short time. Base storage occurs when operating a transistor at saturation.

2-83. Current mode refers to circuits with small signal level changes. Currents of near equal value switch from one path to the other.

2-84. In figure 2-28, if we apply a small positive to the base of Q1 the transistor will cut off. With Q1 cut off, diode D1 will turn ON. A simple series circuit exists with D1 and R_e. The resistance of D1 is small in comparison to R_e and, therefore, determines the current flow in this path. The positive voltage on the base of Q1 is just slightly more positive than the voltage on the emitter, and holds the transistor in cutoff.

2-85. To turn Q1 on, a small negative voltage is applied to the base. The current flow through Q1 now reverse biases D1 and cuts it off. The current path is now through R_L, Q1 and R_e. The forward bias for the transistor is limited so that there will be no significant change in current through R_e as a result of the switch. Thus, the transistor is prevented from saturating. We obtained the current mode of operation by switching a constant current from one path to another — from D1 to Q1.

2-86. Diode D1 can be replaced with a transistor in order to obtain complementary outputs. This variation is shown in figure 2-29. Notice, the base emitter junction of Q2 serves the same purpose as the diode.

2-87. Now refer to figure 2-30. Another transistor can be added and OR the input circuit. Q1 and Q2 make up the OR circuit, and Q3 serves the same purpose as the diode in figure 2-28. We now have an OR input Current Mode Logic Gate with complementary outputs. Refer to the truth table in figure 2-30B.

2-88. Deleted.

2-89. Boolean Equations

2-90. Use of symbols to express and analyze logic circuits is called Boolean Algebra.

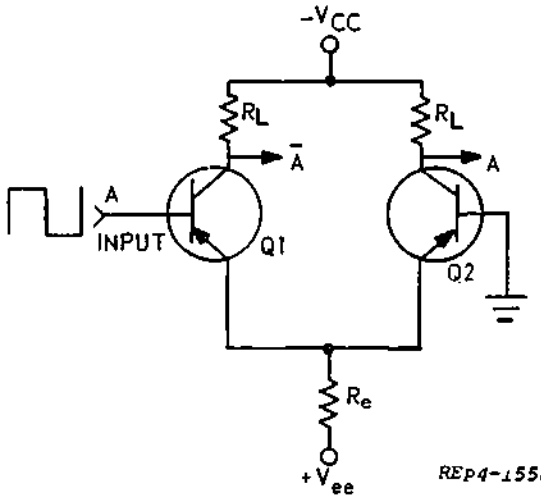
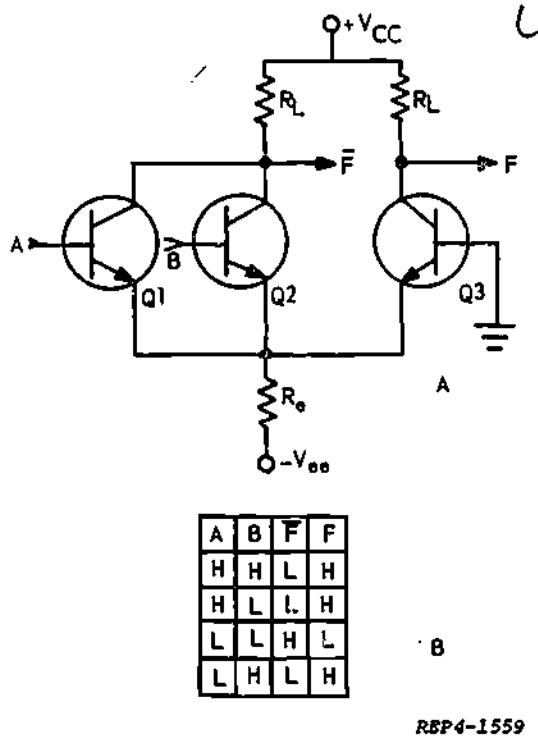


Figure 2-29. CML Gate with Complementary Outputs



A	B	F̄	F
H	H	L	H
H	L	L	H
L	L	H	L
L	H	L	H

Figure 2-30. OR Input CML

Boolean Algebra has rules which simplify computer function analysis. Boolean Algebra is well suited to electrical applications where current is flowing or not flowing. In addition to the binary number system, any system or device having two conditions can be represented by a Boolean Algebra equation.

2-91. Boolean Algebra simplifies the detailed schematics of digital equipment so that a technician can "see the forest despite the trees." Boolean Algebra has proven to be a great asset in troubleshooting.

2-92. Deleted.

2-93. All logical diagrams and Boolean equations in the Boolean logic system consist of three basic logical functions. These three functions are the AND function, the OR function, and the NOT function. We will review these briefly before we consider more complex equations and diagrams.

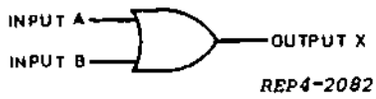


Figure 2-31. OR Gates

2-94. The OR gate performs the OR function. The OR gate has an output with any input (or when all of its inputs are present). Understand that the term "input" is opposed to a "no input" condition. There is either an INPUT or NO INPUT. The same is true with regard to the output; there is either an OUTPUT or NO OUTPUT. Figure 2-31 shows the logic symbol for a two input OR gate.

2-95. The basic rules for the two input OR gate are shown in figure 2-32.

2-96. Deleted.

2-97. Deleted.

2-98. Rule 1 in figure 2-32 states that A is NOT present and B is NOT present, so output X is NOT present. This follows the definition of the OR gate given earlier, which states: "With no input present, there will be no output from the OR gate." Rule 2 states X is present since A is present. Rule 3 states X is present because B is present. Rule 4 states X is present since A or B is present. Both inputs are not needed to produce X, since the definition for the OR gate states the OR gate will have an output when any of its inputs are present. Thus, the OR gate is an "any or all" gate.

2-99. AND Gate

2-100. The AND gate (figure 2-33) performs the AND function. The AND gate will have an output only when all of its inputs are present. If any of the inputs are absent the output will be absent. Thus, the AND gate is an "all or nothing" gate.

Figure 2-33. AND Gate

2-101. The basic rules for the two-input AND gate are given in figure 2-34. The rules are all of the combinations of input A and B with their corresponding outputs.

2-102. In rule 5, NOT A is present and NOT B is present, so NOT X is present. Rule 6 states that NOT A is present and B is present; therefore, NOT X is present. Rule 7 indicates that A is present and B is absent; therefore, X is absent. Rule 8 states that A and B are present; therefore, X is present.

2-103. Equations from Logical Diagrams

2-104. For the OR circuit of figure 2-31, the Boolean equation is written as A + B = X. Translating verbally, this becomes: "If inputs A OR B OR both are present, there will be an output X." Further, this output will exist as long as any of the inputs are present.

2-105. The Boolean equation for figure 2-33 is written as A·B = X, or AB = X. If the term is translated verbally, it becomes: "If, and only if, inputs A and B are present at the same time, there will be an output X." Further, this output will exist only for the duration of time that both inputs are present.

	A	B	X	
1.	0	0	0	READ AS: NOT A, NOT B = NOT X
2.	1	0	1	READ AS: A, NOT B = X
3.	0	1	1	READ AS: NOT A, B = X
4.	1	1	1	READ AS: A + B = X

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Figure 2-32. Boolean OR

	A	B	X	
5.	0	0	0	READ AS: NOT A, NOT B = NOT X
6.	0	1	0	READ AS: NOT A, B = NOT X
7.	1	0	0	READ AS: A, NOT B = NOT X
8.	1	1	1	READ AS: A·B = X

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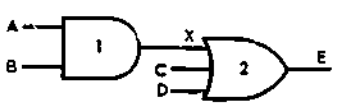
Figure 2-34. Boolean AND

2-106. When writing equations for logic diagrams which have an "AND" circuit feeding an "OR" circuit, or vice versa, a problem of grouping within the equation arises. A system which will allow systematic expansion of the functions within an expression is required.

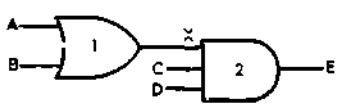
2-107. Figure 2-35A is an AND gate feeding an OR gate. This logic diagram is called an "OR Matrix." Only four primary inputs are involved; writing the equation for this diagram, however, is more complex.

2-108. Designating the output of the AND gate (1) in figure 2-35A as "X" simplifies the problem. The equation for the OR gate (2) is X + C + D = E. The equation for the AND gate is AB = X. Therefore, the equation for the output E is AB + C + D = E; this DOES describe the structure of the logic diagram.

2-109. Figure 2-35B shows an OR gate feeding an AND gate. This logic diagram is called an "AND Matrix." Similarly, there are still only four primary inputs involved. Again, we can simplify the problem by designating the output of the OR gate (1) as "X." The simplified equation for AND gate 2 becomes XCD = E: X taken by itself is stated as A + B = X. Combining the equation A + B with CD, directly, would result in A + BCD which gives a false impression of the overall structure. To ensure that logic diagrams are not misunderstood, signs of groupings must be used for the separation of terms. Thus the term A + B is placed within parenthesis (A+B) to indicate that A and B are to be combined in an OR gate before the complete quantity is combined in the AND gate with signals C and D to make up the output signal E. The correct equation becomes (A+B)CD=E. Other signs of grouping will be discussed as they are required.



A. OR Matrix



B. AND Matrix

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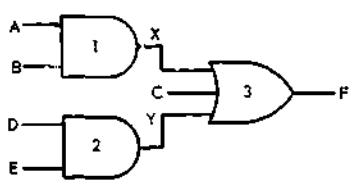
Figure 2-35. Simple Diagrams

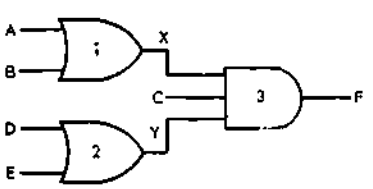
2-110. Figure 2-36A illustrates two AND gates feeding an OR gate. This is an OR matrix because the final gate is an OR gate. Therefore, in the same manner as before, the AND gate outputs may be designated as X and Y to simplify writing the equation.

2-111. The equation for OR gate 3 becomes X + C + Y = F. Working with the AND gates, AB = X and DE = Y. Substitute the quantities of X and Y in the overall equation. Thus, AB + C + DE = F. Note that the original structure is retained, and each AND function is treated as a single quantity.

2-112. Figure 2-36B illustrates an AND matrix. A simplified equation for AND gate 3 may be written as XCY = F. A + B = X, and D + E = Y. At this time substitute the quantities for X and Y in the overall equation. Remember, any time an OR gate feeds an AND gate, signs of grouping must be used to indicate the OR quantity. Thus, the final equation becomes (A + B)C(D + E) = F. Again, we retain the original diagram structure.



A OR Matrix



B. AND Matrix

Figure 2-36. Complex Diagrams

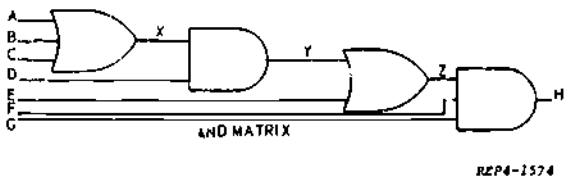


Figure 2-37. Complex AND Matrix

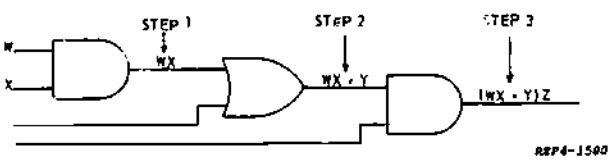
2-113. The diagram in figure 2-37 represents an AND matrix having three inputs. Letters X, Y, and Z are considered to be secondary inputs. Working in the same manner as before, the simplified equation becomes ZFG = H. In a step by step process, the final equation is developed as follows:

1. ZFG = H.
2. Y + E = Z; substitute for Z.
3. (Y + E)FG = H.
4. XD = Y: substitute for Y.
5. (XD + E)FG = H.
6. A + B + C = X: substitute for X.
7. $\left[(A + B + C)D + \overline{E}\right]$ FG = H. This is the complete equation for figure 2-37.

2-114. In step 5, we placed the OR function in parentheses to retain the given quantity: (XD + E). Within this quantity exists another quantity A + B + C, represented by X. To maintain identity and correct separation, the quantity of A + B + C requires grouping signs. The algebraic rule is to enclose the inner group in parentheses, and then place the total expression in brackets, as in step 7.

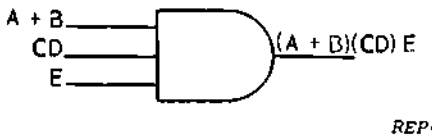
2-115. We can find the output expression for a large diagram using the following steps:

1. To find the output expression for a logic diagram, begin at left and find the output of each logic symbol.

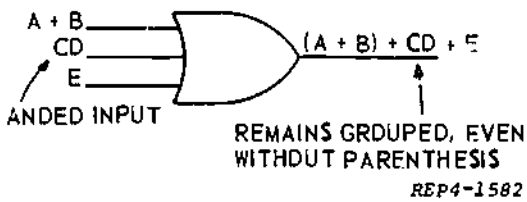


2. If a logic symbol is at the extreme left of the diagram, its inputs are single letters.

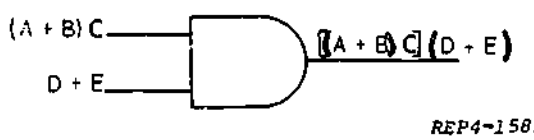
3. An input signal to any symbol NOT at the extreme left may be represented by two or more letters. These letters should remain grouped in the output expression.



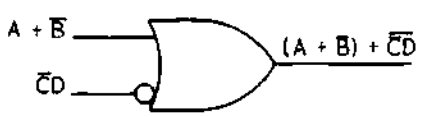
4. Parentheses are used to indicate grouping, except for an ANDed input to an OR or NOR logic symbol.



5. If additional grouping signs are necessary for an expression that already contains parentheses, use brackets.



6. The vinculum is used to group the portion or portions of the output expression that have been inverted.



2-116. Logical Diagrams from Equations

2-117. Simple equations, such as ABCD = E or A + B + C + D = E, offer no particular problem in drawing the correct logic diagram. Also, the equation (A+B)(C+D) = E should offer no problem, because it is an overall AND matrix with two inputs, each of which is an OR gate having two inputs. Following through in the manner previously explained, designate one OR quantity as X and the other as Y. The diagram becomes an AND gate with X and Y inputs. Then expand X and Y to show the complete structure. The diagram is shown in figure 2-38.

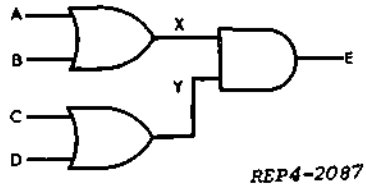


Figure 2-38. Complex AND Matrix

For the purpose of explanation, let's diagram the following equation step by step:

Equation: $[(A+B+C)(D+E)+F+G(H+I)]\ J = K$

Steps:

1. Identify the overall equation as a two-input AND matrix: J AND Z, where Z represents the quantity within the brackets.

2. Draw a logic symbol of an AND gate with J and Z inputs (figure 2-39).

3. Identify Z as a three-input OR gate:

$$(A + B + C)(D + E) + F + G(H + I) = Z$$

(Observe that three quantities are connected by two plus signs).

4. Draw an OR gate with the three inputs, W, F, and Y, where W represents (A + B + C) (D + E) and Y represents G(H + I), (figure 2-40).

5. Draw two AND gates, one for W and one for Y (figure 2-41).

6. Identify the two inputs to AND gate Y as G and V, where V represents (H + I).

7. Develop input V by drawing a two-input OR gate and labeling the inputs H and I (figure 2-42).

8. Identify the two inputs to AND gate W as U and T, where U represents A + B + C and

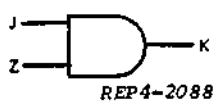


Figure 2-39. AND Gate for K

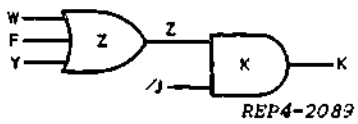


Figure 2-40. OR Gate for Z

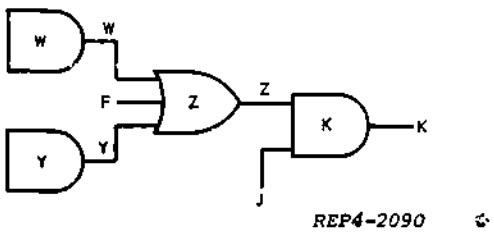


Figure 2-41. AND Gates for W and Y

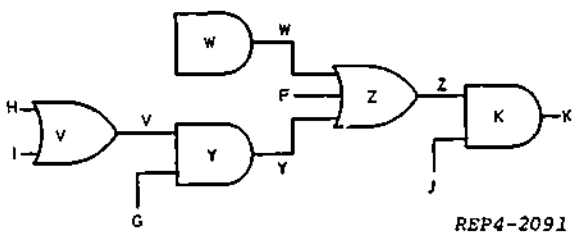


Figure 2-42. AND Input for Y and OR Gate for V

T represents D + E. Follow these steps using figure 2-43.

9. Draw the OR gate for U and label the inputs A, B, and C.

10. Draw the OR gate for T and label the inputs D and E.

2-119. The diagram is now complete as shown in figure 2-43. Check the completed drawing for errors by writing the Boolean equation from the diagram.

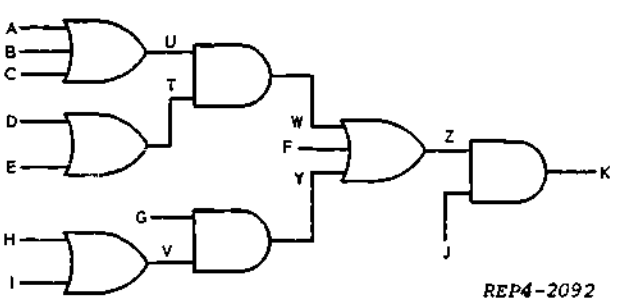
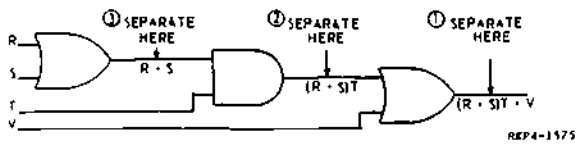


Figure 2-43. OR Gates for U and T

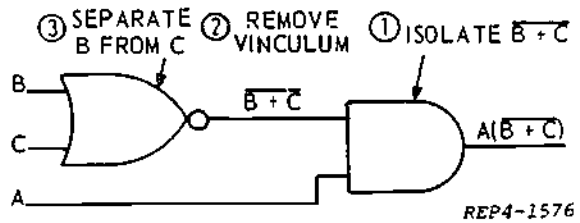
2-120. We can summarize how to construct a logic diagram from an output expression with the following.

1. Begin drawing at the right, and work left until all inputs are single letters.

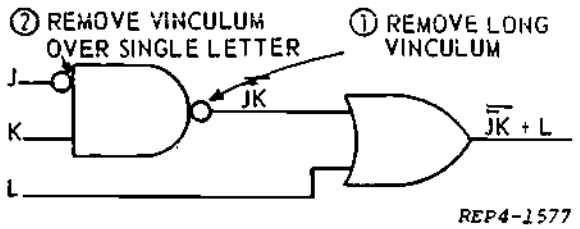
2. Never separate letters WITHIN a group until that group has been separated from the rest of the expression.



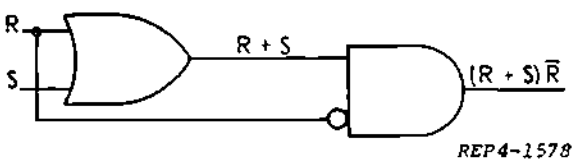
3. If an expression contains a vinculum, do not remove the vinculum until you have isolated this part of the expression from the rest of the expression, and do not separate the letters under the vinculum until you have removed the vinculum.



4. If a vinculum extends over more than one letter, use a NOR or NAND symbol to remove it. If a single letter is inverted, use a NOT symbol on the input.



5. If a single letter is an input to more than one logic symbol, connect input lines with a dot.



CHAPTER 3

LOGIC CIRCUITS AND DIAGRAMS

3-1. You have already learned how to add binary numbers using the rules of arithmetic. In this chapter you will analyze combinations of logic symbols to determine how digital equipment adds numbers by the use of adder circuits. We will discuss half adders, full adders, serial adders, and parallel adders. Next, the chapter discusses the role of multivibrators in digital circuits. The Schmitt trigger circuit is covered in detail. Included are symbols and applications of the various devices.

3-2. Deleted.

3-3. Half and Full Adder

3-4. The sum of two quantities is obtained by adding the digits in corresponding columns. If the sum of the digits in any column equals or exceeds the base number, a unit multiple is carried to the next higher column, with the remainder used in the answer for that column.

3-5. In binary addition, the sum of two zeros is 0, with no carry; the sum of a one and a zero is 1, with no carry; and the sum of two ones is 0, with a 1 (multiple of the base 2) carried to the next column. Logic circuits known as HALF ADDERS fulfill these conditions. In the half adder circuit of figure 3-1, a signal applied to either input A or input B, but not both, produces a signal at the sum output. A signal applied to both inputs produces a signal at the carry output. Figure 3-1 is expressed as:

$$\text{Sum} = (A + B)\overline{AB} \qquad \text{Carry} = AB$$

$$\text{Sum} = \bar{A}B + A\bar{B}$$

Observe that the half adder provides a sum or carry for two inputs only; it has no provision for adding more than two digits. The half adder is used to add the LSD column of two numbers.

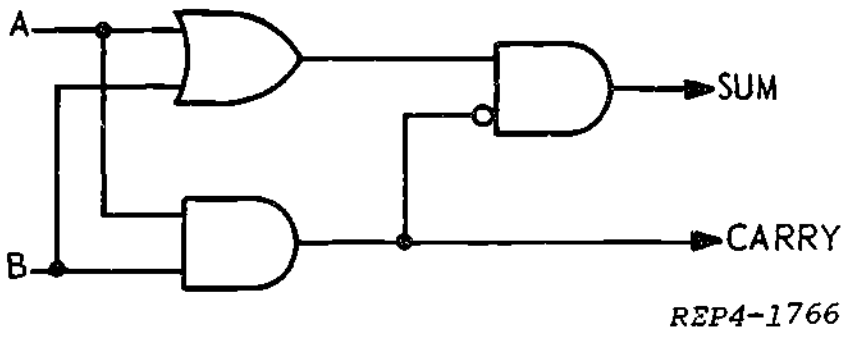


Figure 3-1. Half Adder

RULE →	(a)	(b)	(b)	(b)	(c)	(c)	(c)	(d)
A	0	1	0	0	1	1	0	1
B	0	0	1	0	1	0	1	1
C	0	0	0	1	0	1	1	1
SUM	0	1	1	1	0	0	0	1
CARRY	0	0	0	0	1	1	1	1

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Figure 3-2. Binary Addition (Three Numbers)

3-6. For all columns except the LSD column, a binary full adder must be able to handle three inputs—one for each of the digits being added and one for carry. Use figure 3-2 to apply the four rules for finding the sum of three binary digits (A, B, and C):

Rule (a) — If all three digits are zero, the sum will be 0 with no carry.

Rule (b) — If any digit is one and the others are zeros, the sum will be 1 with no carry.

Rule (c) — If two digits are ones and the other is zero, the sum will be 0 with 1 to carry.

Rule (d) — If all three digits are ones, the sum will be 1 with 1 to carry.

3-7. The four rules become:

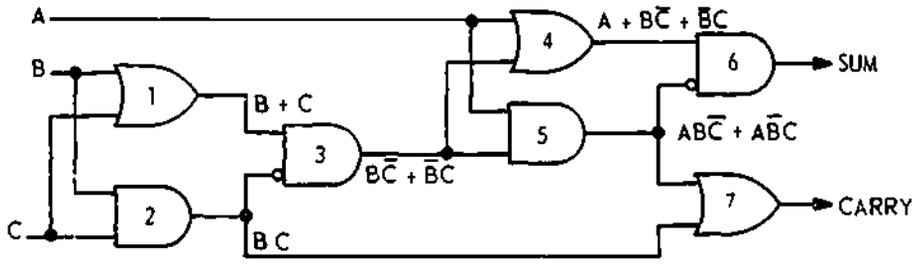
$$SUM = A\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}\bar{B}C + ABC$$

$$CARRY = AB\bar{C} + A\bar{B}C + \bar{A}BC + ABC$$

3-8. The preceding conditions are fulfilled by a logic circuit known as a FULL ADDER, which has three inputs and two outputs, as shown in figure 3-3. In this case, a signal applied to one input only produces a signal at the sum output. Signals applied to any two inputs produce a signal at the carry output. Signals applied to all three inputs produce signals at the sum and carry outputs. Compare figure 3-3 with figure 3-1 to see that a full adder, often referred to as an ADDER, consists of two half adders (1, 2, 3, and 4, 5, 6) and an OR circuit (7).

3-9. Trace the A, B, and C inputs of figure 3-2 through the diagram of figure 3-3. Your SUM and CARRY results should be as shown in figure 3-2.

3-10. Figure 3-4 shows a bank of adders arranged in parallel to produce the sum of two four digit binary numbers. Larger numbers can be handled by increasing the number of adders in parallel. Apply two four digit binary numbers to see how the parallel adder functions.



$$SUM = A\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}\bar{B}C + ABC$$

$$CARRY = AB\bar{C} + A\bar{B}C + \bar{A}BC + ABC$$

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Figure 3-3. Full Adder, Logic Diagram

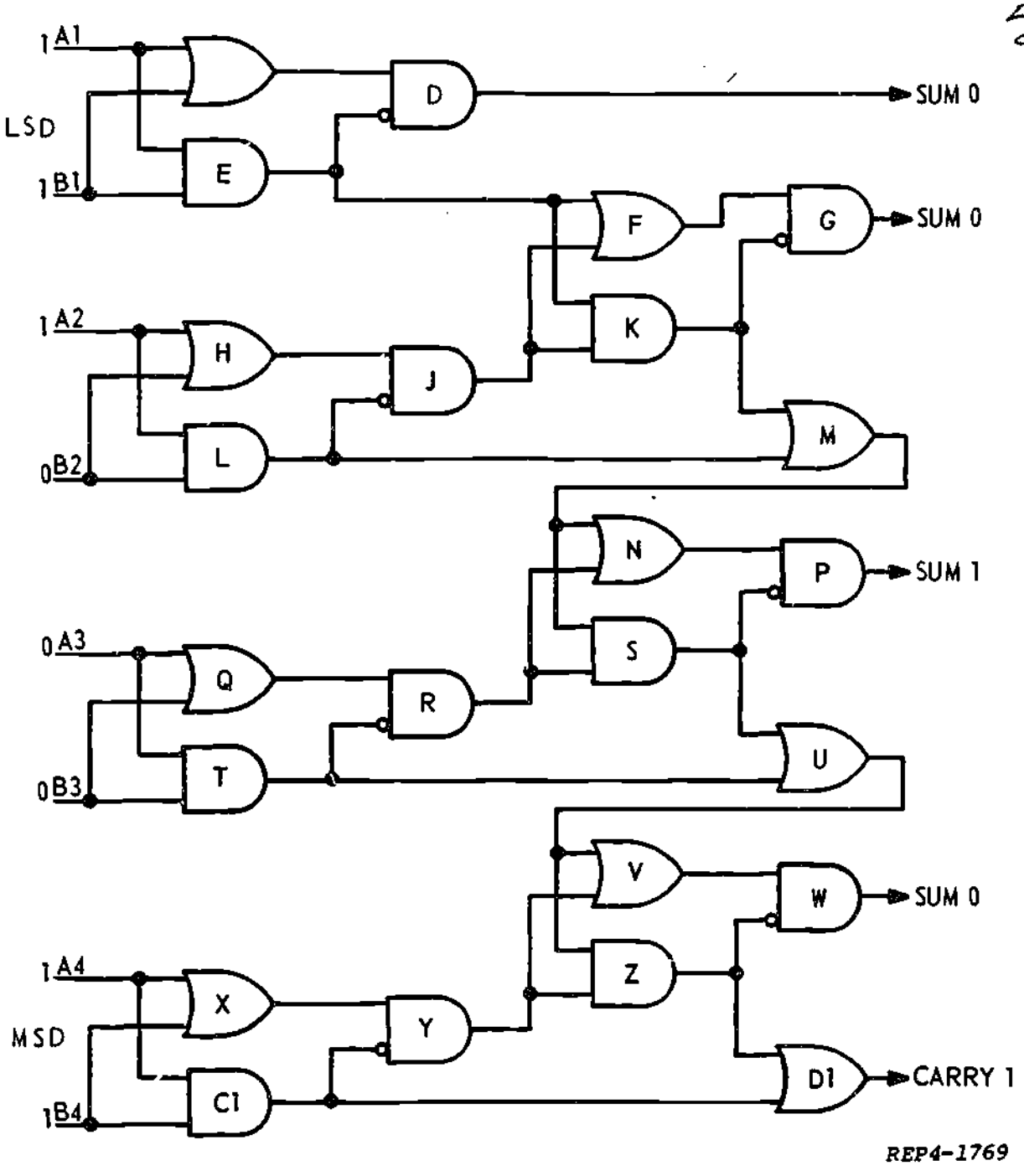


Figure 3-4. Four Bit Parallel Adder

3-11. Assume 1011 (A inputs) is being added to 1001 (B inputs). Inputs are in REVERSE order: the LSDs are held by A1 and B1, with the MSDs held by A4 and B4. The result of the addition is available at the output of D, G, P, W, and D1, with the MSD at D1.

3-12. Follow the addition through, beginning at A1 and B1, to verify the output; D is the LSD and D1 is the MSD. Observe that all adders work simultaneously; inputs are applied in parallel. The answer is 10100.

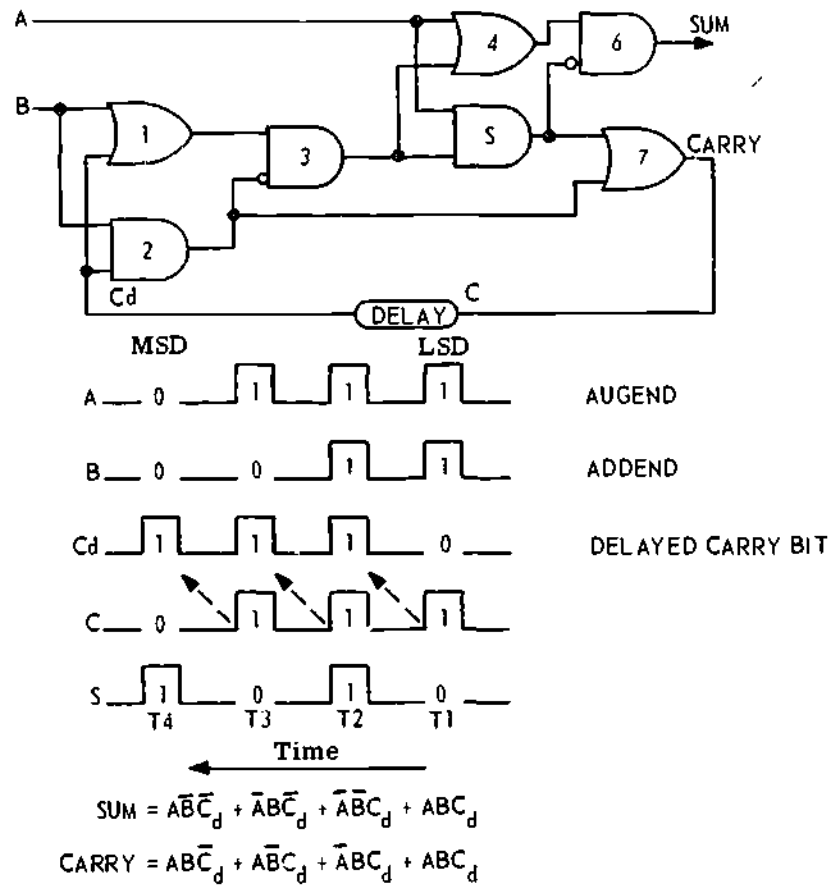


Figure 3-5. Serial Adder

3-13. It is possible to economize on equipment by applying the digit columns serially to the inputs of a single adder. Figure 3-5 shows an adder arranged for serial operation. Compare this logic diagram with figure 3-3. Notice that CARRY pulse C, if any, is delayed, and applied as Cd, in time coincidence with the digits of the next higher order column. The binary inputs proceed from right to left, with the LSDs applied first. AUGEND A is 111 and ADDEND B is 11. At time T1, inputs at A and B activate gates 1, 3, 4, 5, and 7, but not 6, so the first sum is 0 with 1 to carry. Carry pulse C is delayed and applied as the Cd input with inputs at A and B at time T2. Thus, at T2, three 1 inputs activate gates 1, 2, 4, 6, and 7, resulting in 1 at both the SUM and CARRY outputs. At T3, the delayed CARRY bit at Cd and the 1 at A activate gates 1, 3, 4, 5, and 7, making a CARRY input at T4. Therefore, the addition produces the SUM 1010. The pulse at T4 is the MSD.

3-14. Any portion of a digital computer can be designed for either parallel or serial operation, or a combination of the two. Parallel operation offers the advantage of higher processing speeds, while serial operation is more economical.

3-15. Logic Generators and Associated Circuits

3-16. Multivibrators are used extensively in digital circuits. You have studied three general types of multivibrators: astable, monostable, and bistable.

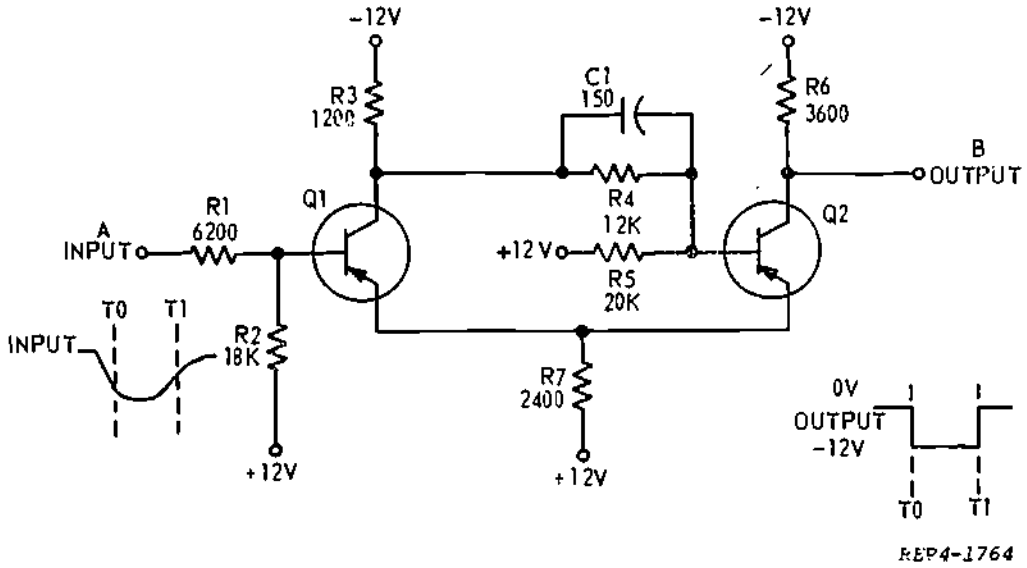


Figure 3-6. Schmitt Trigger Circuit

3-17. The astable multivibrator (also called the FREE RUNNING multivibrator) produces a continuous square or rectangular wave as long as power is applied to the circuit.

3-18. The bistable multivibrator (aiso called the Eccles-Jordan or flip-flop) produces half of an output cycle for each input trigger. Two triggers are necessary to produce a complete cycle. This multivibrator is the basic building block for the logic generator.

3-19. The monostable multivibrator (aiso called the one-shot multivibrator) is used in digital circuits for pulse stretching, pulse shaping, gate operation, and for providing adjustable delayed gates. This multivibrator is capable of producing severai different types of outputs.

3-20. Logic circuits make extensive use of the bistable and monostable multivibrators.

3-21. Schmitt Trigger Circuit

3-22. If the waveshape of a square wave signai degenerates to the point that it is rounded, a Schmitt trigger circuit may be used to furnish a sharp rectangular output pulse of approximately the same duration and phase as the input pulse. The Schmitt trigger circuit improves or restores the originai pulse waveshape.

3-23. In the quiescent state the input to the Schmitt trigger circuit, figure 3-6, is at 0 volts and Q1 is cut off. The voltage divider composed of R3, R4, and R5 divides the source voltages of -12 volts and +12 volts so that the base of Q2 is forward biased. Q2 will be saturated. The current through Q2 develops a voltage drop across R7 which reverse biases Q1 and keeps it cut off. In this condition, the output taken from the collector of Q2 is nearly 0 volts.

3-24. At time T0 the negative signai applied at A input (figure 3-6) has sufficient amplitude to bias Q1 on, and its collector goes toward 0 volts. This change is coupled to the base of Q2, and causes Q2 to cut off. The decrease in current through R7 reduces the reverse bias on Q1, causing it to saturate. The collector voltage of Q2 is now -12 volts.

3-25. The circuit remains in this state until T1, when the input voltage becomes less negative, decreasing to a vaiue that causes Q1 to start conducting less. The collector potentiai of Q1 starts in the negative direction. This change is coupled to the base of Q2 and turns it on. The increase in current through Q2 and R7 puts a reverse bias on Q1 which cuts Q1 off. As a result, Q2 conducts near saturation, and the collector voltage is near 0 volts.

3-26 Notice how the rounded input wave is converted to a square wave output between T0 and T1. The sharp rise and fall at the output is due to the feedback between Q2 and Q1. Any slight change in the conduction of Q1 is applied to the base of Q2 which, in turn, changes Q1 emitter voltage. Capacitor C1 speeds the transition from one state to the other.

3-27. Schmitt trigger circuits find applications as squaring circuits and as voltage level sensing circuits. Voltage sensing circuits are useful in warning or control circuitry. If the input voltage rises above or falls below a specified level, the Schmitt circuit produces an output which then actuates warning or correction circuitry.

3-28. Logic Symbols

3-29. Because some circuits are used so often in digital equipment, it is an advantage to represent them by symbols (as in the case of AND, OR, NAND, and NOR circuits).

3-30. The basic bistable (Eccles-Jordan) multivibrator is modified for use in digital equipment. The modified version is called a flip-flop (FF) and is represented by the logic symbols shown in figure 3-7.

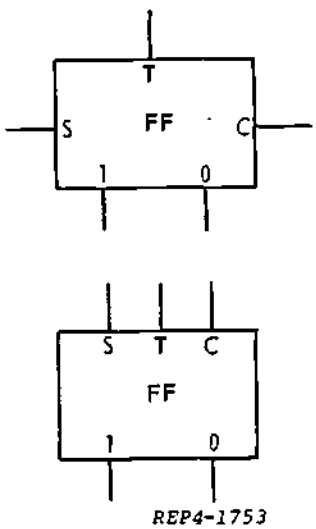


Figure 3-7. Flip-Flop Multivibrator Symbol

3-31. The FF is a device which stores a single bit of information. It has three possible inputs, set (S), clear (C), and trigger (T), and two possible outputs, 1 and 0. The S input is near the 1 output and the C is near the 0 output. When not used, the trigger input, T, may be omitted from the symbol.

3-32. The two outputs are normally of opposite levels—one high, the other low. A 1 is stored in the FF when the 1 output level is high and the 0 output level is low. A 0 is stored in the FF when the above condition is reversed.

3-33. The FF assumes the 1 state when a signal appears at the S input regardless of the original state. It assumes the 0 state when a signal appears at the C input regardless of the original stage. It reverses its state when a signal appears at the T input. There are several possible variations to normal FF operation when inputs are applied to more than one input simultaneously.

3-34. A modified version of the monostable multivibrator is the single shot (SS). The symbols are shown in figure 3-8. Output signal shape, amplitude, duration, and polarity are determined by the circuit characteristics of the SS and not by the input signal. Waveforms may be shown inside or outside the symbol. The unactuated state of the SS is either zero or one. When actuated, it changes to the opposite state and remains in the opposite state for the duration of the pulse of 0.5 microsecond, as shown in figure 3-8.

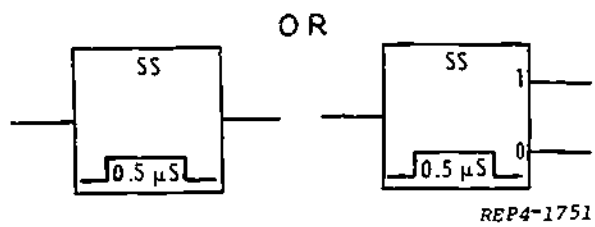


Figure 3-8. Single Shot Multivibrator Symbols

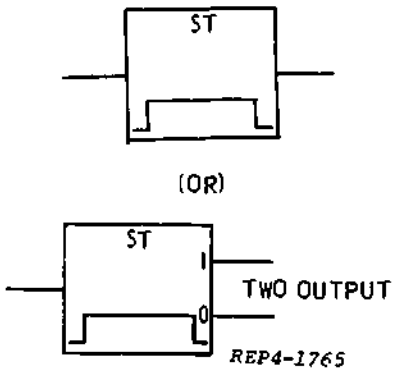


Figure 3-9. Schmitt Trigger Symbols

3-35. The Schmitt trigger (ST) function symbols are shown in figure 3-9. The ST is actuated when the input signal crosses a certain THRESHOLD voltage. Output signal amplitude and polarity are determined by the circuit characteristics of the ST and not by the input signal. Waveforms may be shown inside or outside the symbol, indicating amplitude, polarity, and threshold voltage. The unactuated state of ST is either zero or one. When actuated, it changes to the opposite state and remains in the opposite state as long as the input exceeds the threshold value.

3-36. Compare the symbols of the FF, SS, and ST. Notice how inputs and outputs are indicated. The FF symbol is rectangular in shape, and the SS and ST symbols are square.

3-37. Flip-Flop Circuits

3-38. Figure 3-10 is the schematic of a logic flip-flop with AND gate inputs. This flip-flop is basically an Eccles-Jordan multivibrator with modifications for use in logic circuits.

3-39. The following is the circuit analysis of this flip-flop: Q1 and Q2 are emitter followers for the output. CR1, CR2, CR3, and CR4 are clamping diodes that maintain the logic levels at 0V and -10V. The output from Q1 and Q2 may be used to ionize neon indicators to show the state of the flip-flop by visual inspection.

3-40. Q3 and Q4 form the actual multivibrator, Q3 is the 0 side transistor and Q4 is the 1 side transistor. R1 and R2 are collector load resistors. R2, R6, and R9 form the voltage divider network for biasing Q3. R1, R5, and R10 form the voltage divider network for biasing Q4. C1 and C2 couple fast changes to increase flip-flop switching speed.

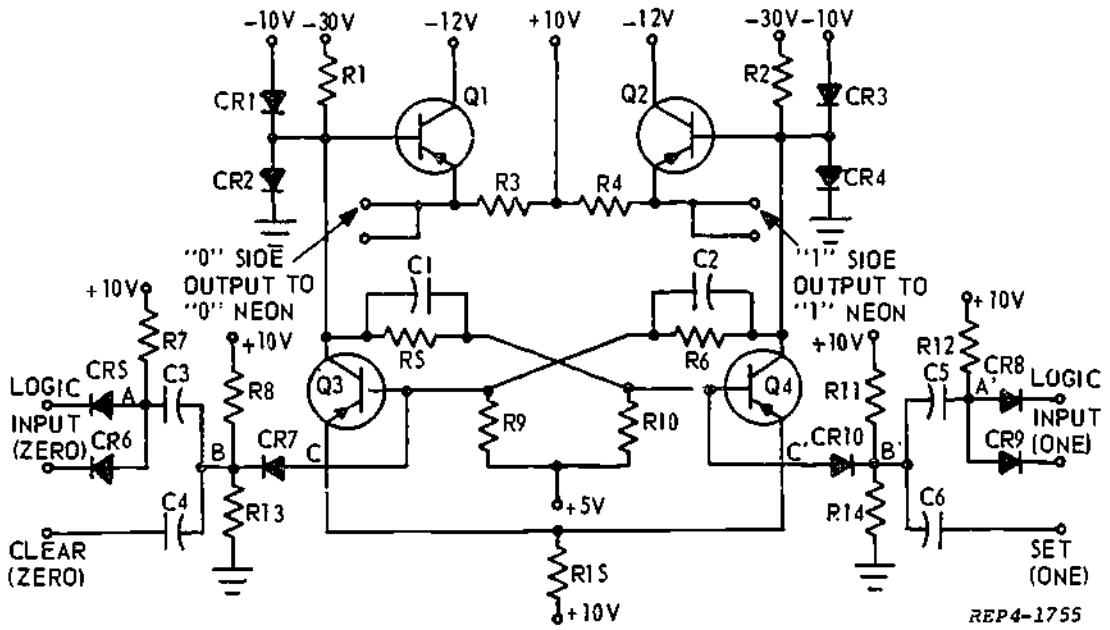


Figure 3-10. Logic Flip-Flop

3-41. The inputs to the flip-flop consist of SET (ONE) and CLEAR (ZERO), both of which bypass the LOGIC INPUT AND gates. CR5, CR6, and R7 form the AND gate that feeds the 0 side transistor and changes the flip-flop to the ZERO state. CR8, CR9, and R12 form the AND gate that feeds the 1 side transistor and changes the flip-flop to the ONE state. C3-R13 and C5-R14 differentiate the outputs of the AND gates. C4-R13 and C6-R14 differentiate the CLEAR and SET inputs. R8-R13 and R11-R14 form voltage divider networks that place a positive potential on the cathodes of CR7 and CR10. This positive potential holds CR7 and CR10 cut off until the negative spike of the differentiated wave is applied. CR7 and CR10 are called CLIPPING diodes.

3-42. While we trace this logic flip-flop through a cycle of operation, refer to both figures 3-10 and 3-11.

3-43. At T0, the flip-flop is in the ONE state; Q4 conducting and Q3 cut off. The 1 output is 0 volts and the 0 output is -10V. CR1 and CR3 are called CLAMPING diodes; they clamp the negative outputs at -10V.

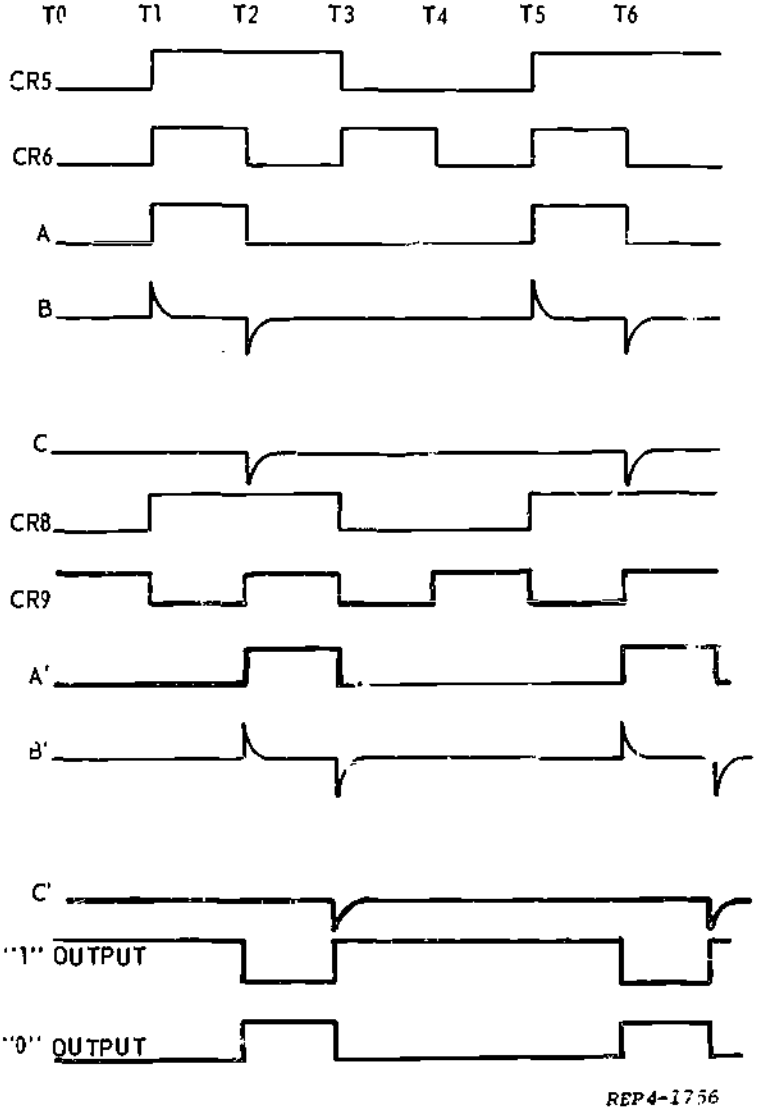


Figure 3-11. Logic Flip-Flop Waveshapes

3-44. At T1, signals are fed to CR5, CR6, CR8, and CR9 as shown by the waveforms of figure 3-11. The output of AND circuit CR5-CR6 will be high only when both inputs are high. The voltage at point A is shown as waveform A. This signal is differentiated by C3 and R13 and appears as waveform B across R13. The positive spike is eliminated from waveform B by limiter diode CR7, and negative trigger (waveform C) appears on the base of Q3. The negative trigger applied to Q3 makes it conduct, and the collector potential of Q3 goes to 0V. This change is coupled to the base of Q4 and turns Q4 off, making the Q4 collector voltage go to -10V. This negative going change is coupled to the base of Q3 and keeps it conducting. At T2, therefore, the 1 output will be at -10V, and the 0 output will be at 0V. The flip-flop is in ZERO state until a trigger is applied to Q4 at T3. From time T2 to T3 the inputs to CR8 and CR9 will be high and the output of the AND circuit will be high (waveform A'). The output will be high only when both inputs are high. The waveform at A' is differentiated by C5 and R14 and appears as waveform B' across R14. CR10 eliminates the positive spike and a negative trigger appears at the base of Q4 (C'). At time T3 the negative trigger will turn Q4 on and cut Q3 off, which returns the flip-flop to the ONE state.

3-45. In summary notice that:

1. Q3 is the 0 side transistor.

2. Q4 is the 1 side transistor.

3. In the ONE state, Q3 is cut off and Q4 is conducting.

4. In the ZERO state, Q3 is conducting and Q4 is cut off.

5. If the flip-flop is in the ONE state, the negative trigger applied to Q3 will change the flip-flop to the ZERO state.

6. If the flip-flop is in the ZERO state, the negative trigger applied to Q4 will change the flip-flop to the ONE STATE.

7. The FF changes state on the downclock (negative going edge) of the input signal.

3-46. The logic symbol in figure 3-12A is used when the AND gates are part of the flip-flop. The logic symbol in figure 3-12B is used when the AND gates are not part of the flip-flop. The logic symbol of figure 3-12C fits the schematic of the FF of figure 3-10 if the AND gates are separate from the flip-flop.

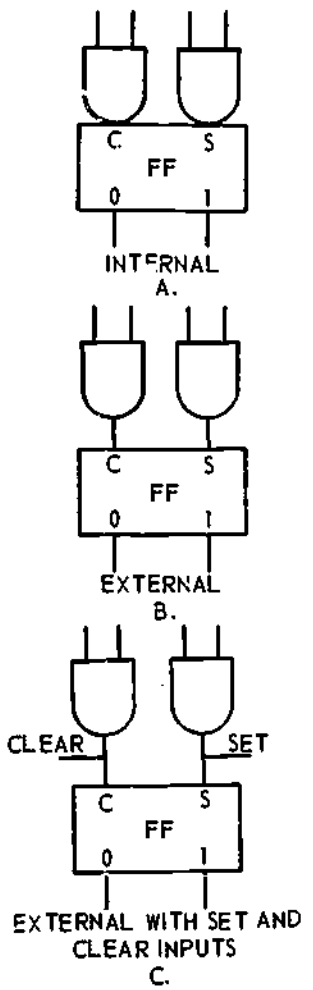


Figure 3-12. Logic Symbols for Flip-Flop

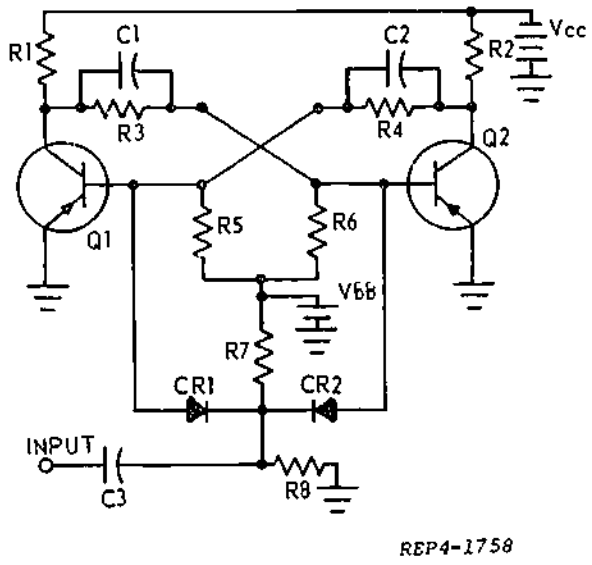


Figure 3-13.
Complementing Flip-Flop

3-47. A complementing flip-flop, shown in figure 3-13 is a bistable device which will accept input pulses from a common source and change from its existing state to the complement of that state each time it is triggered. For example, if it is in the ONE state, an INPUT trigger will switch the FF to the ZERO state, or vice versa.

3-48. With the input pulses applied simultaneously to both transistors, switching time would be delayed, which would cause the rise and fall times of the output signal to be longer. Pulse steering diodes CR1 and CR2 shown in figure 3-13 direct the input pulse to the transistor that is to be triggered into conduction. This prevents an increase in the rise and fall times.

3-49. The circuit shown in figure 3-13 requires negative input pulses. The circuit can be modified so that positive input pulses would be required.

3-50. In figure 3-13, resistors R7 and R8 form a voltage divider from V_{BB} to ground so that the cathodes of the pulse steering diodes are slightly positive with respect to ground. The anodes of CR1 and CR2 are at the base potentials of the transistors. The base of the conducting transistor is negative, and the base of the cutoff transistor is positive.

3-51. Let's assume that Q1 is conducting and that Q2 is cut off. In this state, CR1 has a relatively large negative potential on its anode; CR2 has a positive potential on its anode. This applies forward bias to diode CR2 and reverse bias to diode CR1. When a negative trigger is applied through coupling capacitor C3, the reverse bias on CR1 prevents the pulse from being applied to the base of conducting transistor Q1. Since diode CR2 is forward biased, the negative trigger pulse feeds through to the base of OFF transistor Q2, overcomes the positive bias on the base, and turns Q2 on. When Q2 turns on, Q1 turns off. The bistable multivibrator will remain in this state until the next negative trigger pulse is applied. This pulse will feed through CR1, apply forward bias to Q1 and cause the flip-flop to switch its state again. This input pulse does not couple to the base of Q2 because of the reverse bias on CR2.

3-52. The logic symbol for the complementing flip-flop is shown in figure 3-14.

3-53. A positive trigger pulse applied to the steering circuit of figure 3-13, regardless of the state of the flip-flop, is blocked by the diodes and cannot cause the circuit to switch.

3-54. For positive pulse steering, the diodes must be reversed, and a negative potential is applied to the voltage divider R7 and R8. A positive trigger pulse, therefore, is applied through the forward biased diode to the base of the ON transistor, driving it to cutoff. The reverse biased diode prevents the trigger

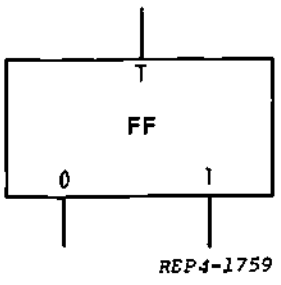


Figure 3-14. Complementing
Flip-Flop Logic Symbol

pulse from being applied to the base of the OFF transistor. Once the circuit switches state, the bias conditions of the diodes reverse, and a second positive trigger pulse is steered to the base of the ON transistor. A negative trigger pulse applied to this arrangement reverse biases the diodes and, therefore, has no effect on the circuit.

3-55. Figure 3-15 shows a complementing flip-flop circuit, with SET and CLEAR capabilities. This flip-flop is reduced to its most simple form. It consists of flip-flop transistors Q6 and Q7, and two steering gates consisting of Q1-Q2 and Q3-Q4. Input to the complementing flip-flop is the leading edge of a negative pulse (downclock), and the flip-flop changes state with each input.

3-56. In the following discussion, transistors Q6 and Q7 with their associated resistors and connections constitute the flip-flop. Transistors Q5 and Q8 serve as input switches.

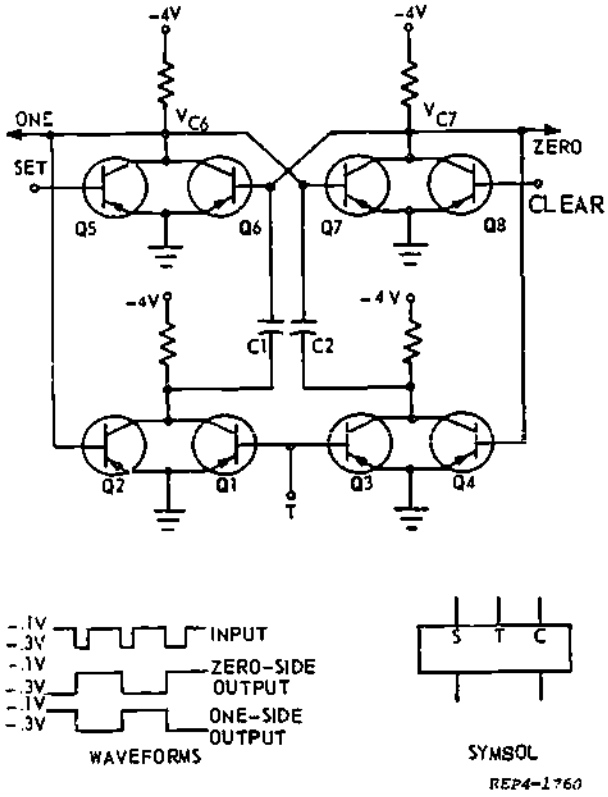


Figure 3-15. DCTL Logic Flip-Flop

3-57. In figure 3-15, suppose that Q6 is OFF and Q7 is ON. The collector voltage of Q6 is -0.3V and, applied to the base of Q7, keeps Q7 ON. Collector voltage of Q7 is -0.1V and keeps Q6 OFF. The flip-flop is in the ZERO state. A negative pulse applied to the SET input changes the flip-flop to the ONE state.

3-58. If a -0.3V pulse is applied to the base of Q5, Q5 conducts. The collector voltage of Q5 and Q6 becomes -0.1 volt, which turns Q7 off. Collector voltage for Q7 then becomes -0.3 volt, which turns Q6 on. The flip-flop is now in the ONE state. It can be reset to the ZERO state by a -0.3V pulse applied to the CLEAR input.

3-59. A negative pulse applied to the SET input always sets the flip-flop to the ONE state. A negative pulse applied to the CLEAR input always sets the flip-flop to the ZERO state.

3-60. With the flip-flop in the ONE state, the -0.1V on the collector of Q6 holds Q2 off while the -0.3V on Q7 holds Q4 ON. With no input, Q1 and Q3 are off. With Q1 and Q2 off, their collectors are at -4V. Capacitor C1 charges to the voltage difference between the base voltage (-0.3V) of Q6 and the collector voltage (-4V) of Q1-Q2 or 3.7V. The base of Q7 and the collectors of Q3-Q4 are at -0.1V, so C2 is uncharged.

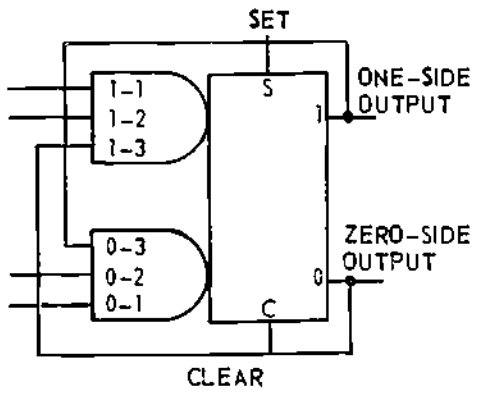
3-61. A negative pulse input (-0.3V) at terminal T turns Q1 ON. This grounds the negative terminal of C1 and impresses the capacitor voltage (3.7V) across the base emitter junction of Q6, turning Q6 OFF. When Q6 is cut off, the flip-flop goes to the ZERO state: C1 is discharged, Q3 and Q4 are OFF, and C2 is charged to 3.7V.

3-62. To summarize the operation of the flip-flop, start with it in the ONE state. Q6 is ON, Q7 is OFF, Q2 OFF, and Q4 ON. C1 is charged, and C2 is discharged. A negative pulse input at T changes the flip-flop to the ZERO state. Q1 is turned ON, Q6 OFF, Q7 ON, Q2 ON, and Q4 OFF. C1 is discharged and C2 is charged. Another negative pulse input changes the flip-flop back to the ONE state.

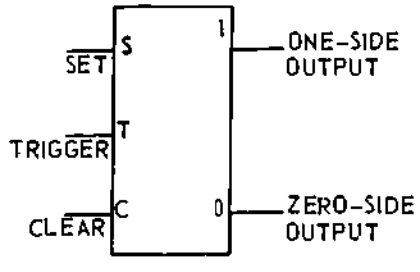
3-63. Actually, figure 3-15 is a direct coupled transistor logic (DCTL) circuit. DCTL circuits have two amplifier stages, connected as a bistable multivibrator. One part conducts and the other is cut off until an input trigger cuts off the conducting side and the cutoff side conducts. Steering circuitry allows the input to trigger one side only.

3-64. The circuits of figures 3-13 and 3-15 are complementing flip-flops because one input is required to change the output from a 1 to a 0, and vice versa.

3-65. The symbols used to represent complemented and complementing logic flip-flops with SET and CLEAR provisions are shown in figure 3-16. These symbols will be used in this text. Symbol A is an internal complemented flip-flop using AND gate inputs to the SET and CLEAR inputs. Symbol B is of the type already discussed. Notice the complementing flip-flop requires only one input to cause a change of state to occur, whereas the complemented flip-flop with its input AND circuitry may require any number of inputs prior to changing state.



A - COMPLEMENTED FLIP-FLOP



B - COMPLEMENTING FLIP-FLOP

REP4-1761

Figure 3-16. Flip-Flop Symbols

3-66. J-K Flip-Flop

3-67. The J-K flip-flop is a basic bistable multivibrator with certain modifications which make it extremely adaptable for digital circuits. It is the most extensively used of all the flip-flops because of its adaptability. It may be employed as an up or down counter, ring counter and storage or shift register. Figure 3-17 shows the logic symbol for the J-K flip-flop with direct set and clear (reset) inputs.

3-68. The condition (set or reset) of the J-K flip-flop is controlled by the inputs J, K, CP, S, and R. Inputs S and R are the direct set and reset inputs, respectively. Anytime one of these input levels goes low (downclock), the J and K inputs will be inhibited. If the set input (S) goes low, the set side output of the flip-flop (Q) will go high. When Q is high, $\overline{Q}$ will be low. If the reset input (R) goes low, the reset side output ($\overline{Q}$) will go high. When $\overline{Q}$ is high, Q will be low. In other words, inputs S and R make it possible to directly set or reset the flip-flop regardless of the input levels present at J, K, and CP.

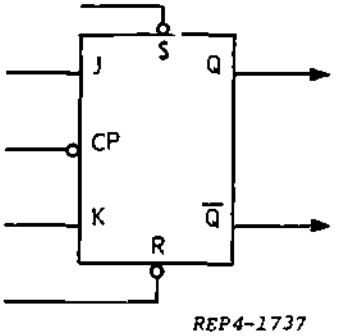


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Figure 3-17. Logic Symbol for J-K Flip-Flop

J	K	CP	FF
L	L	DOWN CLOCKS	NO CHANGE
L	H		RESET $\overline{Q}$ HIGH, Q LOW
H	L		SET $\overline{Q}$ LOW, Q HIGH
H	H		COMPLEMENT

REP4-2103

Figure 3-18. Truth Table for J-K Flip-Flop

3-69. When both direct set and reset inputs are high the condition of the flip-flop is determined by the gated input levels J and K and the clock pulse (CP). Refer to the truth table (figure 3-18) for the four possible input conditions at J and K.

3-70. The four possible conditions as shown in the truth table are:

1. When J and K are both low and there is a downclock at the CP input, the condition of the flip-flop will not change. That is, if the flip-flop was previously set, it will remain set; if it was previously reset, it will remain reset.

2. When J is low and K is high and there is a downclock at the CP input, the flip-flop will reset—Q will be low and $\overline{Q}$ will be high.

3. When J is high and K is low and there is a downclock at the CP input, the flip-flop will set—Q will be high and $\overline{Q}$ will be low.

4. When J and K are both high and there is a downclock at the CP input, the flip-flop will complement. That is, it will assume the opposite in which it was previously.

DECIMAL - NUMBER OF INPUT PULSES	BINARY - STATE OF FLIP-FLOP DCBA
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001
10	1010
11	1011
12	1100
13	1101
14	1110
15	1111 = MAXIMUM COUNT
16	0000 = CLEAR
17	0001 = COUNT STARTS OVER

REP4-2093

Figure 4-1. Count Table

CHAPTER 4

COUNTERS REGISTERS AND STORAGE DEVICES

4-1. Digital data processors and computers must convert pulse information into a usable form. This chapter tells how binary counters use the modified Eccles-Jordan bistable flip-flop as a prime component. Cascading flip-flop circuits enable the data processor to continually monitor the number of input pulses applied. Circuits performing the counter function are called COUNTERS. Circuits capable of storing information are called REGISTERS.

4-2. Counters

4-3. The two types of counters used extensively are the UP COUNTER and the DOWN COUNTER. The up counter counts in an upward direction and the down counter counts downward. Both types count pulses and can indicate when a certain operation is to be performed, or has been performed. Both types of counters can be composed of complemented flip-flops, and they differ only in the way in which the flip-flops are connected.

4-4. When using the up counter, the counter is usually cleared to all zeros, but it may be preset to any desired count. Each time a trigger signal is applied at the LSD flip-flop, the count in the counter is increased by one.

4-5. If a down counter is to be used, the counter is usually set to all ones, or it may be preset to any other desired count. Each input trigger applied to the LSD flip-flop reduces the count by one. The two counters described are both BINARY COUNTERS; that is, their outputs are binary numbers. Binary counters are further classified as SERIAL or PARALLEL counters. The serial counter will be discussed.

4-6. A serial binary counter consists of a group of flip-flops that are connected in series so that each flip-flop changes state as it receives a pulse from the preceding flip-flop. A square wave drives the LSD flip-flop; from now on, we will call this square wave the CLOCK signal. (See figure 4-2 for a serial counter.) The type of flip-flops used in the construction of the counter will determine if the up clock or down clock portion of the square wave is used.

4-7. The serial counter counts pulses one at a time. Each pulse applied to the counter input changes the state of one or more of the flip-flops in such a way that the binary configuration in the flip-flops represents the number of input pulses counted. Figure 4-1 gives a short list of equivalent numbers in decimal and binary notation for review.

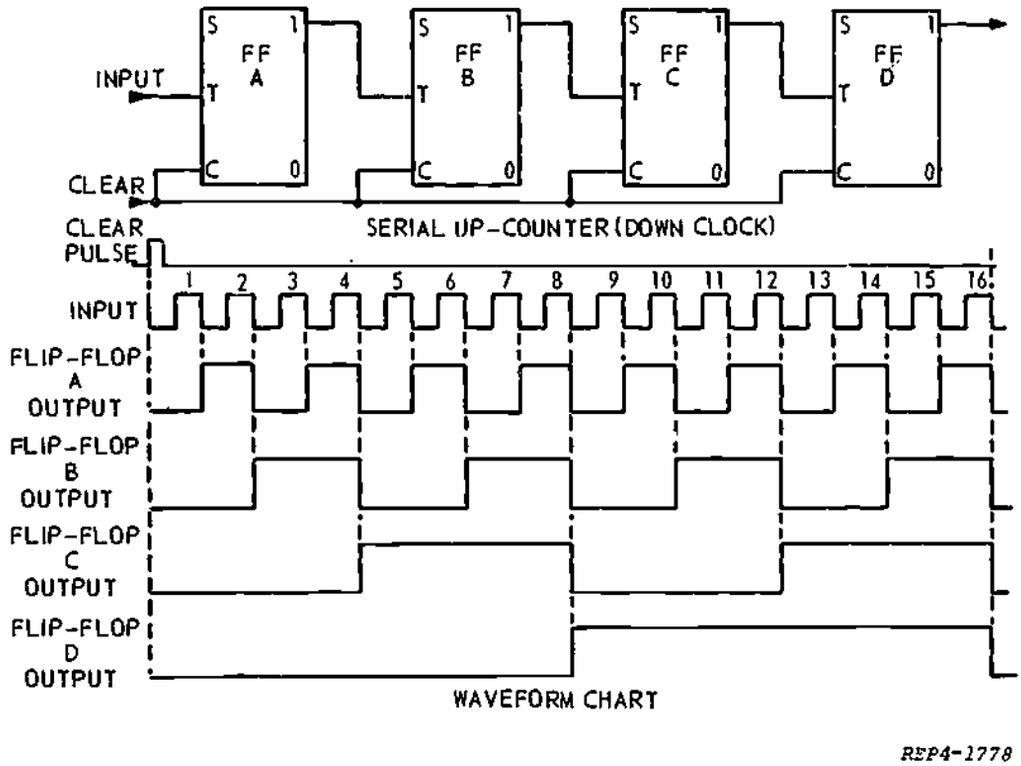

Figure 4-2. Serial Up Counter

4-8. In the counter in figure 4-2, each flip-flop represents a power of two. The output from each flip-flop is taken from the 1 side and fed to the trigger input of each succeeding flip-flop. This counter has 16 different possible states and, as each pulse is applied, the circuit makes a progressive transition from state to state. The 16th input pulse clears the counter to its original state. Recognize from the waveform chart that all flip-flops trigger on the down clock. Before the application of the first input, all flip-flops are cleared to the ZERO state.

4-9. The down clock of the first input pulse applied to flip-flop A causes a transition from the ZERO state to the ONE state. See the waveforms in figure 4-2. Flip-flop A is now in the ONE state. Flip-flop B is not affected because the flip-flop has felt only an up clock from flip-flop A. Since the flip-flops are insensitive to an up clock, flip-flop B remains in the ZERO state. The overall result of the first input pulse is that flip-flop A has changed to the ONE state, while all of the other flip-flops remain in the ZERO state.

4-10. The down clock of the second input pulse causes flip-flop A to return from the ONE state to the ZERO state. Flip-flop B now receives a down clock and changes from the ZERO state to the ONE state. Flip-flop C does not respond to the change in flip-flop B because flip-flop C receives only an up clock. The overall result of the application of the second input pulse is that flip-flop B is in the ONE state while all of the other flip-flops are in the ZERO state. In summary:

a. Flip-flop A changes state each time the input pulse down clocks.

b. Each of the other flip-flops makes a transition when, and only when, the preceding flip-flop changes from the ONE state to the ZERO state (down clock).

4-11. Only the down clocks are used. Each flip-flop goes through a complete cycle of operation for every two down clocks applied to it. Figure 4-2 has four flip-flops (A, B, C, and D) and maximum count is 15. The

maximum count of a serial counter may be extended by adding more flip-flops.

4-12. Figure 4-1 shows the resulting state of the flip-flops of the counter in figure 4-2 after a given number of input pulses. Note that the state of the flip-flops corresponds to the binary count of the number of input pulses. Thus, when seven pulses have been received by the counter, flip-flops A, B, and C are in the ONE state and D is in the ZERO state. The binary representation of seven is 0111. Remember flip-flop A contains the LSD and flip-flop D contains the MSD.

4-13. To determine the count in a serial counter, it is necessary to connect a meter, oscilloscope, or neon light to the individual flip-flops to determine the state of each flip-flop.

4-14. Figure 4-3 shows a four-stage serial up counter with corresponding waveforms. This counter uses complemented flip-flops. The waveform chart shows the trigger pulses and the clear pulse as well as the 1 side output waveshapes for flip-flops A, B, C, and D.

4-15. Deleted.

4-16. The operation of the counter is similar to the counter in figure 4-2. The count increases by one each time a trailing edge (down clock) of the input trigger pulse occurs.

4-17. In the serial up counter of figure 4-3, the 1 side output of each flip-flop feeds to both the 1 and the 0 side input AND gates of the next flip-flop. Since the flip-flops change state on the down clock of a pulse, a flip-flop in the counter can change state only when the voltage output of a preceding flip-flop goes from high to low. Initially all flip-flops are cleared to the ZERO state by the CLEAR pulse. If a trigger pulse is applied to LSD flip-flop A, the down clock will cause flip-flop A to go to the ONE state and represent a count of one in the counter. When flip-flop A is in the ONE state, a high is felt at both the ONE and ZERO inputs of flip-flop B.

4-18. The second input trigger pulse applied to flip-flop A causes it to go to the ZERO

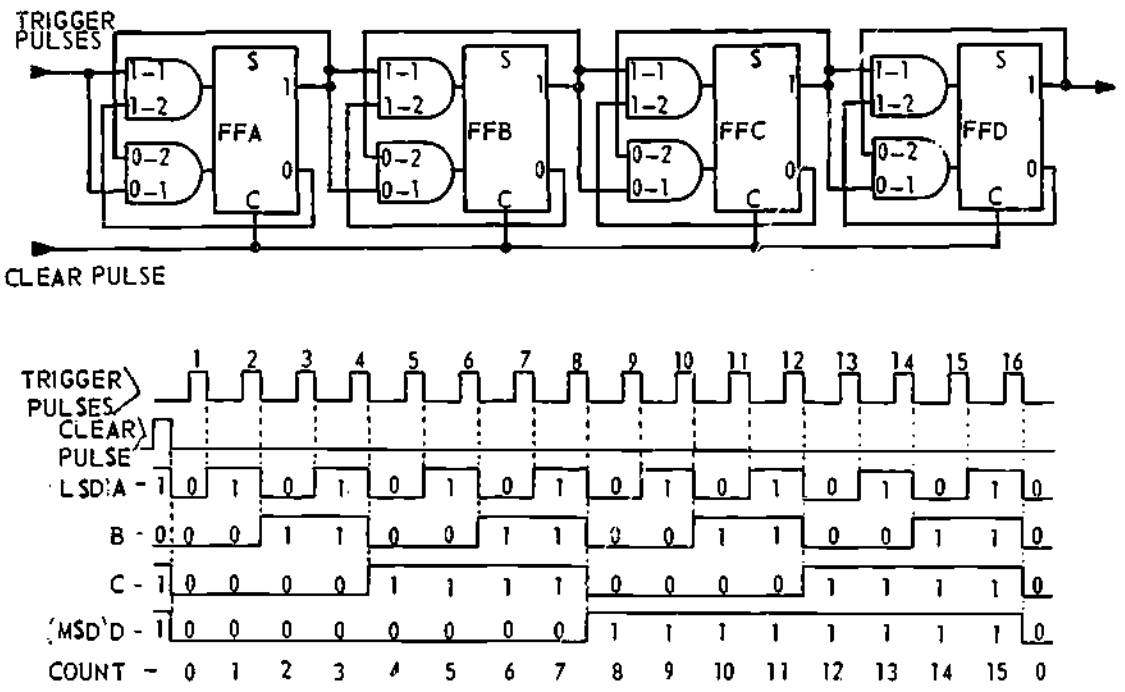

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Figure 4-3. Serial Up Counter and Waveforms

state. As the 1 side output of flip-flop A changes from a high to a low, it triggers flip-flop B to the ONE state. Flip-flop B now indicates that two pulses have been counted. The third trigger pulse causes flip-flop A to go to the ONE state. At this time both A and B are in the ONE state and three pulses have been counted. The 1 side outputs of flip-flops A and B are high. The down clock of the fourth trigger pulse will cause flip-flop A to change to the ZERO state. When flip-flop A changes to the ZERO state, its 1 side output down clocks, causing flip-flop B to change to the ZERO state. At the time flip-flop B changes from the ONE state to the ZERO state, its 1 side output down clocks. This causes flip-flop C to change to the ONE state. At this time, flip-flops A and B are in the ZERO state and flip-flop C is in the ONE state. Four pulses have been counted. This process continues with the application of more trigger pulses until all flip-flops are in the ONE state. When the 16th trigger arrives, all of the flip-flops are cleared to the ZERO state. (Recall that the maximum count of four flip-flops is 15.) The process will start over and will continue as long as trigger pulses are applied to LSD flip-flop A.

4-19. A counter designed to decrease its reading by one with each input trigger pulse is called a down counter. In a binary down counter the 0 side output from each stage feeds the next stage. See figure 4-4.

4-20. When a flip-flop makes the transition from the ZERO state to the ONE state, the 0 side output down clocks. The down clock from the 0 side output will cause a transition in the next flip-flop. The following rules apply for the down counter.

a. Flip-flop A makes a transition for each down clock of the input trigger pulse.

b. Each of the other flip-flops makes a transition when, and only when, the preceding flip-flop goes from the ZERO state to the ONE state.

4-21. When using the down counter, the counter is usually set to all ones, but it may be preset to any desired count. Each time a trigger pulse is applied to the LSD flip-flop the count in the counter is decreased by one.

4-22. For example (refer to figure 4-4), consider the number 15 which is $1111_{(2)}$. This configuration was placed in the counter by the down clock of the SET pulse.

4-23. The down clock of the first trigger pulse, following the SET pulse, will cause

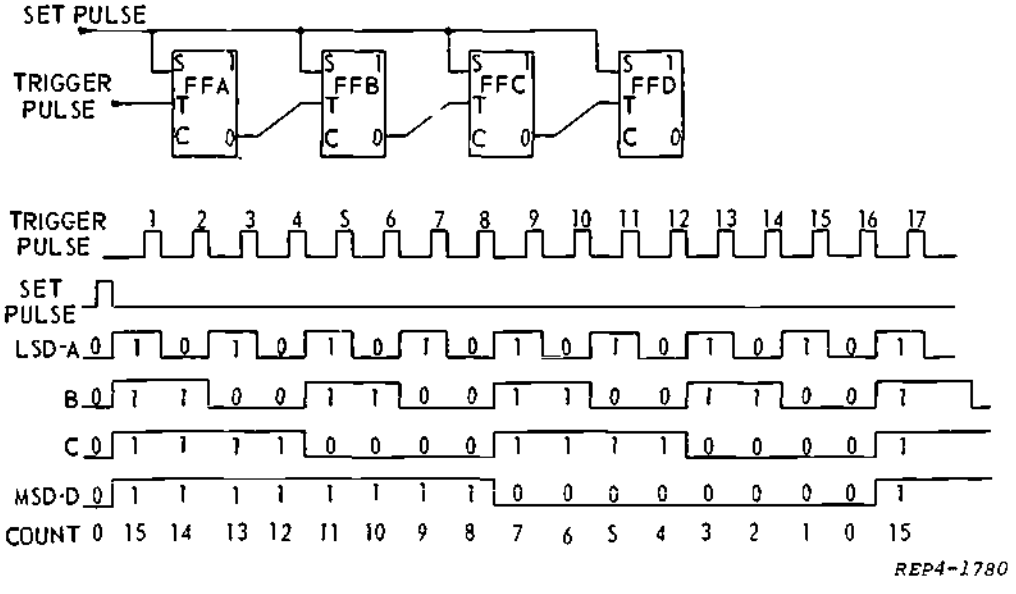


Figure 4-4. Serial Down Counter (Down Clock)

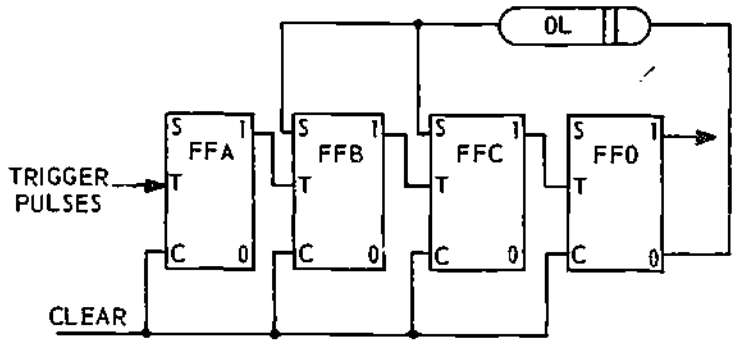


Figure 4-5. Decade Counter

flip-flop A to change to the ZERO state. An up clock is produced at the 0 side output of flip-flop A, which does not affect flip-flop B. Therefore, the new binary configuration is 1110. The counter retains this count until the next trigger pulse is applied.

4-24. The second trigger pulse will cause flip-flop A to change to the ONE state causing a down clock to be produced at the 0 side output of flip-flop A. The down clock is felt at the trigger input of flip-flop B. This causes flip-flop B to go to the ZERO state and produces an up clock at the 0 side output of flip-flop B, which has no effect on flip-flop C. Therefore, the counter has a new count of 1101.

4-25. This process will continue until all flip-flops are in the ZERO state, at the down clock of pulse 15. The 16th pulse will set all of the flip-flops to the ONE state and the process will start over. This continues as long as trigger pulses are applied to the LSD flip-flop.

4-26. Another type of counter is a decade counter. It is a four stage up counter with a feedback loop, designed to skip six counts so that it recycles to all zeros after the tenth trigger pulse.

4-27. A four stage counter will normally have 16 conditions in its truth table, whereas the decade counter will have only ten.

4-28. Refer to figure 4-5 and table 4-1 for an explanation of its operation. The clear pulse will initially put FFA through FFD in the ZERO state and the count is now zero.

4-29. For trigger pulses one through seven, the decade counter will operate the same as the serial up counter discussed previously. From the table, we see that after the seventh trigger FFA, FFB, and FFC are in the ONE state and FFD is in the ZERO state.

4-30. On the down clock of the eighth trigger input, FFA, FFB, and FFC will go to ZERO state and FFD to the ONE state. This will be felt as a down clock from the 0 side output of FFD, which is returned through the feedback circuit to the S inputs of FFB and FFC, placing them in the ONE state. Thus, the count in the decade counter is advanced to fourteen. From the table we see that counts eight through thirteen are skipped.

4-31. The purpose of the delay in the feedback loop is to insure that the eighth trigger

Table 4-1

TRUTH TABLE
FOR DECADE COUNTER

	A	B	C	D	
CLEAR	0	0	0	0	= 0
TRIGGER 1	1	0	0	0	= 1
2	0	1	0	0	= 2
3	1	1	0	0	= 3
4	0	0	1	0	= 4
5	1	0	1	0	= 5
6	0	1	1	0	= 6
7	1	1	1	0	= 7
8	0	1	1	1	= 14
9	1	1	1	1	= 15
10	0	0	0	0	= 0

has passed and FFB and FFC have gone to the ZERO state before the output of FFD will cause them to change states again. All this must occur before the ninth trigger arrives.

4-32. After the ninth trigger, the count will go to 15 and the tenth trigger will put the decade counter to all ZEROS again.

4-33. Another type of counter is the ring counter. The ring counter is a sequence counter with the output of the last stage connected to the input of the first stage. One of the stages is set to the ONE state, with the rest of the stages in the ZERO state. Each input pulse, then, moves the ONE state to the succeeding stage.

4-34. As with other type counters, there are a great many possible circuits for ring counters. Figure 4-6 shows a four stage ring counter. In this circuit, flip-flop A is placed in the ONE state and the other flip-flops are in the ZERO state by the clear pulse. Then flip-flop A is the only one whose output is a 1. Observe that the input signal is applied to the C (Clear) terminals on all flip-flops.

4-35. The down clock of the first input pulse changes flip-flop A to the ZERO state, but has no effect on the others, since they are already in the ZERO state. However, the change of flip-flop A from the ONE state to the ZERO state (feeding from 1 at A to S at B) causes flip-flop B to change (clock) to the ONE state.

4-36. In this manner, each input pulse clocks the flip-flop that is in the ONE state to the ZERO state, and the resulting change in state clocks the next flip-flop to the ONE

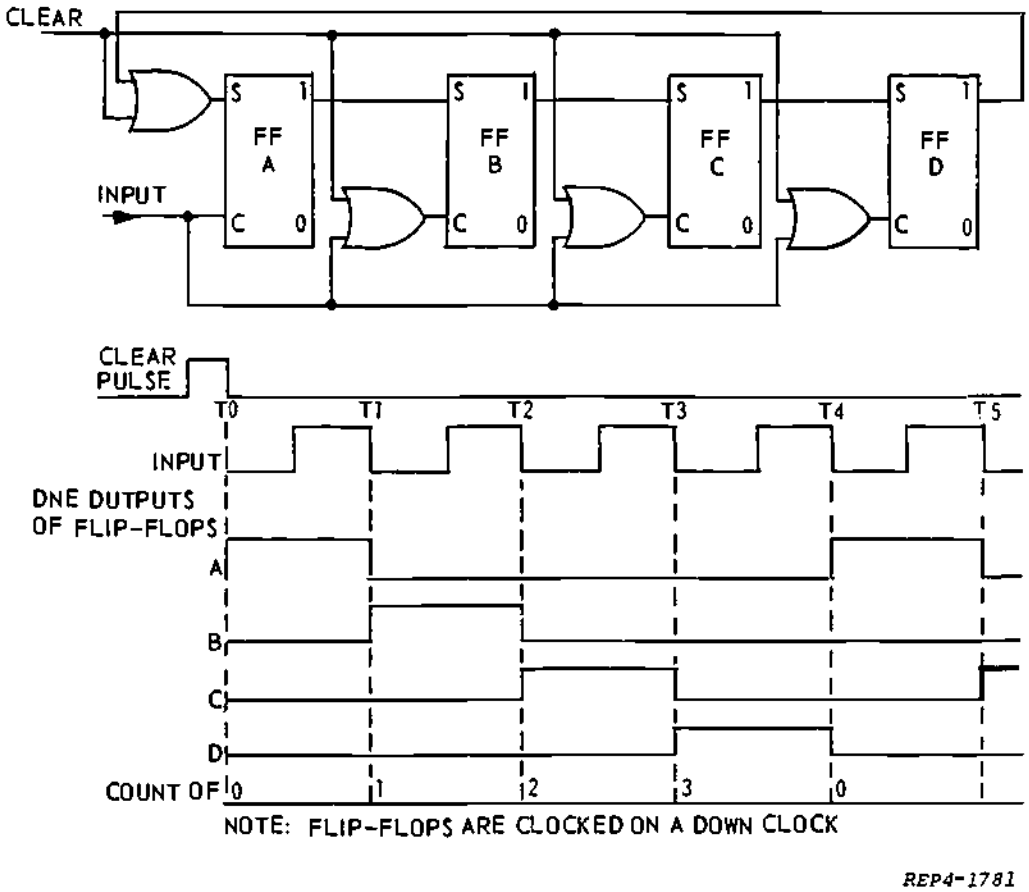


Figure 4-6. Ring Counter

state. Thus, as the input pulses continue to come in, the conditions of the flip-flops will be:

INPUT PULSE	D	C	B	A	COUNT
CLEAR	0	0	0	1	0
1	0	0	1	0	1
2	0	1	0	0	2
3	1	0	0	0	3
4	0	0	0	1	0
5	0	0	1	0	1

4-37. You can see from the waveshapes shown in figure 4-6 that one, and only one, flip-flop is activated (in the ONE state) at any particular time. Also, there are only four possible states. The four stage ring counter, therefore, has a maximum count of four. Four input pulses return the counter to its original state.

4-38. In digital machines, it is a common practice to assign one of the flip-flops the 0 count when it is in the ONE state, and assign the following stages the 1, 2, 3, etc., counts in sequence.

4-39. To illustrate, let us use the chart in paragraph 4-36 and figure 4-6 to assign flip-flop A the 0 count when it is in the ONE state. When the first input pulse down clocks at T1, flip-flop A changes from the ONE state to the ZERO state, and the output from its 1 side changes flip-flop B to the ONE state. A count of 1 is now registered in the counter, because flip-flop B is in the ONE state. Flip-flop C is clocked to the ONE state at T2 for the count of 2 and flip-flop D is clocked to the ONE state at T3, with the count of 3.

4-40. A unique characteristic of ring counters is that only one output from a single flip-flop output could TURN ON a single step of a series of sequential operations. A ring counter of the type discussed could control up to four steps, since it has four stages. It is simply a matter of adding or subtracting stages to arrive at any desired number of steps. For instance, a ring counter could have ten stages to represent 0 through 9.

4-41. Deleted.

4-42. Count Detect Circuits

4-43. Binary counters are capable of representing many combinations of information. These combinations or counts can be used to direct other equipment operations. A count detect circuit is used when it becomes necessary to determine the count in a counter.

4-44. The output of the count detect circuit can be used to initiate another action, or to indicate when an operation is finished. For instance, if we wanted to store for the first step, add for the second step, and read out for the third step, we could detect the step numbers and generate a control pulse to initiate each step.

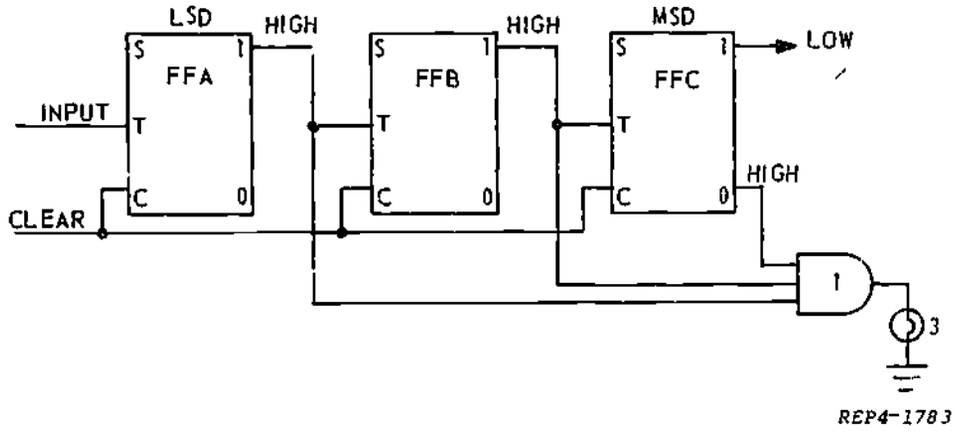


Figure 4-7. Count Detector

indicate when an operation is finished. For instance, if we wanted to store for the first step, add for the second step, and read out for the third step, we could detect the step numbers and generate a control pulse to initiate each step.

4-45. A count detect circuit for detecting a count of three is shown in figure 4-7. Flip-flops A, B, and C make a binary counter. Gate 1 is an AND gate with inputs from the ONE side of the flip-flops A and B, and the ZERO side of flip-flop C. The binary number 3 is represented by 011. This means that with a count of three in the counter, flip-flops A and B are in the ONE state, and flip-flop C is in the ZERO state. At this time, gate 1 has all of its inputs high so it will have an output. With any other count in the counter, the gate will not have an output.

4-46. To determine the proper connections that must be made to detect a certain number, write the desired number in binary form. A binary 1 represents a ONE side connection, and a binary 0 represents a ZERO side connection.

4-47. If we want to detect a count of five from the counter in figure 4-8, we start by writing 5 in binary notation (101 binary = 5). The AND gate must have connections to the ONE side of flip-flops A and C, and to the ZERO side of flip-flop B. (The input flip-flop is the LSD.)

4-48. If we wanted to generate control pulses, we could connect the count detect circuit as in figure 4-9. We want the equipment to add on the second count, and print out the fourth count. We know that 2 is 010, and 4 is 100. We simply connect the AND gates to the counter to detect these numbers.

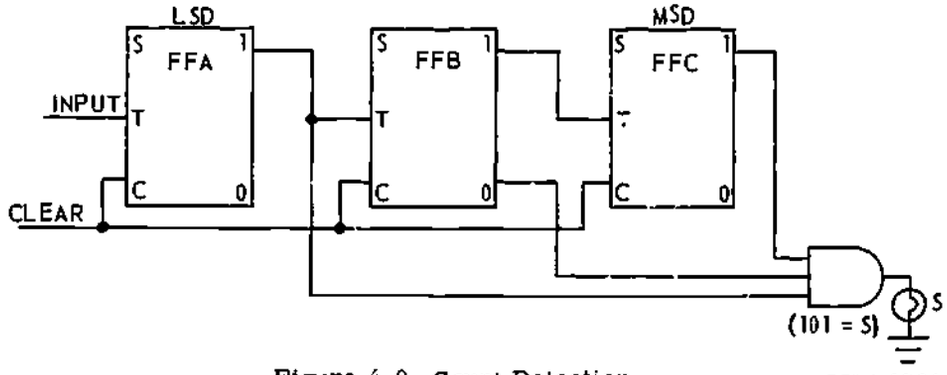
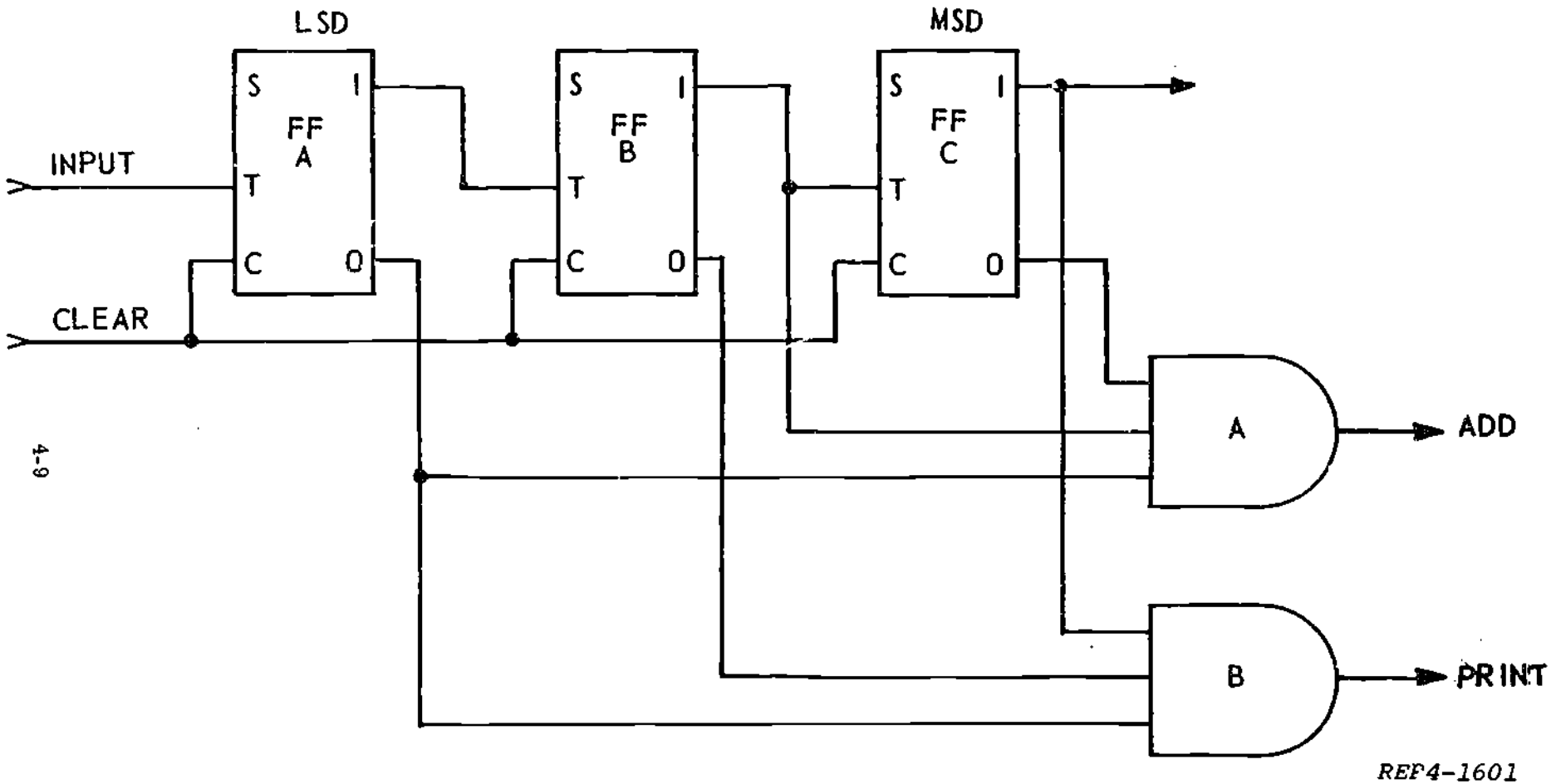


Figure 4-8. Count Detection



4-9

Figure 4-9. Count Detection

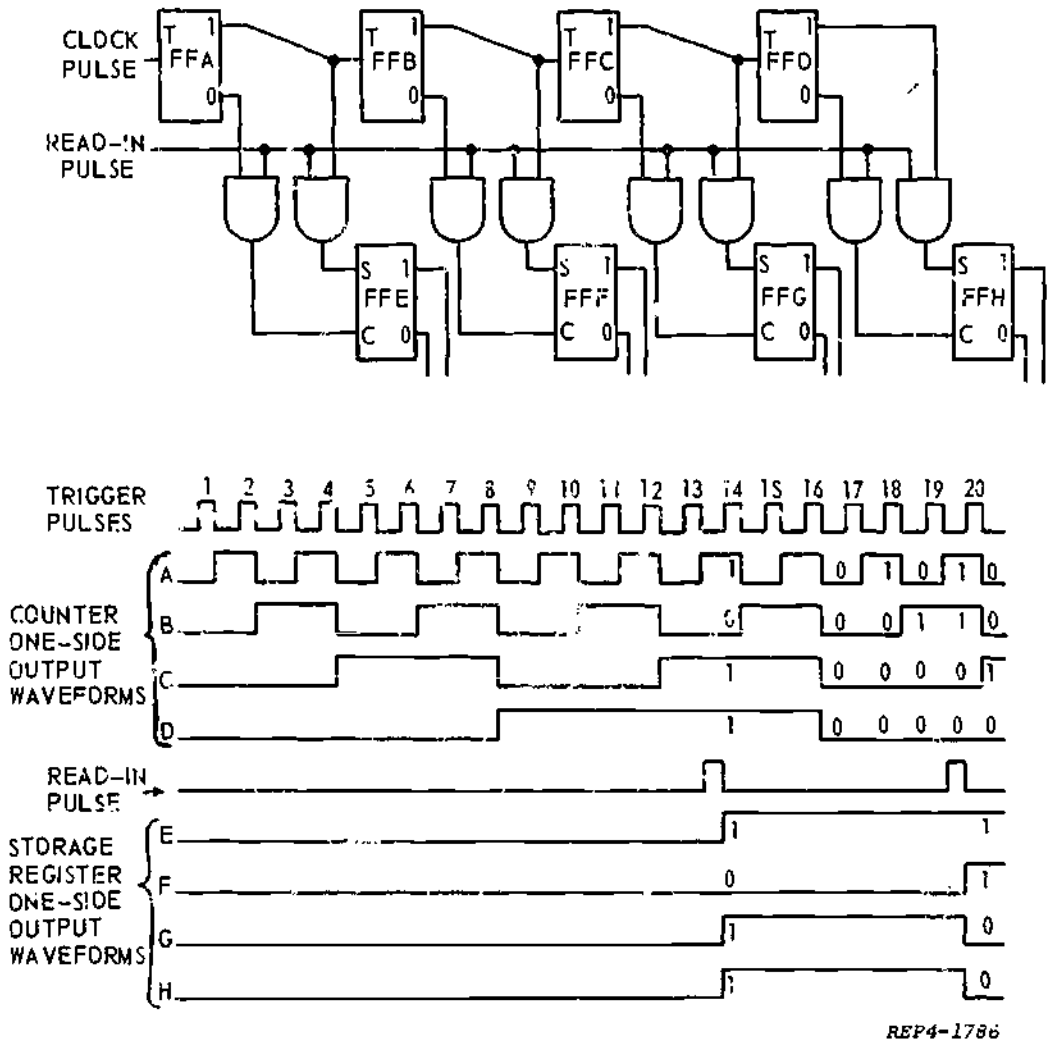


Figure 4-10. Parallel Storage Register with Waveforms

4-49. Registers

4-50. Digital equipments have facilities to store binary information for future use. The STORAGE REGISTER is composed of flip-flops and is used to store information for short periods of time. Each flip-flop in the storage register stores one BIT of binary data. Recall, a bit is a binary digit, and can be a 0 or a 1.

4-51. The circuit in figure 4-10 is a storage register connected to a serial counter. The count in the counter is transferred to the storage register by a READ IN pulse. After the count has been stored in the register, the counter can continue counting without affecting the storage register. The READ IN of a number to the storage register is rapid and can take place between counts in the counter.

4-52. The counter consists of flip-flops A, B, C, and D, while the storage register has flip-flops E, F, G, and H. Each of the flip-flops in the serial up counter has its 1 side output and its 0 side output connected through AND gates to the 1 and 0 side (set and clear) inputs of flip-flops in the storage register. In addition, a READ IN or transfer pulse is applied simultaneously to both the S and C AND gate inputs of all the flip-flops in the storage register.

4-53. Assume all flip-flops in the storage register are in the ZERO

state and 1101 is in the counter just before the read in pulse occurs.

4-54. Flip-flop A is in the ONE state, causing a high to be felt at one input of the S AND gate of flip-flop E.

4-55. Flip-flop B is in the ZERO state, causing a high to be felt at one input of the C AND gate of flip-flop F.

4-56. Flip-flop C is in the ONE state, causing a high to be felt at one input of the S AND gate of flip-flop G.

4-57. Flip-flop D is in the ONE state, causing a high to be felt at one input of the S AND gate of flip-flop H.

4-58. When the read in pulse up clocks, both inputs to the S AND gates of flip-flops E, G, and H, and the C AND gate of flip-flop F will be high. At the time the read in pulse down clocks, flip-flops E, G, and H will go to the ONE state and flip-flop F will remain in the ZERO state.

4-59. After the down clock of the read in pulse, the storage register contains the binary configuration that was contained in the counter. Thus, the number in the counter has been stored in the register. The number in the storage register can remain there, even though the counter continues counting, until a new read in pulse occurs. Compare the counter and storage register logic circuit with the waveforms (figure 4-10). The output from the storage register is sampled at the 1 and 0 sides of each flip-flop in the register and used as input signals to other circuits throughout the computer.

4-60. Figure 4-11A illustrates the symbol for a single four stage parallel register. It is necessary to indicate the number of bits or individual flip-flops in the register. In some applications, individual input and output lines are shown as in figure 4-11B.

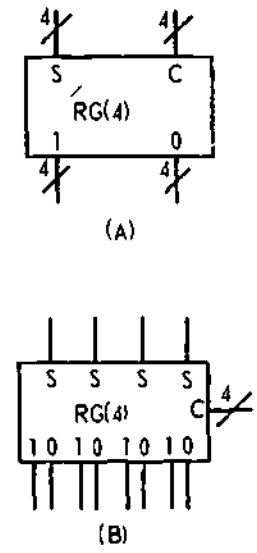


Figure 4-11. Multistage Storage Register Symbols

4-61. Another type of register is the shift register. Figure 4-12 illustrates a typical shift register with the input taken from a storage register. This shift register has a parallel input and a right shift serial output.

4-62. Using the diagram of the shift register in figure 4-12, notice that the output of each flip-flop is fed directly to the input of the following flip-flop. A shift register can have many more than three flip-flops, but the connections remain the same throughout.

4-63. Before the read in (transfer) pulse is applied, assume flip-flops A, B, and C are in the ZERO state and the storage register contains a binary count of five (101). With the above conditions existing, the transfer pulse is applied to AND gates 1, 2, and 3. At the time the transfer pulse down clocks (T0), flip-flops A and C are set to the ONE state. Flip-flop B remains in the ZERO state since AND gate 2 does not have two high inputs. The shift register and storage register now contain the same binary configuration of 101, as shown by the waveforms.

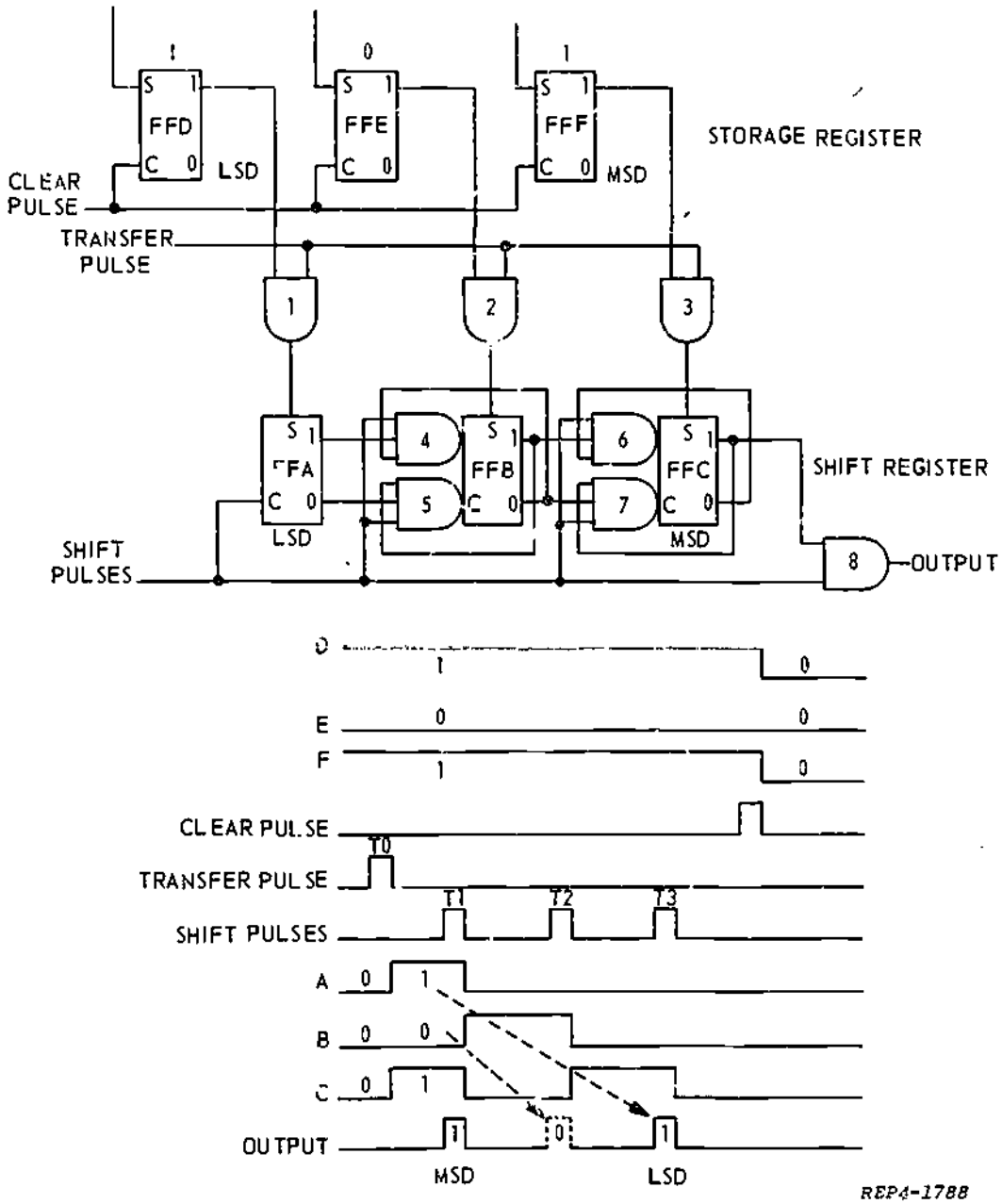


Figure 4-12. Shift Register

4-64. The output of flip-flop C is high and is one input to AND gate 8. When the shift pulse goes high at time T1, both inputs to AND gate 8 are high and the output goes high.

4-65. With the down clock of the shift pulse at time T1, flip-flop A changes to the ZERO state, flip-flop B changes to the ONE state, flip-flop C changes to the ZERO state, and the output goes low. Thus, one bit has been shifted out of the register. At time T1 the one bit in flip-flop A was transferred to flip-flop B. The zero bit in flip-flop B was transferred to flip-flop C and the one bit in flip-flop C was gated out of AND gate 8, leaving a binary configuration of 010 in the shift register.

4-66. With 010 in the shift register the only flip-flops that are activated for a change of state are flip-flops B and C. The output AND gate is held closed due to flip-flop C

being in the ZERO state. Thus, with the down clock of the T2 shift pulse, flip-flop A remains in the ZERO state, flip-flop C changes to the ONE state, and no output signal is produced.

4-67. However, the count in the shift register has moved one more place to the right and a zero bit (a no output signal with respect to the shift pulses) has been shifted through AND gate 8, leaving a binary configuration of 001 in the shift register. Flip-flop C and AND gate 8 are now activated. When the shift pulse is applied, an output from AND gate 8 appears. When the down clock of T3 occurs, flip-flop A and flip-flop B remain in the ZERO state, and a flip-flop goes to the ZERO state. At this time shift out is complete. You can see that one shift pulse is necessary to shift out each binary bit.

4-68. Let us review th action of the shift register.

1. Storage register had binary configuration of 101.

2. The shift pulse (T1) produced a one bit output and shifted the configuration to the right, with a remaining configuration of 010.

3. Shift pulse (T2) shifted the configuration to the right for the second time, and produced a zero bit output with a remaining configuration of 001.

4. Shift pulse T3 shifted the configuration to the right for the third time, and produced a one bit output with a remaining configuration of 000.

4-69. Figure 4-13 illustrates the two types of logic symbols used for the shift register.

4-70. The shift register symbol represents a binary register with provisions for displacing or shifting the contents of the register one stage at a time to the right or left by means of the SHIFT PULSE input.

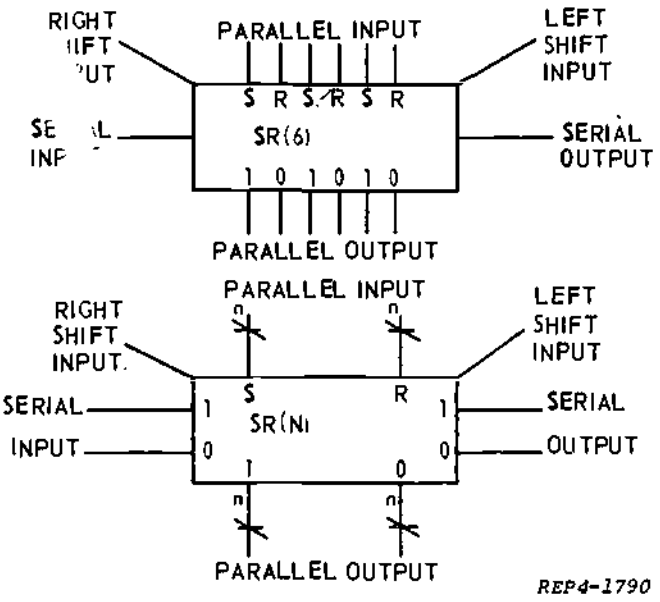


Figure 4-13.
Shift Register Symbols

4-71. The location of a shift pulse at the left corner of the symbol, indicates that the shift is from left to right. If the shift input is located at the right corner of the symbol, the shift is from right to left.

4-72. Other symbols usually associated with logic circuits include delay lines and amplifiers.

4-73. The amplifier symbols shown in figure 4-14 represent linear or nonlinear current or voltage amplifiers. These amplifiers may have one or more stages and may produce gain or inversion. Level changers and inverters, pulse amplifiers, emitter followers, relay pullers, lamp drivers, and shift register drivers are examples of devices for which this symbol is applicable.

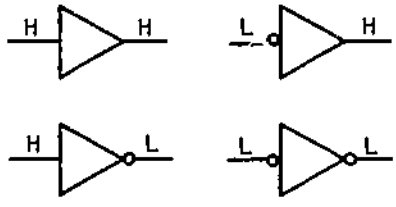


Figure 4-14. Amplifier Symbols

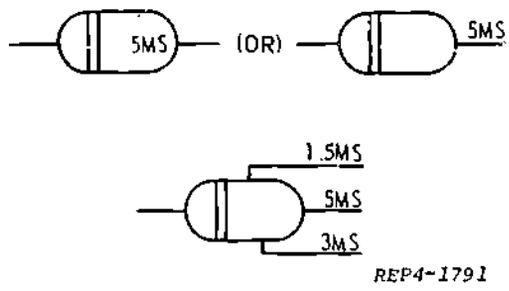


Figure 4-15. Delay Line Symbols

4-74. In the delay line symbols shown in figure 4-15, if the duration of the delay line is tapped, the delay time with respect to the input is included adjacent to the tapped output. Twin vertical lines indicate the input side. (The serial adder of figure 3-5 includes a delay line.)

4-75. Storage Devices

4-76. The memory systems in a digital computer provide storage for data involved in the solution of given problems and feed this information to the data processing or arithmetic unit when needed. This data can be stored and obtained at a later time through use of a storage device. The main storage element inside the computer is usually called MEMORY.

4-77. Access time and storage capacity are the two most important characteristics of any memory system. They are determined by the kind of storage unit used. No one system has the desired capabilities of large capacity and short access time. In fact, most large capacity units have a long access time, and most low capacity storage units have short access time. A combination of storage units is necessary to obtain the required specifications.

4-78. A solution is to use fast access storage devices for the main memory and slower devices as auxiliary or buffer storage facilities. Then large groups of numbers at a time can be sent back and forth, as required, and stored in consecutive storage units. Sometimes the computer can continue its computations during the transfer. Instead of having to locate individual storage units in the auxiliary storage, the computer has access to large blocks of registers.

4-79. Only the main memory is used for all operations inside the computer. When the main memory fills up with intermediate results, instructions send large blocks of results to the auxiliary storage and bring back fresh data or even additional program instructions, as required.

4-80. Three types of storage devices are in common use today: magentic cores, magnetic tapes, and magnetic drums.

4-81. Characteristics of Storage Units

4-82. The capacity of a storage unit may be expressed in terms of the maximum number of bits, characters, or words that may be stored within the medium.

4-83. Storage units of small capacity, such as flip-flop storage registers, are usually rated according to the bit capacity. For example, a storage register with 36 flip-flops is capable of storing 36 single binary digits and is said to have a capacity of 36 bits.

4-84. When describing the storage capacity of larger memory devices, such as magnetic tapes and drums, WORD CAPACITY rather than BIT CAPACITY is usually given. In such cases the number of bits in a word must be stated.

4-85. Storage capabilities of magnetic cores, drums, and tapes are listed in figure 4-16. The storage capacity of each unit is stated in words.

STORAGE DEVICE	CAPACITY	MODE OF ACCESS	ACCESS TIME	PERMA-NENCE	VOLA-TILE	USE
Magnetic Cores	10 to 100,000 words	Random	1 to 100 μsec	Erasable	No	High-Speed Internal
Magnetic Drums	20 to 2,000,000 words	Sequential & Cyclic	10 to 100 μsec	Erasable	No	Medium-Speed Internal
Magnetic Tapes	2 to 20,000,000 Words/Reel	Sequential and Progressive	1 to 100 sec	Erasable	No	Slow-Speed External

Figure 4-16. Characteristics of Magnetic Cores, Drums and Tapes

4-86. Modes of Access

4-87. The bits of information stored in a memory unit are combined to form words with a specific bit length. Each word contains the same number of bits and is assigned a location number within the storage unit which is known as its ADDRESS. The mode of access refers to the method used in the memory system to gain access in these storage locations or addresses. The mode of access may be either random or sequential.

4-88. Random access refers to the ability of the memory system to provide immediate access to any memory location without regard to its physical location within the storage unit. In the random access mode of operation, any memory location may be addressed in the same amount of time as any other location. Magnetic core memories are usually operated in the random access mode.

4-89. Sequential access indicates a one-after-the-other process. Memory locations on magnetic tape are usually addressed in this manner. To address any one location, all the locations up to the desired location must be sensed and checked. When the proper address has been reached, the information is read out. The readout time can vary from a relatively short period of time to an extremely long period of time, depending on the location.

4-90. Sequential access systems are broken into two groups, cyclic and progressive. The cyclic mode is a mode of access in which each location recurs at a given interval. Examples of this type of access include magnetic drums, tape loops, and punched tape.

4-91. The progressive mode does not move constantly in one direction as the cyclic mode. Rather, the progressive mode can be started, stopped, or reversed, to locate the desired memory location. Examples of progressive access are magnetic tape (reels), punched cards, and punched tapes.

4-92. Deleted.

4-93. Access Time

4-94. Access time is defined as the time interval between the instant information is requested and the instant it becomes available. Scientists are constantly trying to decrease this time interval.

4-95. In memory systems using the random access method, the time interval is the same for any location in the memory.

4-96. Sequential access systems, however, have a different access time for each piece of information. In this system access time is given in maximum, minimum, and average times. As an example, in the magnetic drum, the maximum access time is associated with that memory location which has just passed by the read heads and must make a complete revolution before coming under the read heads again.

4-97. Minimum access time occurs when the needed information is the next piece of information to pass under the read heads. The average access time is the mean time between the minimum and maximum time.

4-98. Permanence

4-99. This characteristic specifies whether or not information in storage may be erased. A magnetic memory is erasable, since any word can be changed or deleted without altering the memory system. Examples of nonerasable memories are punched cards and punched tape.

4-100. Volatility

4-101. If information in the memory system is lost when power is removed, the memory system is VOLATILE. A delay line is a volatile memory and, in order to retain the data, information must be periodically rewritten. If a power loss should occur, the information would be lost. Any magnetized memory system is a nonvolatile memory in that it does not lose its information except by being demagnetized. Figure 4-16 shows some of the characteristics of typical memory systems.

4-102. Magnetic Tapes

4-103. Two types of tape are used with digital computers, paper and magnetic. Both types can be used for either input or output functions. Each type has its own distinctive processing equipment and the tapes are not interchangeable.

4-104. Magnetic tape usually is a coated plastic tape about 1/2 inch wide, similar to the tape used in home style tape recorders. The coating has magnetic properties that enable the tape to be magnetized in very small spots.

4-105. Information is thus represented in the form of a pattern of magnetic bits. In one form of tape recording, a magnetized spot or bit may represent a binary one, and a nonmagnetized spot may represent a binary zero. A more common system of writing on tape requires that both 1s and 0s be expressed as magnetized bits; the 1s with north-south magnetic alignment and the 0s with south-north alignment. A large amount of information can be stored on a length of tape. A typical tape has a word density of 41 computer words per inch. A tape 2000 feet long contains 52,388,000 bits of data per tape.

4-106. Magnetic Drums

4-107. The magnetic drum storage system is an endless track memory. Its most important components are a rotating drum and a set of stationary heads. The magnetic drum consists of a nonmagnetic base cylinder, usually manufactured of aluminum because of its paramagnetic characteristics and good heat dissipation. The diameter of the drums varies from 1/4 inch to 4 feet, and their lengths vary from 1/4 inch to 3 feet. A magnetic coating is applied to the base in one of three ways. One method is to dip or spray the aluminum surface with oxide of iron.

4-108. Another method is to closely wrap the drum surface with ferromagnetic wire and then mill the surface flat. This method obtains properties not present in the iron oxides. The third method of magnetic surface preparation is to electroplate the surface with a ferromagnetic alloy. This method has slightly better magnetic properties.

4-109. The drum is usually formed directly on a shaft, and the shaft is turned to produce drum rotation. The shaft can be directly connected to the rotor of a drive motor or it can be belt driven.

4-110. Magnetic Memory Cores

4-111. Another device that is finding wide use as a storage element is the bistable ferromagnetic core. Its square hysteresis loop and rapid switching time along with its reliability, ruggedness, and small size make the ferromagnetic core an ideal device for use in computer circuits. Some of these computer circuits include shift registers, storage registers, and memory units. The added advantage is that ferromagnetic cores can retain binary information almost indefinitely without a constant source of power.

CHAPTER 5

DIGITAL/ANALOG CONVERTERS

5-1. Conversion circuits are necessary whenever machine language differs from the language of its input and output equipment. Humans are accustomed to thinking in terms of the decimal system; however, most equipment makes computations or decisions in digital form. When humans monitor certain internal portions of the machine's information, a conversion circuit must be incorporated to change the machine's language to a form the human can understand. If you work with digital equipment, it is much easier to insert or extract the information in decimal or octal form. This requires the use of conversion circuits in the input and output of the machine.

5-2. A digital computer performs mathematical computations by expressing numbers in terms of digits that can assume certain values. The results obtained are expressed in digital form. For example, a digital computer may use the binary digits zero and one to express numbers. The digits are assigned certain values such as -3 volts and 0 volts. Often it is necessary to convert these numbers into physically measurable quantities such as voltage or length. A physical condition, such as the azimuth position of an antenna, is represented best by a proportional (analog) voltage. It is desirable, therefore, to use analog voltages in certain applications of digital equipment. If the computer expresses antenna azimuth in digital form, then the digital form must be converted to an analog voltage prior to use. This chapter discusses DIGITAL TO ANALOG, ANALOG TO DIGITAL, MECHANICAL TO DIGITAL, and BINARY TO DECIMAL readout conversion systems.

5-3. Digital to Analog Conversion

5-4. One form of digital to analog converter employs relays to select the output of a voltage divider ladder. The count in the counter determines the position of the relay contacts; therefore, the counter CONTROLS or DETERMINES the output voltage from the voltage divider ladder.

5-5. Such a circuit is shown in figure 5-1. Figure 5-1A shows the flip-flop in the ONE state and figure 5-1B shows it in the ZERO state.

5-6. In figure 5-1A, the high (0 volts) output from the 1 side of the flip-flop causes Q1 to conduct. When Q1 conducts, collector current flows through the relay coil. The energized coil pulls the relay armature up. When the armature is up, it makes contact with the upper section (contact 1) of relay K1. R1 is connected in and R2 is removed from the ladder circuit.

5-7. In figure 5-1B the 1 side output of the flip-flop is -3 volts because the flip-flop is in the ZERO state. The -3V output is applied to the base of Q1 and cuts off Q1 collector current. With no current the relay is de-energized. The resistor R2 is now connected in and R1 is removed from the ladder circuit.

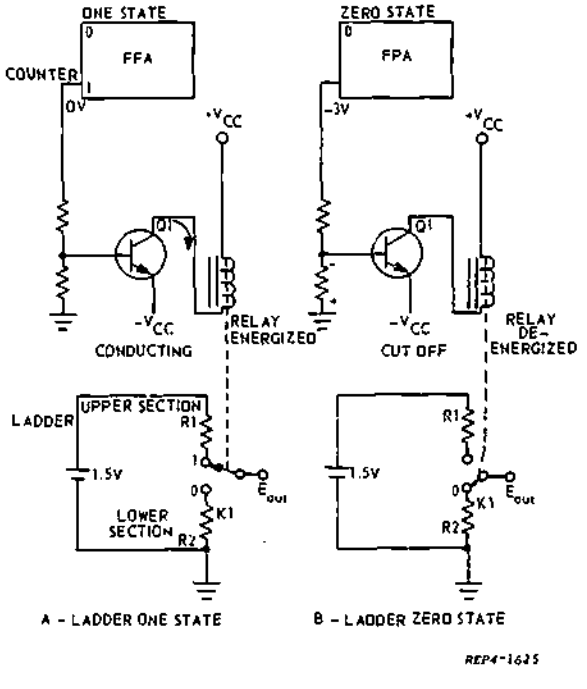


Figure 5-1. Ladder Control Circuit

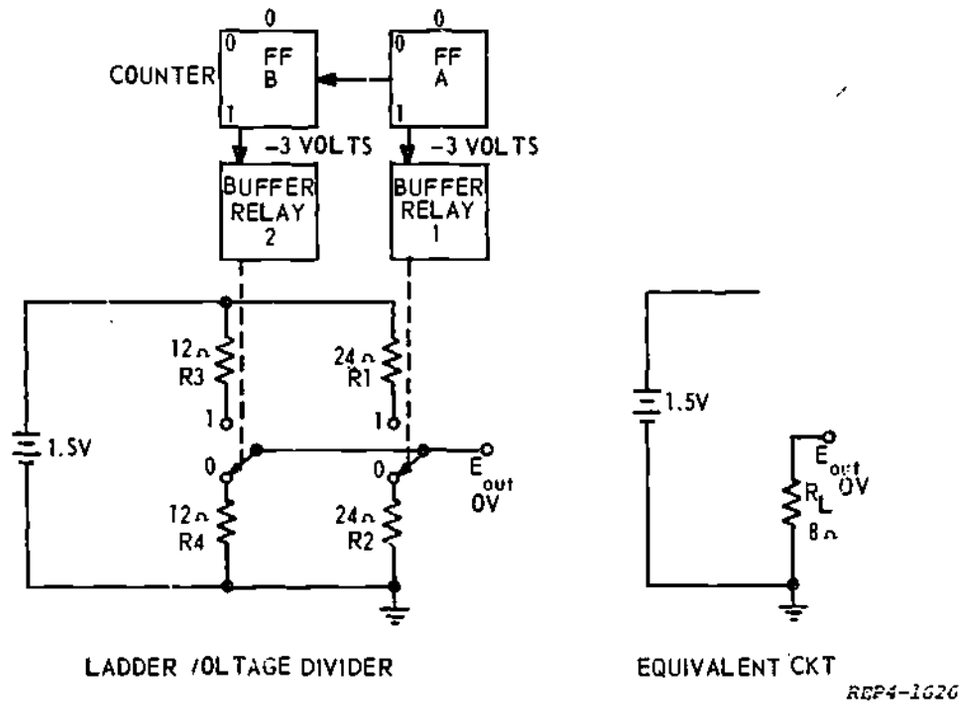


Figure 5-2. Digital-to-Analog Converter (Zero Count)

5-8. Thus, the state of the flip-flop determines whether R1 or R2 is connected in the circuit. When the flip-flop is in the ONE state, R1 is connected. When the flip-flop is in the ZERO state, R2 is connected.

5-9. A two-stage digital-to-analog converter is shown in figure 5-2 with a zero count in the counter. Since there is a zero count in the counter, both flip-flops are in the ZERO state, and both armatures are in the down position. R3 and R1 are removed and R2 and R4 are inserted in the ladder circuit. In the equivalent circuit of the ladder, the circuit is open and the output voltage is zero.

5-10. In figure 5-3, flip-flop A is in the ONE state and flip-flop B is in the ZERO state. Therefore, the armature for relay K1 is in the up position and the armature for relay K2 is in the down position. In the equivalent circuit R_U equals R1 (24 ohms) and R_L equals R4 (12 ohms).

The formula for the output voltage is:

$$E_{out} = E_{applied} \times \frac{R_L}{R_L + R_U}$$

Therefore,

$$E_{out} = 1.5 \text{ V} \times \frac{12 \text{ ohms}}{12 \text{ ohms} + 24 \text{ ohms}}$$

$$E_{out} = 1.5 \text{ V} \times 1/3 = .5 \text{ volts}$$

When the count is one, the output voltage is .5 volts.

5-12. When the count is two, flip-flop A is in the ZERO state and flip-flop B is in the ONE state (figure 5-4). The armature for relay K1 is down and for relay K2 is in the up position. The upper section of the ladder contains R3 and the lower section contains R2. In the equivalent circuit, R_U is equal to 12 ohms and R_L is equal to 24 ohms. Therefore, the output voltage is:

$$E_{out} = 1.5\text{V} \times \frac{24 \text{ ohms}}{12 \text{ ohms} + 24 \text{ ohms}}$$

$$E_{out} = 1.5\text{V} \times 2/3 = 1 \text{ volt}$$

When the count is two, the output voltage is 1 volt.

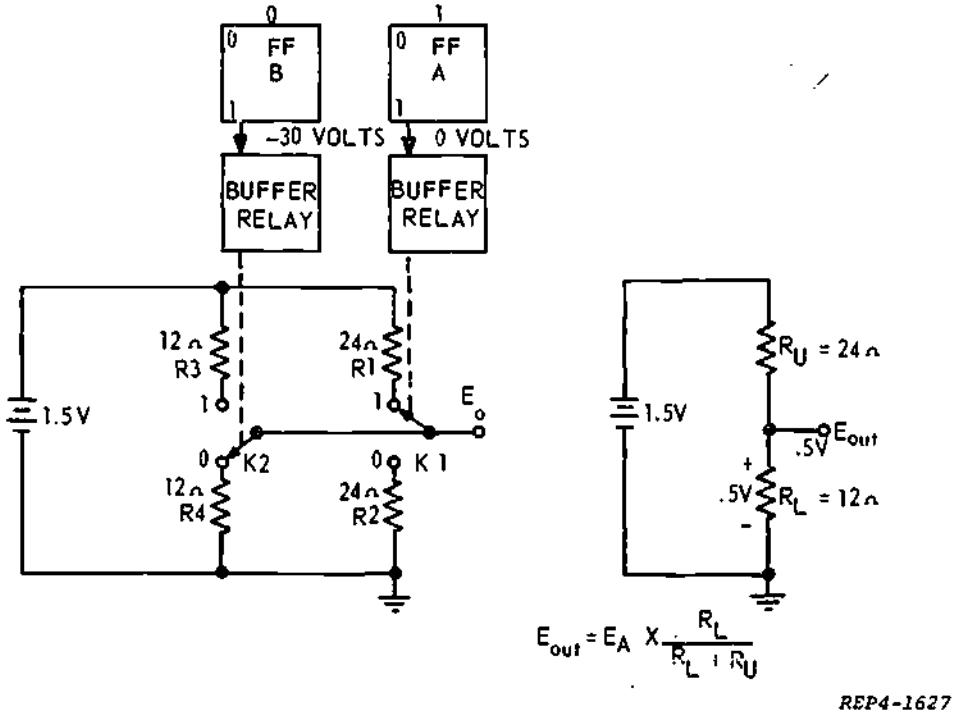


Figure 5-3. Digital-to-Analog Converter (One Count)

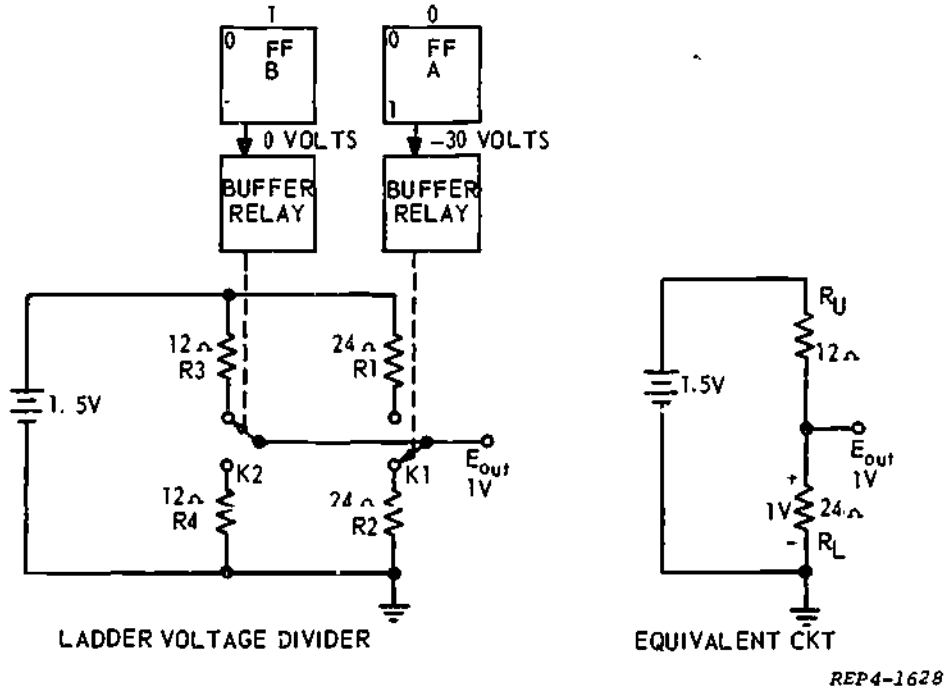


Figure 5-4. Digital-to-Analog Converter (Two Count)

5-13. When the count is three, both flip-flops are in the ONE state and both relay armatures are in the up position (figure 5-5). Resistors R1 and R3 are placed in the upper section, and R2 and R4 are removed from the lower section. In the equivalent circuit R_U equals 8 ohms and R_L is open. Since the output is taken across R_L, the output voltage is equal to the applied voltage (1.5 V). When the count is three, the output is 1.5 volts.

5-14. In summary: A zero count equals 0 volts, a one count equals .5 volts, a two count equals 1 volt, and a three count equals 1.5 volts. As the count increases by one the output voltage increases by .5 volts. The .5-volt increase is called the "voltage step." The amplitude of the step depends upon the applied voltage and the maximum count of the counter.

5-15. A five stage digital to analog converter circuit is shown in figure 5-6. The converter is connected to a five-stage counter that can hold a maximum count of 31. The ladder is made up of two sections containing identical pairs of resistors in each leg. Notice that the value of the resistors is cut in half as the place value of the binary digit doubles. Thus, considering the value of a resistor in the leg of flip-flop A as being R, the resistor in the leg of flip-flop B is one-half R (R/2), the resistor in the leg of flip-flop C is .5 x .5R or .25 R (R/4). The resistor in leg D is one-eighth R (R/8), and the resistor in leg E is one-sixteenth R (R/16), Recall the binary numbering system and observe that, beginning at A as the LSD and continuing through B, C, D, and E (the MSD), we have powers of two: $2^0 = 1$, $2^1 = 2$, $2^2 = 4$, etc. The denominator of R, then, corresponds to the power of two.

5-16. An easy method for determining the output voltage of a digital-to-analog converter is as follows:

$$\frac{\text{Count in Counter}}{\text{Maximum Possible Count}} \times \text{Supply Voltage}$$

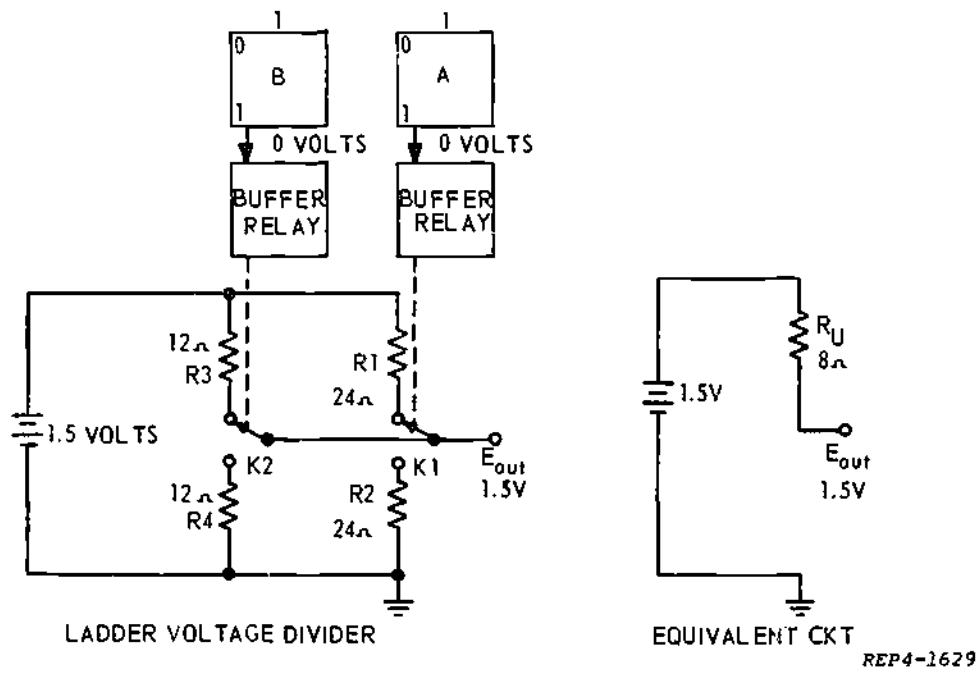


Figure 5-5. Digital-to-Analog Converter (Three Count)

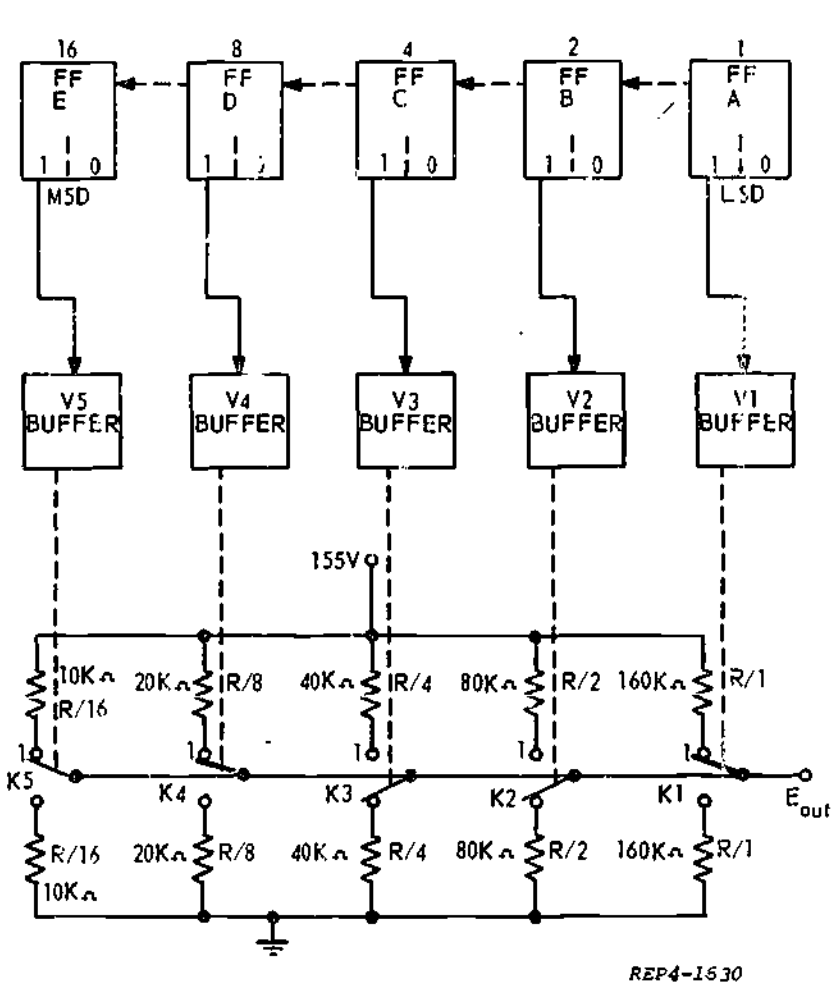


Figure 5-6. Digital-to-Analog Circuit

Example 1:

A five stage counter contains a count of 11001 or 25, as shown in figure 5-6. Find the output voltage if 155 volts is applied to the ladder.

$$E_{out} = \frac{25}{31} \times 155 \text{ volts}$$

$$E_{out} = 125 \text{ volts}$$

Example 2:

In figure 5-7 find the count in the counter and the output voltage.

5-17. The count in the counter is determined by adding the denominators of the resistors being used in the upper section of the ladder. For figure 5-7, this sum equals 16 + 4 + 2 + 1 or 23. Maximum possible count may be determined by adding the denominators of all the resistors in the lower section. This sum equals 16 + 8 + 4 + 2 + 1 or 31.

Using the above formula, the output voltage is

$$\frac{23}{31} \times 155 \text{ or } 115 \text{ volts}$$

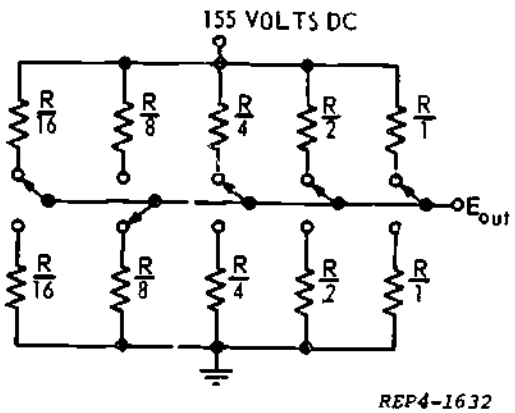


Figure 5-7. Ladder Configuration

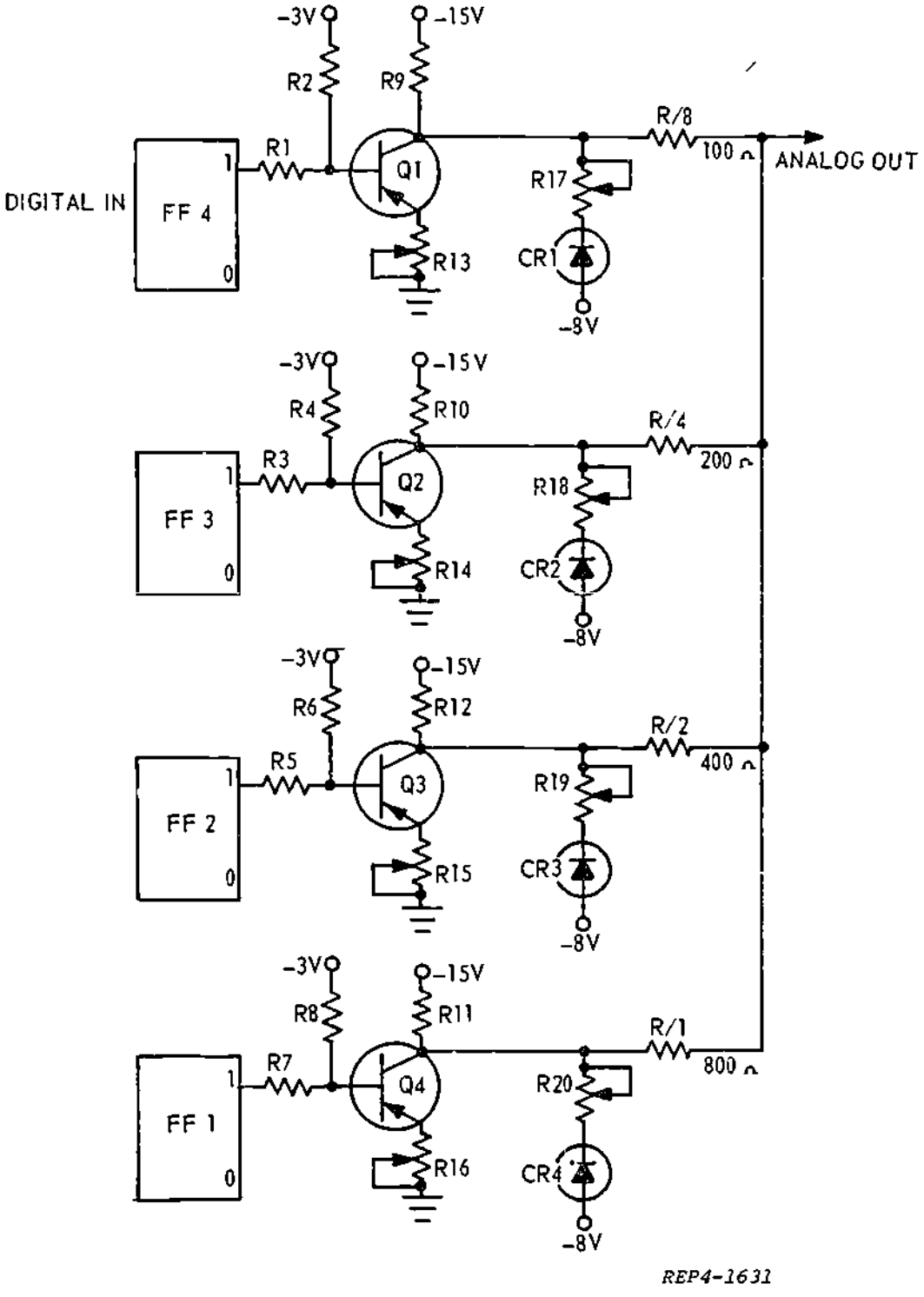


Figure 5-8. Resistive Ladder with Electronic Switching

5-18. The digital-to-analog converter, therefore, is a voltage divider ladder whose output is proportional to the binary count being converted. The resistance in each leg of the ladder is cut in half as the place value of the binary digit in the flip-flop doubles.

5-19. The need for high speed Digital-to-Analog (D/A) Converters has made the electromechanical D/A converter obsolete. The time required for relays to energize or deenergize severely limits the capabilities of digital equipment.

5-20. The electronic D/A converter shown in figure 5-8 has no mechanical parts to slow down response time. Each flip-flop represents a power of two (FF1 is the LSD or $2^0 = 1$, etc.), and the converter shown can hold a maximum count of 15. The circuitry at the output of each flip-flop is nearly identical; therefore, only the purpose of the components associated with FF1 will be discussed.

5-21. FF-1: Stores the binary count to be converted.

5-22. R7-R8: Voltage divider network to develop bias voltage, so Q4 is cut off when FF1 is in the ONE state or saturated when FF1 is in the ZERO state.

5-23. R16: Control used to calibrate the analog output with FF A in the ZERO state.

5-24. R20 and CR4: Limits the collector voltage of Q4 when FF1 is in the ONE state. R20 calibrates the analog output voltage when FFA is in the ONE state.

5-25. R/1: Part of resistive ladder network similar to the one used in electromechanical D/A converters.

5-26. Four flip-flops can have a maximum count of 15. For this count, all must have a high out, and with the high out all transistors will be cut off. Diodes CR1, CR2, CR3, and CR4 clamp the collectors of the transistors to -8 volts. With all collectors clamped to -8 volts, the equivalent circuit shown in figure 5-9 exists. For a maximum binary count of 15, -8 volts is developed as the analog output.

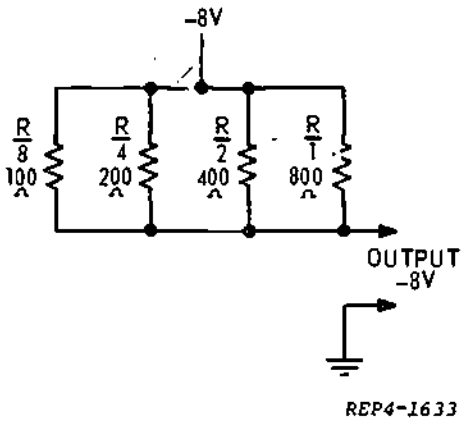


Figure 5-9. Equivalent Circuit (Fifteen Count)

5-27. Notice the values of the resistive ladder resistors associated with each flip-flop. Flip-flop 4 has a resistor (R/8) having 1/8 of the value of the resistor associated with flip-flop 1; therefore, 8 times the value of current will flow when flip-flop 4 is in the ONE state as compared to when flip-flop 1 is high. Under this condition FF4 develops 8 times the voltage of FF1. This relationship makes the output voltage directly proportional to the binary count.

5-28. When a binary count of 0 exists, all flip-flops will have a low voltage at the 1-side outputs which will be sufficient to saturate transistors Q1 through Q4. This places all collectors at nearly 0 volts. The equivalent circuit (figure 5-10) shows that a binary count of zero will produce an analog output of 0 volts.

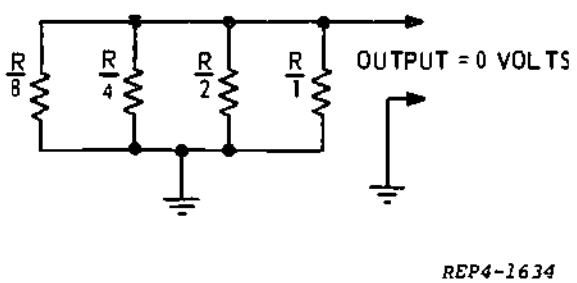


Figure 5-10. Equivalent Circuit (Zero Count)

5-29. With a binary count of 0001, the collectors of Q1, Q2, and Q3 (figure 5-8) will be at 0 volts. The collector of Q4 will be at a -8V since Q4 is cut off. In this condition there will be -0.533 volt at the output due to the parallel combination of R/8, R/4, and R/2 in series with R/1. Figure 5-11 illustrates the equivalent circuit and the resultant output voltage.

5-30. A simple way of determining the analog voltage for any binary count is to:

1. Divide the count in the counter by the maximum possible binary count. The quotient will be a ratio.

2. Multiply this ratio by the maximum voltage output.

5-31. Apply steps 1 and 2 to the circuit in figure 5-11. Maximum voltage is -8V and maximum count is 15.

5-32. With this knowledge the output for any binary count can be quickly determined.

EXAMPLE: Given a binary count of seven, calculate the analog voltage output for the circuit in figure 5-8.

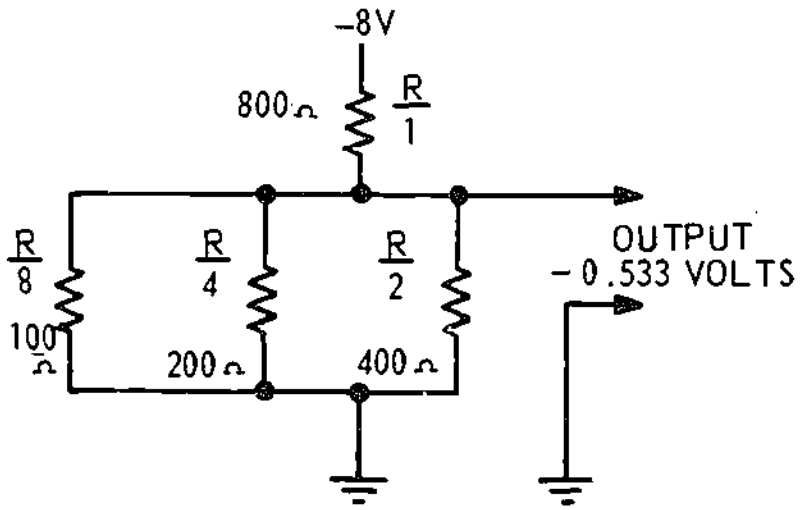
$$\frac{7}{15} \times -8V = \text{OUTPUT}$$

$$= -3.731 \text{ volts}$$

5-33. Analog to Digital Conversion

5-34. Many electronic devices provide information in analog form. The process of converting an analog measurement of a physical variable into a numerical value, thereby expressing the quantity in digital form, is known as DIGITIZING. When analog data is to be handled, stored, or manipulated in a computer, it is usually necessary to convert to equivalent binary data.

5-35. Figure 5-12 shows an analog to digital (A/D) converter in common use. This converter takes an analog input and processes it to develop a digital output. Because the time required to obtain a digital readout is directly proportional to the amplitude of the analog voltage to be converted, the variable time A/D converter circuit has an advantage over fixed time conversion circuits. This circuit allows more samplings per second.



REP4-1635

Figure 5-11. Equivalent Circuit (One Count)

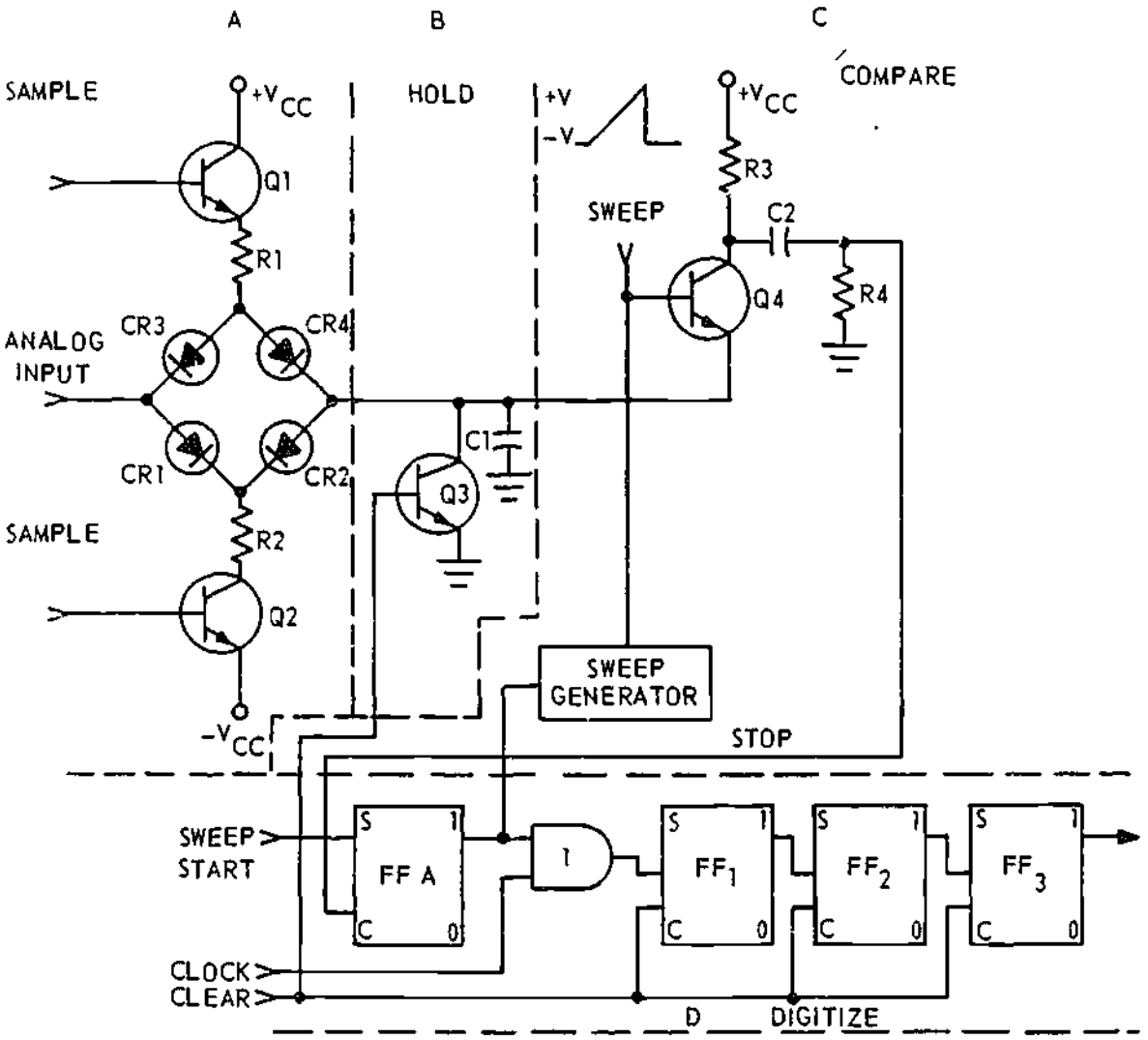


Figure 5-12. Variable Time A/D Converter

5-36. The circuit can be broken down into four basic blocks according to function. The components enclosed by the dotted lines in area A perform the SAMPLE function, those in B the HOLD function, those in C the COMPARE function, and D the DIGITIZE function. The main point to understand in circuit operation is the relationship between

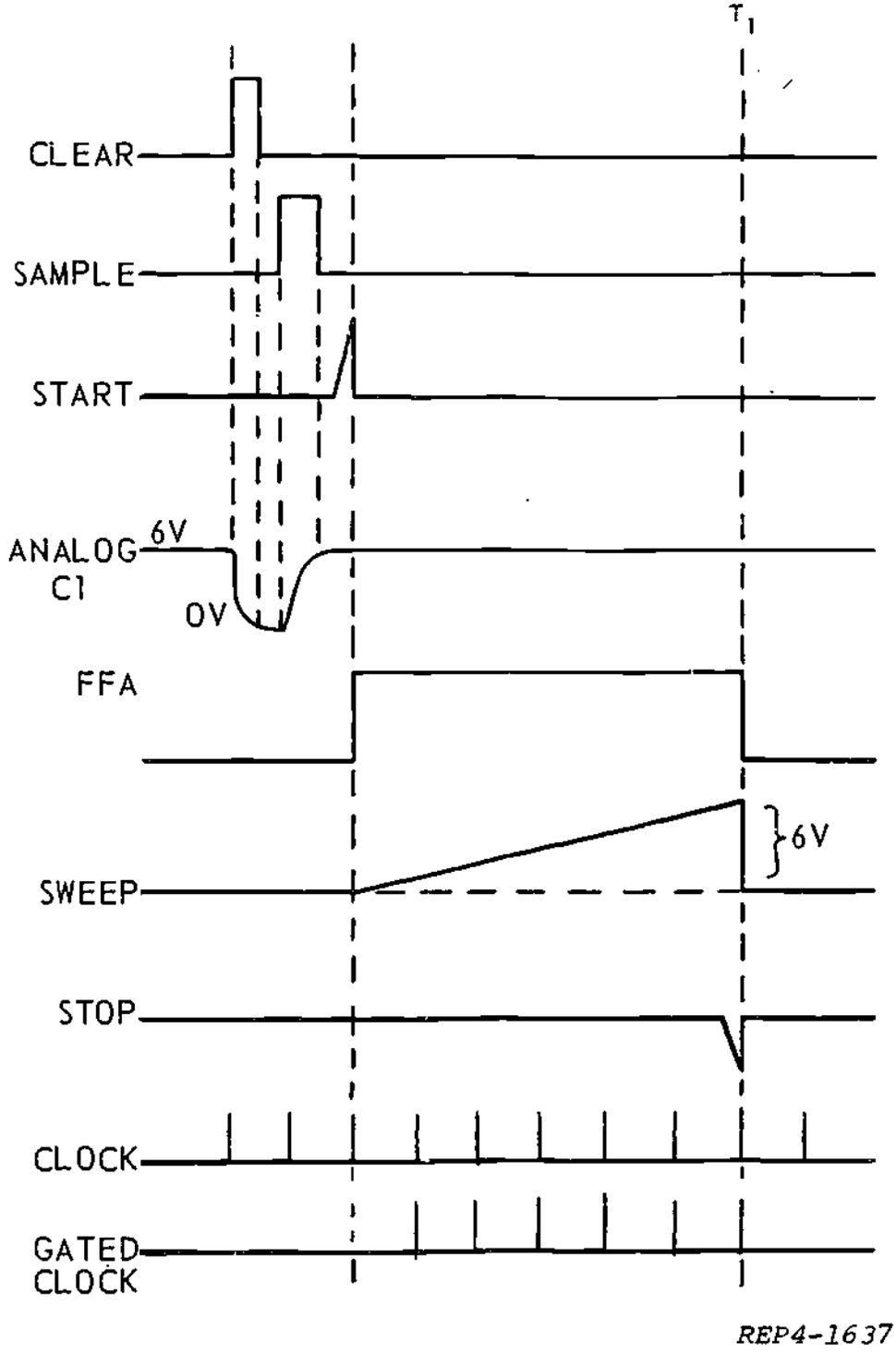


Figure 5-13. A/D Converter Waveforms

the analog voltage, sweep voltage, and clock pulses shown in figure 5-13. For example, assume the analog voltage to be converted is 6 volts. If a serial upcounter is allowed to accumulate a count from the time the sweep starts until the sweep voltage equals the amplitude of the analog voltage, the count will be proportional to the analog voltage.

5-37. Figure 5-13 shows the time relationships of the various signals. Observe the CLEAR and SAMPLE inputs. The CLEAR pulse is applied to the base of Q3, to discharge C1, and to the CLEAR inputs of flip-flops FF1, FF2, and FF3, placing them in the ZERO state. The SAMPLE pulse is then applied to the base of Q1 and Q2, allowing current to flow from $-V_{CC}$ up through Q2, R2, CR1, CR2, CR3, CR4, R1, and Q1 to $+V_{CC}$. Because CR1, CR2, CR3, and CR4 are conducting, the 6 volts present at the ANALOG INPUT will charge capacitor C1 to 6 volts. At the end of the sample pulse, Q1, Q2, and the four diodes cut off. With this condition, there is no discharge path for C1, and C1 holds the 6-volt charge. The down clock of the SWEEP START pulse is applied to the SET input of FFA, setting it to the ONE state, which places a high on the input to AND gate 1. Positive CLOCK pulses are gated through, causing the serial up counter in the digitizer to begin counting. The output of FFA is also applied to the sweep generator and starts a positive going sweep. The 6-volt charge on C1 is applied to the emitter of Q4. When the positive going sweep applied to the base of Q4 passes through 6 volts, Q4 becomes forward biased. The collector voltage of Q4 drops. This down clock is coupled by C2 and R4 to the CLEAR input of FFA. This causes FFA to change to the ZERO state, stopping the sweep generator and disabling AND gate 1, allowing no more clock pulses through. Notice that the counter stops counting at the exact instant the sawtooth voltage equals the analog voltage across C1. This causes the count in the counter to be directly related to the amplitude of the analog voltage. In this example, a 6-volt analog input resulted in a count of six in the counter.

☆ U. S. GOVERNMENT PRINTING OFFICE: 1976-671-585/178

ATC 178

ATC ST 3AQR3X020-X
Prepared By Keesler TTC
KEP-ST/Digest VII

Technical Training

Electronic Principles (Modular Self Paced)

Modules 51 - 55

DIGESTS

1 April 1975

AIR TRAINING COMMAND

7-11

Basic and Applied Electronics Department
Keesler Air Force Base, Mississippi

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1 April 1975

These Digests provide a summary for each module, 51 - 55, in the Electronic Principles Course. The Digest is designed as a refresher for students with electronics experience and/or education who do not need to study any of the other resources in detail.

After reading a Digest, if you feel that you can accomplish the objectives of the module, take the Module Self Check in the back of the Guidance Package – if you decide not to take the self-check, select another resource and begin study.

CONTENTS

MODULE 51

NUMBERING SYSTEMS AND MATHEMATICAL COMPUTATIONS

Digital circuits can perform arithmetic operations using data that has been transcribed to the binary or octal numbering system. The rule for converting decimal information to its binary or octal equivalent is to divide the decimal number by base 2 for binary or base 8 for octal. Continue the division till a quotient of 0 is reached. The remainders will form the binary or octal equivalent, with the LSD being the first remainder and the MSD the last.

Each digit of a binary or octal number has value relative to its position with respect to the binary or octal point. From this a place value chart is developed, see Table 51-1. The place value chart is used to convert binary to decimal and octal to decimal. Each digit in the binary or octal number is multiplied by its place value, and then the decimal equivalents are added.

To convert a binary number to its octal equivalent, divide the binary number into groups of three, starting at the binary point. Each group then relates to a single digit in the octal number. Octal to binary conversion reverses the procedure.

Binary and octal addition requires a carry to the next higher order column whenever the sum exceeds the value of the largest digit, 1 in binary and 7 in octal. Otherwise, binary and octal addition is performed in the same manner as in the decimal system.

Table 51-1

BINARY AND OCTAL PLACE VALUE CHARTS

Powers of 2	2^4	2^3	2^2	2^1	2^0
Decimal Equivalent	16	8	4	2	1

Powers of 8	8^4	8^3	8^2	8^1	8^0
Decimal Equivalent	4096	512	64	8	1

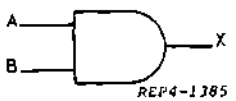
The direct method of subtraction is used for finding the difference of two binary or octal numbers. Should it be necessary to borrow from the next higher order filled column, it is equal to two ones in binary and eight in octal, to the next lower order column. The complement method can also be used for binary subtraction. The procedure is to complement the subtrahend, add it to the minuend, end around carry, and add to find the difference.

MODULE 52

LOGIC FUNCTION AND BOOLEAN EQUATIONS

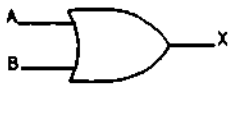
In electronic digital circuits, specific voltage levels are given to the binary digits 1 and 0. These then correspond to a HIGH logic level and a LOW logic level respectively. Data is processed by moving these logic levels through gates. A gate is a circuit with two or more inputs and only one output.

Diode AND gates are designed so that their output is HIGH when all of its inputs are HIGH simultaneously. For all other times the output is LOW. A chart that shows the output of the gate for all possible combinations of input conditions is known as a TRUTH TABLE. The truth table shows there will be a HIGH at the output of the AND gate when all the inputs are HIGH, and a LOW output when any input is LOW. See figure 52-1.



A	B	X
L	L	L
L	H	L
H	L	L
H	H	H

Figure 52-1 AND Gate Logic Symbol and Truth Table



A	B	X
L	L	L
L	H	H
H	L	H
H	H	H

Figure 52-2. OR Gate Logic Symbol and Truth Table

A	B	X
L	L	L
L	H	H
H	L	H
H	H	L

Figure 52-3. Exclusive OR Logic Symbol and Truth Table

Another basic logic circuit is the OR gate. The OR gate will have a HIGH at its output whenever any of its inputs are HIGH, and a LOW when all of the inputs are LOW. The logic symbol and truth table for a two input OR gate is shown in figure 52-2.

A STATE INDICATOR is a small circle at the input or output of a gate. The state indicator at the input signifies that the logic LOW will activate a gate function. The output of a gate is low when activated if a state indicator is shown at the output.

The EXCLUSIVE OR is a logic function that has no output when there are two like inputs. The output will be HIGH when the logic levels at the inputs are different from each other, and LOW when they are the same. See figure 52-3.

Direct coupled transistor logic, referred to as DCTL, are gating circuits using transistors in series or parallel arrangements. The gate output is directly coupled to another transistor where the base emitter junction is used as a logic level voltage clamp. Current mode logic, or CML, is another type of transistor logic. The advantage of CML is that the transistors are not saturated when they are conducting, thus speeding up switching time.

A combination of logic symbls is a logic diagram. Logic diagrams may be used in trouble analysis of digital circuits. Logic operations are expressed as a Boolean equation using letters and mathematical symbols. Letters are used to represent gate inputs and outputs. The three basic logic functions and their symbols are: AND represented by a dot $\cdot$; OR by a plus $+$; and NOT by a bar or vinculum $\bar{}$; Each Boolean equation is an expression of specific logic operation which can then be shown as a logic diagram. The $\cdot$ is diagrammed by the AND gate, the $+$ by the OR gate, and the $\bar{}$ by the small circle state indicator. The $\bar{}$ over one letter is shown as a state indicator at the input to a gate, and if over a group of letters by a state indicator at the output from a gate.

Module 53

LOGIC CIRCUITS AND DIAGRAMS

Multivibrators are readily adaptable for use in logic circuits. The monostable multivibrator, also known as the single shot, is used for pulse stretching or shaping, and for adjustable gate delay.

The Schmitt trigger is a multivibrator similar to the monostable MV, except that the output pulse width is determined by the time duration of the input signal. It is used to restore the shape of a square wave that has become degenerated. Figure 53-1 is a schematic of a typical Schmitt trigger.

Flip-flops are bistable multivibrators that have been modified for use in digital circuits. They are used in counters and registers. Two basic types of flip-flops are the complementing and complemented. A complementing FF uses triggers or clock pulses to switch states. A complemented FF has diode AND gates, differentiating networks, and clipping diodes in its SET and CLEAR (RESET) inputs. The logic symbols are shown in figure 53-2.

The J-K is a modified flip-flop whose state, after a clock pulse, is determined

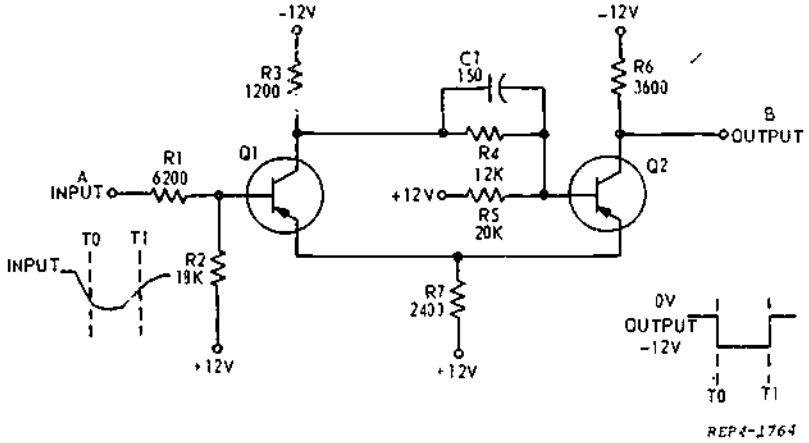


Figure 53-1. Schmitt Trigger

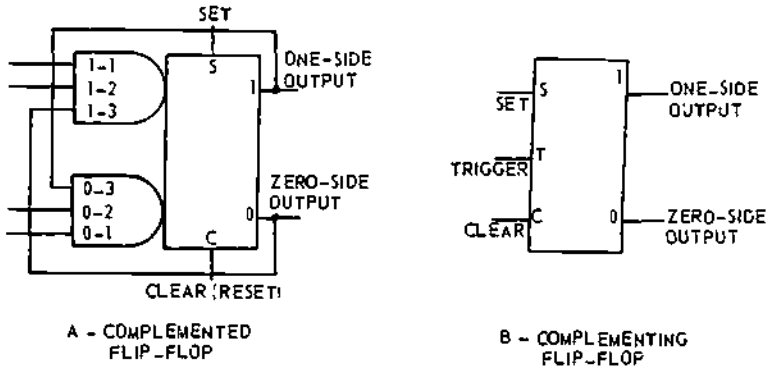


Figure 53-2

by the logic levels existing on the J and K inputs. With a high on J or K, the FF will be set or reset; if J and K are both high the FF toggles; and if both are low, the FF does not change.

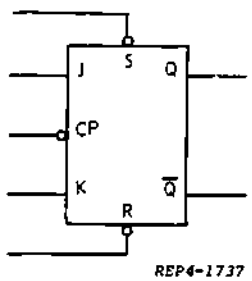


Figure 53-3. Logic Symbol J-K FF

A series half adder is a logic circuit that can add two binary digits. It has two inputs and two outputs, the sum and carry. It can only be used for addition of the LSD column. For all higher order columns, adding circuits must be capable of handling a possible carry from a lower order column. The series full adder can perform this function one column at a time.

The parallel full adder consists of several full adders arranged in parallel. Addition of complete binary quantities can then be accomplished during one timing pulse, thus offering faster processing.

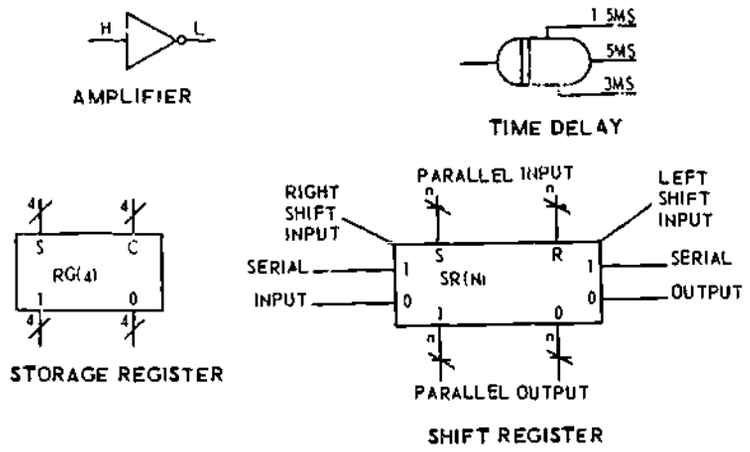


Figure 54-1. Logic Symbols

Module 54

COUNTERS, REGISTERS, AND STORAGE DEVICES

Counters are made up of cascaded flip-flops whose function is to monitor the number of clock pulses. Either complementing or complemented flip-flops are suitable. They are used for program timing or frequency division.

Two basic types of counters are the up-counter and the down-counter. The up-counter is initially cleared to all zeroes, then its count increases by one with each clock pulse. The down-counter is first set to all ones, and its count decreases by one with each clock pulse. AND gates can be connected to either the 1 or 0 outputs of counter stages to detect a particular count.

A decade counter is a four-stage up counter that has only 10 possible states instead of 16. This is done by feedback circuits which preset the counter to skip six counts. At every tenth clock pulse, the decade counter resets to all zeroes.

Another type of counter is the ring counter. Here the output of the last stage is fed back as an input to the first stage. One stage will be in the one state and all the others in the zero state. Clock pulses then move the one through each succeeding stage.

A storage register is a group of flip-flops used to store data for an indefinite period of time. Information from a serial up counter is transferred to the storage register by a read-in pulse. The storage register has the capability of parallel read-in and parallel read-out.

The shift register can receive information in series or parallel from a storage register with a transfer or shift pulse. It can then be extracted serially one digit at a time or transferred out in parallel all at one time for later use in data processing.

Figure 54-1 illustrates the logic symbols of an amplifier, time delay, storage register, and shift register.

Three types of magnetic storage devices are core, drum, and tape. The two most important characteristics to be considered in any storage device are storage capacity and access time.

Module 55

DIGITAL/ANALOG CONVERTERS

Digital circuits process data binarily. Therefore, a need exists for converting information such as a voltage or a compass heading, into binary form, and vice versa.

Figure 55-1 is the schematic of a digital to analog conversion circuit. The binary count in the counter is transferred to the resistive ladder from which an equivalent voltage is taken.

Figure 55-2 is the schematic of an analog to digital conversion circuit. A sample analog voltage is compared to a rising sweep voltage while an up counter in the digitizer is accumulating a count. When processing is finished the binary count will be proportional to the analog voltage.

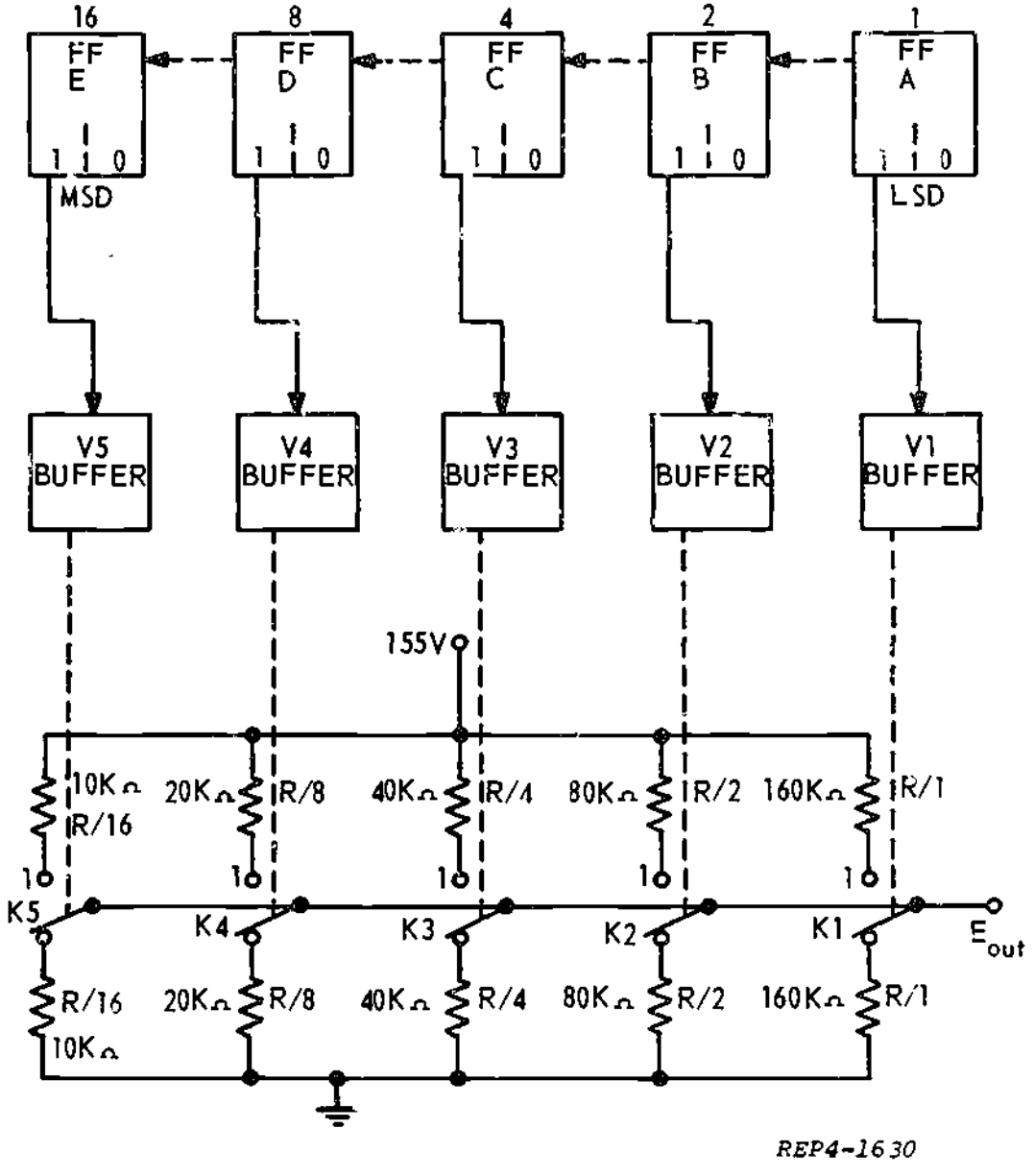


Figure 55-1. Digital/Analog Converter

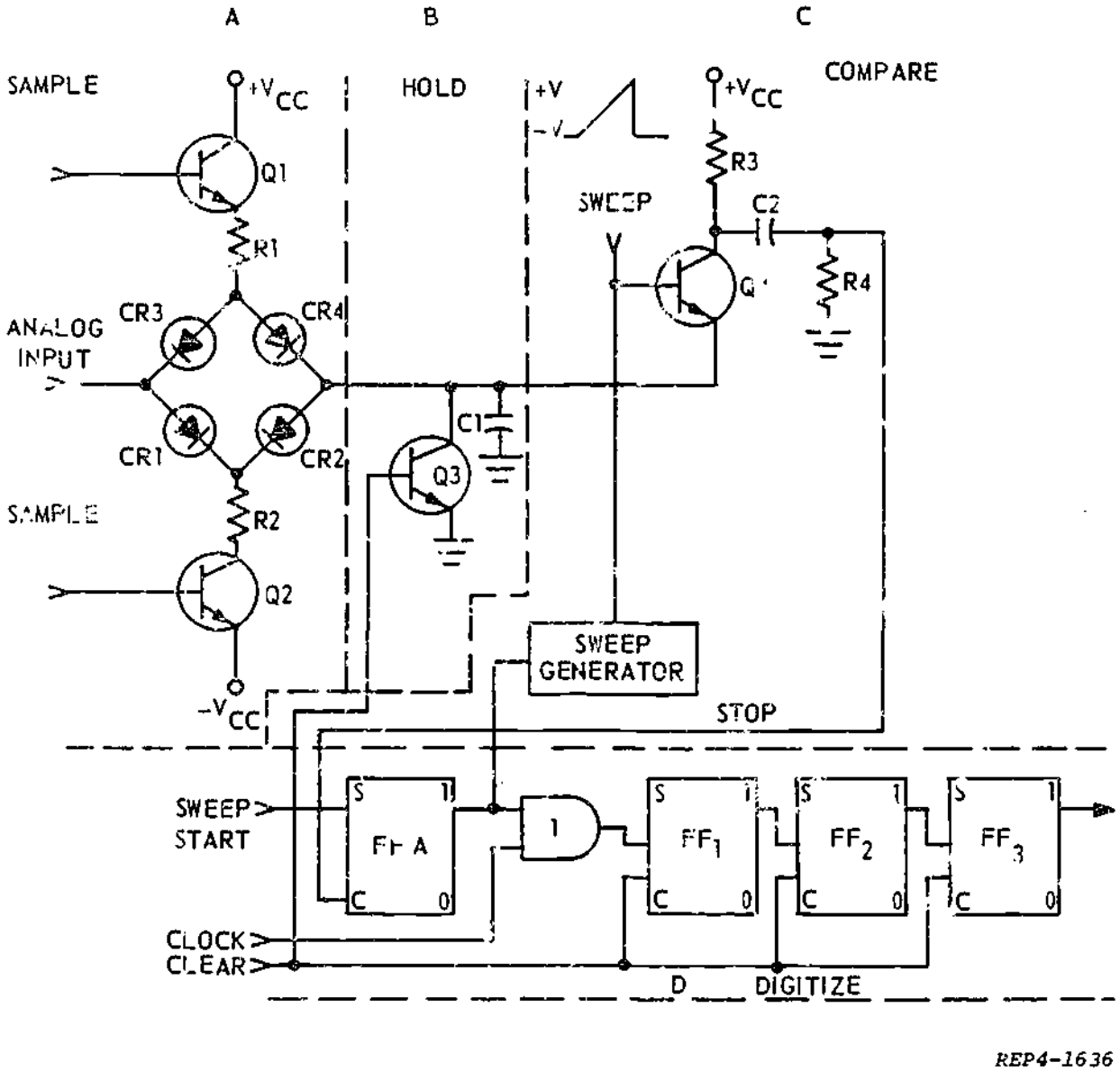


Figure 55-2. Analog/Digital Converter

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PREPARE THE MAN

Technical Training

ELECTRONIC PRINCIPLES (MODULAR SELF-PACED)

MODULE 51

NUMBERING SYSTEMS AND MATHEMATICAL COMPUTATIONS

October 1975

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ELECTRONIC PRINCIPLES

MODULE 51

NUMBERING SYSTEMS AND MATHEMATICAL COMPUTATIONS

This Guidance Package is designed to guide you through this module of the Electronics Principles Course. This Guidance Package contains specific information, including references to other resources you may study, enabling you to satisfy the learning objectives.

CONTENTS

OVERVIEW

1. SCOPE: Digital computers perform arithmetic operations using several numbering systems. The numbering systems most commonly used are the decimal, octal and binary. This chapter discusses the conversion of the above systems (one to the other) and the addition and subtraction of octal and binary numbers.

2. OBJECTIVES: Upon completion of this module you should be able to satisfy the following objectives:

a. Given a decimal number (not to exceed four digits), convert to its equivalent octal and binary value.

b. Given an octal number (not to exceed four digits), convert to its equivalent decimal and binary value.

c. Given a binary number (not to exceed four digits), convert to its equivalent octal and decimal value.

d. Given an octal addition problem (not to exceed two rows of four digit numbers), solve for the sum.

e. Given an octal subtraction problem (not to exceed four digits per line), solve for the difference.

f. Given a binary addition problem (not to exceed three rows of five digits), solve for the sum.

g. Given a binary subtraction problem (not to exceed two rows of five digits), solve for the difference using the direct method or by complementing and adding.

LIST OF RESOURCES

To satisfy the objectives of this module, you may choose, according to your training, experience, and preferences, any or all of the following:

READING MATERIALS:

Digest
Adjunct Guide with Student Text, Volume VII

Supersedes Guidance Package, KEP-GP-51, 1 September 1974.

AT THIS POINT, IF YOU FEEL THAT THROUGH PREVIOUS EXPERIENCE OR TRAINING YOU ARE FAMILIAR WITH THIS SUBJECT, YOU MAY TAKE THE MODULE SELF-CHECK.

CONSULT YOUR INSTRUCTOR IF YOU NEED HELP.

ADJUNCT GUIDE

INSTRUCTIONS:

Study the referenced materials as directed.

Return to this guide and answer the questions.

Confirm your answers at the back of this Guidance Package.

Contact your instructor if you experience any difficulty.

Begin the program.

A. Turn to Student Text, Volume VII and read paragraphs 1-1 through 1-35. Return to this page and answer the following questions.

1. All the twos in the number 222 have the same numerical value. (TRUE) (FALSE)

2. If we move a number one column to the left in the decimal numbering system we

_____ a. double the value of the number.

_____ b. multiply the number by itself.

_____ c. multiply the number by ten.

3. Any number raised to the zero power is equal to

_____ a. zero.

_____ b. itself.

_____ c. one.

10^3	10^2	10^1	10^0	Power of Radix
1000	100	10	1	Place Value
			2	=
		3		=
	5			=
2				=

Figure 1

4. Use figure 1 and expand the decimal number 2532. Show your work. (Example paragraph 1-34.)

CONFIRM YOUR ANSWERS

B. Turn to Student Text, Volume VII and read paragraphs 1-36 through 1-38. Return to this page and answer the following questions.

1. Identify the portion of the number 706.4 to which each of the following terms are related. (Write the letter of the correct term on the lines drawn to the number below).

a. Integral portion

b. Least significant digit (LSD)

c. Most significant digit (MSD)

d. Place holder

e. Decimal point

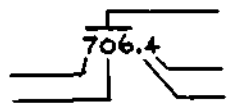


Figure 2

2. Identify the portion of the number $509_{(10)}$ to which each of the following terms are related. (Write the letter of the correct term on the lines drawn to the number below).

a. Least significant digit (LSD)

b. Most significant digit (MSD)

c. Place holder

d. Radix or base

Figure 3

3. Identify the portion of the number 12^5 to which each of the following terms are related. (Write the letter of the correct term on the lines drawn to the number below).

a. Exponent or power

b. MSD

c. LSD

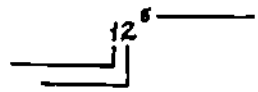


Figure 4

4. Identify the portion of the number $703_{(8)}$ to which each of the following terms are related. (Write the letter of the correct term on the lines drawn to the number below).

a. Integral portion

b. Least significant digit

c. Most significant digit

d. Place holder

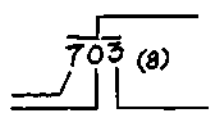


Figure 5

5. Identify the portion of the number $405_{(8)}$ to which each of the following terms are related. (Write the letter of the correct term on the lines drawn to the number below.)

a. MSD

b. LSD

c. Radix or base

d. Octal point

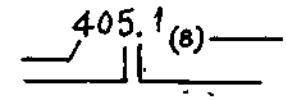


Figure 6

6. Identify the portion of the number $101.01_{(2)}$ to which each of the following terms are related.

a. Integral portion

b. Fractional portion

c. Place holder

d. Binary point

e. LSD

f. MSD

g. Radix or base

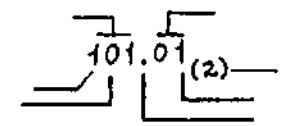


Figure 7

CONFIRM YOUR ANSWERS

C. Turn to Student Text, Volume VII and read paragraphs 1-39 through 1-40. Return to this page and answer the following questions.

1. In the binary numbering system, the right-most column (left of the binary point) can represent a maximum count of

____ a. 1^0

____ b. 2

____ c. 1

____ d. 0

2. Write the binary count next to the following decimal numbers.

1 -	11 -
2 -	12 -
3 -	13 -
4 -	14 -
5 -	15 -
6 -	16 -
7 -	17 -
8 -	18 -
9 -	19 -
10 -	20 -

3. Expand the binary number $1101_{(2)}$. Show your work. (Example paragraph 1-34).

1. Convert $37_{(10)}$ to its equivalent binary value. (Show your work).

2. Convert $402_{(10)}$ to its equivalent binary value. (Show your work).

3. Convert $1301_{(10)}$ to its equivalent binary value. (Show your work).

CONFIRM YOUR ANSWERS

D. Turn to Student Text, Volume VII and read paragraphs 1-41 through 1-45. Return to this page and answer the following questions.

CONFIRM YOUR ANSWERS

E. Turn to Student Text, Volume VII and read paragraphs 1-46 through 1-55. Return to this page and answer the following questions.

1. Convert $11111_{(2)}$ to its decimal equivalent. (Show your work)

2. Convert $10101_{(2)}$ to its decimal equivalent (Show your work)

3. In the octal system when we have used all available digits in the units column, we

_____ a. move the highest octal digit to the next higher column.

_____ b. move that digit to the next higher column and reset the units column to zero.

_____ c. reset the unit column to zero and carry one to the next column.

4. In the octal system the right-most column changes by units, and the next most significant column changes by

_____ a. eights.

_____ b. sixty fours.

_____ c. five hundred and twelves.

5. In the octal system, if we have a two in the third column to the left of the octal point it represents

_____ a. 2×3

_____ b. 2×8^2

_____ c. 2×64

_____ d. $128_{(10)}$

6. Expand the number $2371_{(8)}$. Show your work. (Example paragraph 1-34).

CONFIRM YOUR ANSWERS

F. Turn to Student Text, Volume VII and read paragraphs 1-56 through 1-60. Return to this page and answer the following questions.

1. Convert $38_{(10)}$ to its equivalent octal value. (Show your work).

2. Convert $122_{(10)}$ to its equivalent octal value. (Show your work.)

3. Convert $2143_{(10)}$ to its equivalent octal value. (Show your work).

CONFIRM YOUR ANSWERS

G. Turn to Student Text, Volume VII and read paragraphs 1-61 through 1-69. Return to this page and answer the following questions.

1. Convert $347_{(8)}$ to its equivalent binary and decimal value.

2. Convert $573_{(8)}$ to its equivalent binary and decimal value.

3. Convert $2135_{(8)}$ to its equivalent binary and decimal value.

4. Convert $1011_{(2)}$ to its octal equivalent.

5. Convert $1101_{(2)}$ to its octal equivalents.

CONFIRM YOUR ANSWERS

H. Turn to Student Text, Volume VII and read paragraphs 1-70 through 1-75. Return to this page and answer the following questions.

SOLVE THE FOLLOWING PROBLEMS FOR THE SUM.

1. $111_{(2)}$
   $+101_{(2)}$

2. 1011
   +1001
   $+1111_{(2)}$

3. 10011
   +11101
   $+10101_{(2)}$

CONFIRM YOUR ANSWERS

I. Turn to Student Text, Volume VII and read paragraphs 1-76 through 1-81. Return to this page and answer the following questions.

SOLVE THE PROBLEMS FOR THE DIFFERENCE. (Show all work.)

1. 1101
   $- 111_{(2)}$

2. 10001
   $- 1101_{(2)}$

3. 11100
$-10111_{(2)}$

CONFIRM YOUR ANSWERS

J. Turn to Student Text, Volume VII and read paragraphs 1-82 through 1-84. Return to this page and answer the following questions.

SOLVE THE FOLLOWING PROBLEMS FOR THE SUM.

1. $54_{(8)}$
$+45_{(8)}$

2. $367_{(8)}$
$+455_{(8)}$

3. $4577_{(8)}$
$+3211_{(8)}$

CONFIRM YOUR ANSWERS

K. Turn to Student Text, Volume VII and read paragraphs 1-85 through 1-86. Return to this page and answer the following questions.

SOLVE THE FOLLOWING PROBLEMS FOR THE DIFFERENCE.

1. $63_{(8)}$
$-34_{(8)}$

2. $523_{(8)}$
$-434_{(8)}$

3. $5327_{(8)}$
$-1456_{(8)}$

CONFIRM YOUR ANSWERS

MODULE SELF-CHECK

1. Write a, b, c, d, e, or f, in the spaces provided relating each term to that portion of the number.

_____	a. integral portion
3 2 0 1 (8)	b. place holder
– – – –	c. octal point
_____	d. radix
2 0 5 7 .0(8)	e. LSD
– – – – –	f. MSD

2. Write a, b, c, d, e, or f, in the spaces provided relating each term to that portion of the number.

_____	a. integral portion
1 0 1 1 (2)	b. place holder
– – – –	c. binary point
_____	d. radix
0 1 0 1 . (2)	e. LSD
– – – – –	f. MSD

3. Convert $1710_{(10)}$ to its: a. equivalent octal and b. binary value.

4. Convert $1426_{(8)}$ to its: a. equivalent decimal and b. binary value.

5. Convert $1001_{(2)}$ to its: a. equivalent decimal and b. octal value.

6. Solve for the sum.

a. $1041_{(8)} + 7652_{(8)}$

b. $726_{(8)} + 134_{(8)}$

7. Solve for the difference.

a. $274_{(8)}$
$-165_{(8)}$

b. $3145_{(8)}$
$-1432_{(8)}$

8. Solve for the sum.

a. $11011_{(2)}$
$+01101_{(2)}$

b. $1101_{(2)}$
$+\ 111_{(2)}$

c. $10100_{(2)}$
$11011_{(2)}$
$+00111_{(2)}$

9. Solve for the difference using the direct method.

a. $11001_{(2)}$
$-10110_{(2)}$

b. $11100_{(2)}$
$-10011_{(2)}$

10. Solve for the difference using the complement method.

a. $1100_{(2)}$
$-0111_{(2)}$

b. $1011_{(2)}$
$-0110_{(2)}$

CONFIRM YOUR ANSWERS

ANSWERS TO A - ADJUNCT GUIDE

1. False
2. c
3. c
4. 2 5 3 2

$2 \times 10^0 = 2 \times 1 = 2$

$3 \times 10^1 = 3 \times 10 = 30$

$5 \times 10^2 = 5 \times 100 = 500$

$2 \times 10^3 = 2 \times 1000 = 2000$

$2532_{(10)}$

If you missed ANY questions, review the material before you continue.

ANSWERS TO B - ADJUNCT GUIDE

1. 706.4 (a; b; c; d; e)
2. $509_{(10)}$ (d; a; c)
3. 12^5 (a; b; c)
4. $703_{(8)}$ (a; c; d; b)
5. $405.1_{(8)}$ (c; a; b; d)
6. $101.01_{(2)}$ (a; b; f; g; c; e; d)

If you missed ANY questions, review the material before you continue.

ANSWERS TO C - ADJUNCT GUIDE

1. $101.01_{(2)}$ (a; b; f; g; c; e; d)
2. a, c
3.

1 - 1	11 - 1011
2 - 10	12 - 1100
3 - 11	13 - 1101
4 - 100	14 - 1110
5 - 101	15 - 1111
6 - 110	16 - 10000
7 - 111	17 - 10001
8 - 1000	18 - 10010
9 - 1001	19 - 10011
10 - 1010	20 - 10100

4. 1 1 0 1

$1 \times 2^0 = 1 \times 1 = 1$

$0 \times 2^1 = 0 \times 2 = 0$

$1 \times 2^2 = 1 \times 4 = 4$

$1 \times 2^3 = 1 \times 8 = 8$

$13_{(10)}$

If you missed ANY questions, review the material before you continue.

ANSWERS TO D - ADJUNCT GUIDE

1. 37 + 2 = 18 R 1 LSD

18 + 2 = 9 R 0

9 + 2 = 4 R 1

4 + 2 = 2 R 0

2 + 2 = 1 R 0

1 + 2 = 0 R 1 MSD

$37_{(10)} = 100101_{(2)}$

ANSWERS TO D CONTINUED

2. 402 ÷ 2 = 201 R 0 LSD
   201 ÷ 2 = 100 R 1
   100 ÷ 2 = 50 R 0
   50 ÷ 2 = 25 R 0
   25 ÷ 2 = 12 R 1
   12 ÷ 2 = 6 R 0
   6 ÷ 2 = 3 R 0
   3 ÷ 2 = 1 R 1
   1 ÷ 2 = 0 R 1 MSD

   $402_{(10)} = 110010010_{(2)}$

3. 1301 ÷ 2 = 650 R 1 LSD
   650 ÷ 2 = 325 R 0
   325 ÷ 2 = 162 R 1
   162 ÷ 2 = 81 R 0
   81 ÷ 2 = 40 R 1
   40 ÷ 2 = 20 R 1
   20 ÷ 2 = 10 R 0
   10 ÷ 2 = 5 R 0
   5 ÷ 2 = 2 R 1
   2 ÷ 2 = 1 R 0
   1 ÷ 2 = 0 R 1 MSD

   $1301_{(10)} = 10100010101_{(2)}$

If you missed ANY questions, review the material before you continue.

ANSWERS TO E - ADJUNCT GUIDE

1. $31_{(10)}$
2. $21_{(10)}$
3. c
4. a
5. b, c

ANSWERS TO E CONTINUED

6. 2 3 7 1

   $1 \times 8^0 = 1 \times 1 = 1$

   $7 \times 8^1 = 7 \times 8 = 56$

   $3 \times 8^2 = 3 \times 64 = 192$

   $2 \times 8^3 = 2 \times 512 = 1024$

   $1273_{(10)}$

If you missed ANY questions, review the material before you continue.

ANSWERS TO F - ADJUNCT GUIDE

1. 38 ÷ 8 = 4 R 6 LSD

   4 ÷ 8 = 0 R 4 MSD $38_{(10)} = 46_{(8)}$

2. 122 ÷ 8 = 15 R 2 LSD

   15 ÷ 8 = 1 R 7

   1 ÷ 8 = 0 R 1 MSD $122_{(10)} = 172_{(8)}$

3. 2143 ÷ 8 = 267 R 7 LSD

   267 ÷ 8 = 33 R 3

   33 ÷ 8 = 4 R 1

   3 ÷ 8 = 0 R 4 MSD $2143_{(10)} = 4137_{(8)}$

If you missed ANY questions, review the material before you continue.

ANSWERS TO G - ADJUNCT GUIDE

1. $347_{(8)} = 231_{(10)} = 11100111_{(2)}$
2. $573_{(8)} = 379_{(10)} = 101111011_{(2)}$
3. $2135_{(8)} = 1117_{(10)} = 10001011101_{(2)}$

ANSWERS TO G CONTINUED

4. $1011_{(2)} = 13_{(8)}$

5. $1101_{(2)} = 15_{(8)}$

If you missed ANY questions, review the material before you continue.

ANSWERS TO H - ADJUNCT GUIDE

1. $1100_{(2)}$

2. $100011_{(2)}$

3. $1000101_{(2)}$

If you missed ANY questions, review the material before you continue.

ANSWERS TO I - ADJUNCT GUIDE

1. $110_{(2)}$

2. $100_{(2)}$

3. $101_{(2)}$

If you missed ANY questions, review the material before you continue.

ANSWERS TO J - ADJUNCT GUIDE

1. $121_{(8)}$

2. $1044_{(8)}$

3. $10010_{(8)}$

If you missed ANY questions, review the material before you continue.

ANSWERS TO K - ADJUNCT GUIDE

1. $27_{(8)}$

2. $67_{(8)}$

3. $3651_{(8)}$

If you missed ANY questions, review the material before you continue.

YOU MAY STUDY ANOTHER RESOURCE OR TAKE THE MODULE SELF-CHECK.

ANSWERS TO MODULE SELF-CHECK

1. $\overset{a}{\overline{3\ 2\ 0\ 1}}_{(8)}$

   f b e d

   $\overset{a}{\overline{2\ 0\ 5\ 7\ .\ 0}}_{(8)}$

   f b e c d

2. $\overset{a}{\overline{1\ 0\ 1\ 1}}_{(2)}$

   f b e d

   $\overset{a}{\overline{0\ 1\ 0\ 1}}_{(2)}$

   f b e d

3. a. $3256_{(8)}$ b. $11010101110_{(2)}$

4. a. $804_{(10)}$ b. $1100010110._{(2)}$

5. a. $9_{(10)}$ b. $11_{(8)}$

6. a. $10713_{(8)}$ b. $1062_{(8)}$

7. a. $107_{(8)}$ b. $1513_{(8)}$

8. a. $101000_{(2)}$ b. $10100_{(2)}$

   c. $110110_{(2)}$

ANSWERS TO MODULE SELF-CHECK CONTINUED

9. a. $11_{(2)}$ b. $1001._{(2)}$

10. a. $101_{(2)}$ b. $101._{(2)}$

HAVE YOU ANSWERED ALL OF THE QUESTIONS CORRECTLY? IF NOT, REVIEW THE MATERIAL OR STUDY ANOTHER RESOURCE UNTIL YOU CAN ANSWER ALL QUESTIONS CORRECTLY. IF YOU HAVE, CONSULT YOUR INSTRUCTOR FOR FURTHER GUIDANCE.

Part 4 - Microfiche

SAVE A LIFE

If you observe an accident involving electrical shock,
DON'T JUST STAND THERE - DO SOMETHING!

RESCUE OF SHOCK VICTIM

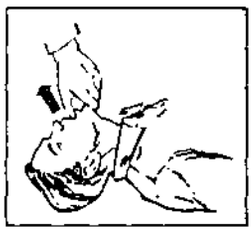
The victim of electrical shock is dependent upon you to give him prompt first aid. Observe these precautions:

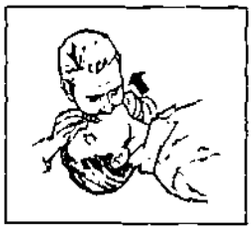
1. Shut off the high voltage.
2. If the high voltage cannot be turned off without delay, free the victim from the live conductor. REMEMBER:
   a. Protect yourself with dry insulating material.
   b. Use a dry board, your belt, dry clothing, or other non-conducting material to free the victim. When possible PUSH - DO NOT PULL the victim free of the high voltage source.
   c. DO NOT touch the victim with your bare hands until the high voltage circuit is broken.

FIRST AID

The two most likely results of electrical shock are: bodily injury from falling, and cessation of breathing. While doctors and pulmotors are being sent for, DO THESE THINGS:

1. Control bleeding by use of pressure or a tourniquet.
2. Begin IMMEDIATELY to use artificial respiration if the victim is not breathing or is breathing poorly:
   a. Turn the victim on his back.
   b. Clean the mouth, nose, and throat. (If they appear clean, start artificial respiration immediately. If foreign matter is present, wipe it away quickly with a cloth or your fingers).





   c. Place the victim's head in the "sword-swallowing" position. (Place the head as far back as possible so that the front of the neck is stretched).
   d. Hold the lower jaw up. (Insert your thumb between the victim's teeth at the midline - pull the lower jaw forcefully outward so that the lower teeth are further forward than the upper teeth. Hold the jaw in this position as long as the victim is unconscious).
   e. Close the victim's nose. (Compress the nose between your thumb and forefinger).
   f. Blow air into the victim's lungs. (Take a deep breath and cover the victim's open mouth with your open mouth, making the contact air-tight. Blow until the chest rises. If the chest does not rise when you blow, improve the position of the victim's air passageway, and blow more forcefully. Blow <u>forcefully</u> into <u>adults</u>, and <u>gently</u> into <u>children</u>.
   g. Let air out of the victim's lungs. (After the chest rises, quickly separate lip contact with the victim allowing him to exhale).
   h. Repeat steps f. and g. at the rate of 12 to 20 times per minute. Continue rhythmically without interruption until the victim starts breathing or is pronounced dead. (A smooth rhythm is desirable, but split-second timing is not essential).

DON'T JUST STAND THERE - DO SOMETHING!

PREPARE THE MAN

ATC GP 3AQR3X020-X
Prepared by Keesler TTC
KEP-GP-52

Technical Training

ELECTRONIC PRINCIPLES (MODULAR SELF-PACED)

MODULE 52

LOGIC FUNCTIONS AND BOOLEAN EQUATIONS

1 September 1975

AIR TRAINING COMMAND

7-11

Designed For ATC Course Use

ATC Keesler 6-0397

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Radar Principles Branch
Keesler Air Force Base, Mississippi

ATC GP 3AQR3X020-X
KEP-GP-52
1 September 1975

ELECTRONIC PRINCIPLES (MODULAR SELF-PACED)

MODULE 52

LOGIC FUNCTIONS AND BOOLEAN EQUATIONS

This Guidance Package is designed to guide you through this module of the Electronics Principles Course. This Guidance Package contains specific information, including references to other resources you may study, enabling you to satisfy the learning objectives.

CONTENTS

OVERVIEW

1. SCOPE: Computers operate on the movement of discrete voltage levels which represent the binary digits. The logic functions controlling these movements are called GATES. The two basic gates are the AND and the OR. Truth tables are developed for these gates when used with or without state indicators.

Boolean algebra is the language of logic operations, and it is used for analyzing malfunctions. Logic diagrams are drawn from Boolean equations.

2. OBJECTIVES: Upon completion of this module, you should be able to satisfy the following objectives:

a. Given the AND logic symbol with two inputs, construct the truth table.

b. Given the OR logic symbol with two inputs, construct the truth table.

c. Given the AND or OR logic symbol with state indicators, construct the truth table.

d. Given the exclusive OR logic symbol with two inputs, construct the truth table.

e. Given the direct coupled transistor logic (DCTL) circuitry of a series and parallel logic gate (not to exceed three inputs), draw the logic symbol for each gate.

f. Given a current mode logic circuit (CML), construct the truth table.

g. Given a Boolean equation, draw the logic diagrams (consisting of 3 to 6 gates).

LIST OF RESOURCES

To satisfy the objectives of this module, you may choose, according to your training, experience, and preferences, any or all of the following:

READING MATERIALS:

Digest
Adjunct Guide with Student Text VII

Supersedes Guidance Package, KEP-GP-52, 1 September 1974.

AT THIS POINT, IF YOU FEEL THAT THROUGH PREVIOUS EXPERIENCE OR TRAINING YOU ARE FAMILIAR WITH THIS SUBJECT, YOU MAY TAKE THE MODULE SELF-CHECK.

CONSULT YOUR INSTRUCTOR IF YOU NEED HELP.

ADJUNCT GUIDE

INSTRUCTIONS:

Study the referenced materials as directed.

Return to this guide and answer the questions.

Check your answers against the answers at the back of this Guidance Package.

Contact your instructor if you experience any difficulty.

Begin the program.

A. Turn to Student Text, Volume VII and read paragraphs 2-1 through 2-21. Study the AND gate symbol and its input and output characteristics, the actual circuit, and the truth table. Return to this page and answer the following questions.

Use figure 1 to answer questions 1, 2, and 3.

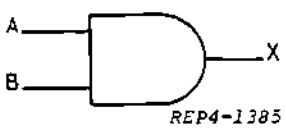


Figure 1

1. Write the correct output for the gate if A is low and B is high. X is (high) (low).

2. Write the correct output for the gate if A is high and B is high. X is (high) (low).

3. Draw the correct diode circuitry for the logic symbol.

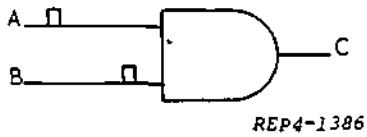


Figure 2

4. The AND gate shown in figure 2 will have an output at C if the inputs to A and B are as shown (observe pulse timing). (True) (False)

5. Construct the truth table for the logic symbol shown in figure 3.

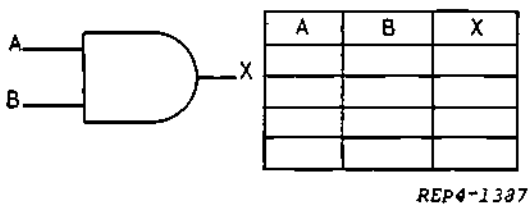


Figure 3

CONFIRM YOUR ANSWERS AT THE BACK OF THIS GUIDANCE PACKAGE.

B. Turn to Student Text, Volume VII and read paragraphs 2-22 through 2-32. Study the OR gate symbol, its input and output characteristics, the diode circuit, and the truth table. Return to this page and answer the following questions.

1. Write the correct output for the gate in figure 4 if A is low and B is high. C is (high) (low).

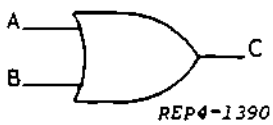
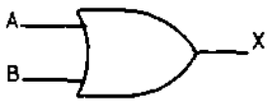


Figure 4

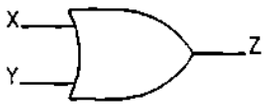
2. Write the correct output for the gate shown in figure 5, if A is high and B is low. X is (high) (low).



REP4-1390

Figure 5

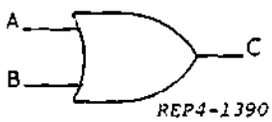
3. Write the correct output for the gate shown in figure 6, if X is high and Y is high. Z is (high) (low).



REP4-1390

Figure 6

4. Draw the correct diode circuitry for the logic symbol shown in figure 7.



REP4-1390

Figure 7

5. The OR gate shown will have an output at C if the inputs to A and B are as shown in figure 8.

a. True (one pulse only)

b. True (two pulses)

c. False

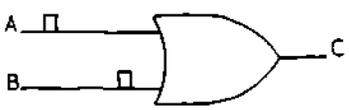
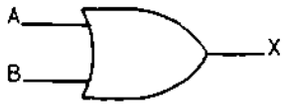


Figure 8

6. Construct the truth table for the logic symbol shown in figure 9.



REP4-1597

A	B	X

REP4-1391

Figure 9

CONFIRM YOUR ANSWERS AT THE BACK OF THIS GUIDANCE PACKAGE.

C. Turn to Student Text, Volume VII and read paragraphs 2-33 through 2-47. You will see how the input to a gate may be inhibited and also how an AND gate may be changed to a NOT AND gate. Return to this page and answer the following questions.

1. A NOT function denotes

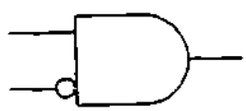
a. amplification of the signal.
b. depletion of polarity reference.
c. inversion of a signal.

2. A gate circuit is said to be INHIBITED when the state indicator is shown in the

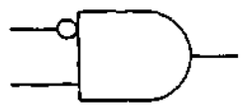
a. input.
b. output.

3. Which of the following is an AND gate notted?

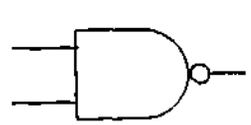
a.



b.



c.



REP4-1392

Figure 10

4. Write the correct output bit for the gate shown in figure 11, if A is high and B is high.

REP4-1393

Figure 11

5. Draw the circuit for the gate shown in figure 12.

REP4-1393

Figure 12

6. Construct the truth table for the logic symbol shown in figure 13.

A	B	X

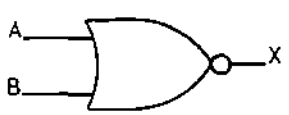
REP4-1394

Figure 13

CONFIRM YOUR ANSWERS AT THE BACK OF THIS GUIDANCE PACKAGE.

D. Turn to Student Text, Volume VII and read paragraphs 2-48 through 2-52. You will see how a basic OR gate can be changed into a NOT OR gate by adding an inverter to its output, and how the circuit actually functions. Return to this page and answer the following questions.

1. Write the correct output for the logic symbol shown in figure 14, if A and B are high.



REP4-1597

Figure 14

Use figure 15 for items 2 through 4.

REP4-1569

Figure 15

2. Write the correct output for the logic symbol shown, if A and B are low.

3. Draw the correct circuit for the gate shown.

4. Construct the truth table for the gate shown.

CONFIRM YOUR ANSWERS AT THE BACK OF THIS GUIDANCE PACKAGE.

E. Turn to Student Text, Volume VII and read paragraphs 2-53 through 2-56. Study the exclusive OR gate. Pay particular attention to the input characteristics, and note that the logic diagram is different from the logic symbol. Study the truth table carefully. Return to this page and answer the following questions.

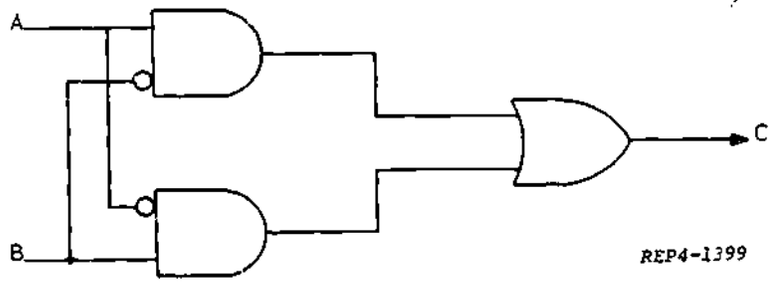


Figure 16

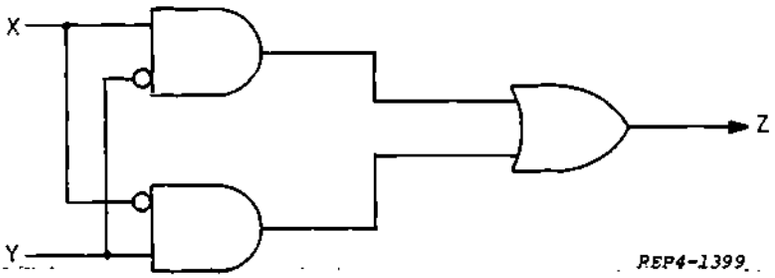


Figure 17

1. Write the correct output for the logic diagram shown in figure 16, if A is high and B is low. Output _____

2. Write the correct output for the logic diagram shown in figure 17, if X and Y are high. Output _____

3. An Exclusive OR will develop a high output when either input A or B is present, but not when BOTH inputs are present. (True) (False)

4. Draw the logic symbol for the Exclusive OR logic diagram shown in question 1.

5. Construct the truth table for Exclusive OR logic diagram shown in question 1.

A	B	C

REP4-1400

Figure 18

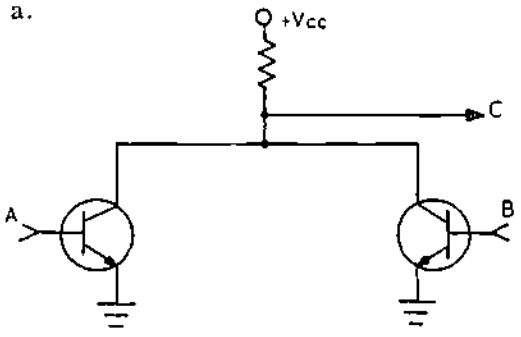
CONFIRM YOUR ANSWERS AT THE BACK OF THIS GUIDANCE PACKAGE.

_____

F. Turn to Student Text, Volume VII and read paragraphs 2-57 through 2-88. Relating to DCTL and CML. You should become aware that these circuits are AND and OR gates. Return to this page and answer the following questions.

1. Draw the logic symbols (AND or OR) which represent EACH of the following direct coupled transistor logic (DCTL) circuits.

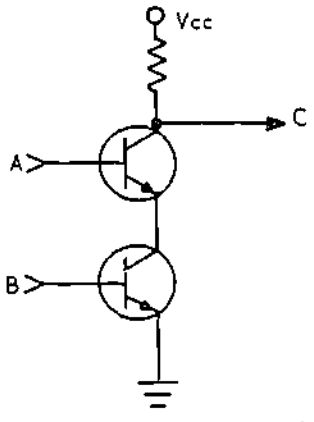
a.



REP4-1590

Figure 19

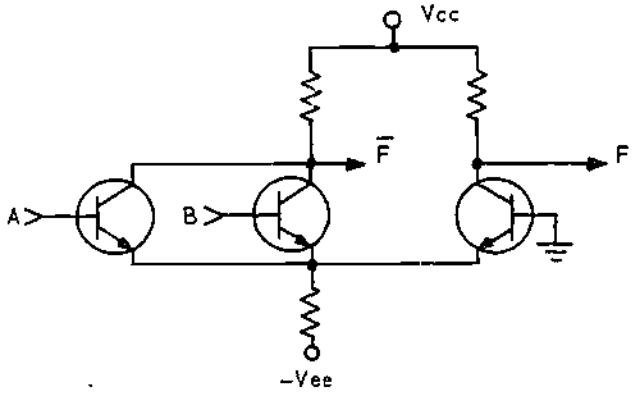
b.



REP4-1590

Figure 20

2. Write the outputs for the current mode logic circuit shown in figure 21, if A is high and B is low.



F̄ _____

F _____

REP4-1591

Figure 21

3. Construct the truth table for the current mode logic circuit shown in question 2.

A	B	F̄	F

REP4-1592

Figure 22

CONFIRM YOUR ANSWERS AT THE BACK OF THIS GUIDANCE PACKAGE.

G. Turn to Student Text, Volume VII and read paragraphs 2-89 through 2-115. Notice that each logic gate can be expressed by combinations of letters and symbols which resemble simple algebra. Be careful to note that the signs do not mean the same in Boolean algebra. Return to this page and answer the following questions.

1. Boolean algebra is used in _____

_____.

2. In Boolean algebra, the · sign means

_____ and the + sign means _____.

3. Parentheses and brackets are used for

_____.

4. A line over a letter or group of letters is called a _____.

5. The vinculum indicates the _____ or _____ function.

6. The _____ is used in diagramming an expression with a vinculum.

CONFIRM YOUR ANSWERS AT THE BACK OF THIS GUIDANCE PACKAGE.

H. Turn to Student Text, Volume VII and read paragraphs 2-116 through 2-120. Study the rules for diagramming an expression or vice versa. Return to this page and answer the following questions.

1. In diagraming an equation, the gate on the _____ is drawn first.

2. The vinculum cannot be used as a grouping sign. (True) (False)

3. Each grouping in the expression can be represented by a single gate. (True) (False)

4. The three basic logic symbols are _____, _____, and _____.

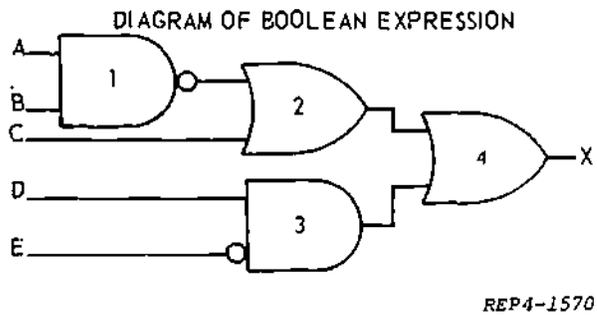
5. Draw the logic diagram for each of the following equations:

a. $\left[\overline{(A \cdot B + C)} \cdot D\right] + E = X$

b. $A \cdot B + C + \overline{D} \cdot \overline{E} = Z$

6. Write the Boolean equation for each of the following logic diagrams.

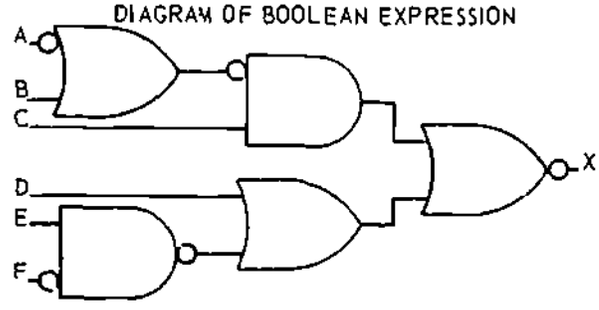
a.



REP4-1570

Figure 23

b.



REP4-1571

Figure 24

CONFIRM YOUR ANSWERS AT THE BACK OF THIS GUIDANCE PACKAGE.

A	B	X1	X2	X3	X4	X5	X6	X7
L	L							
L	H							
H	L							
H	H							

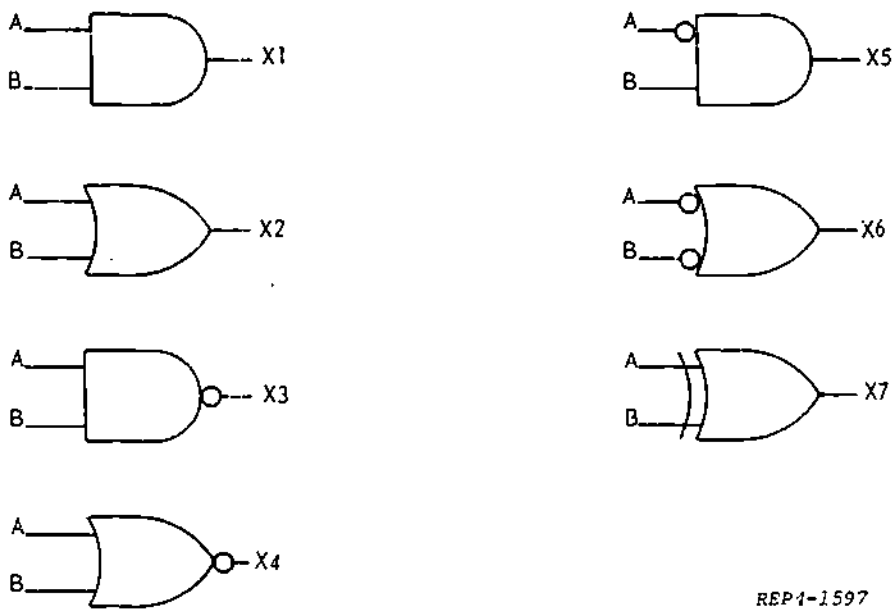


Figure 25

MODULE SELF-CHECK

Questions 1 through 7: Identify the logic symbols and complete the truth table shown in figure 25.

8. Draw the logic symbol and identify the circuit shown in figure 26.

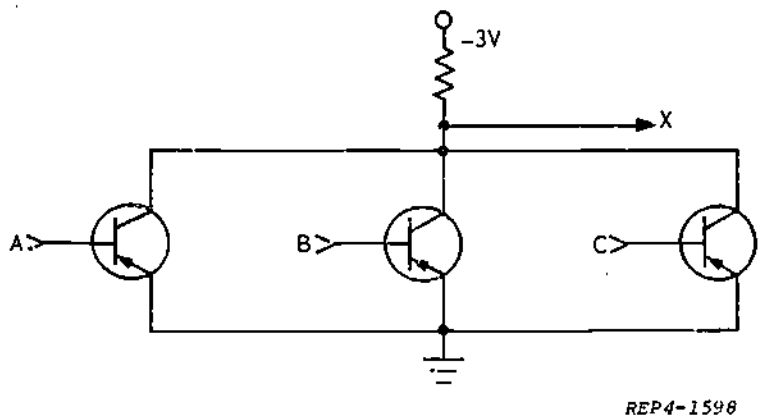


Figure 26

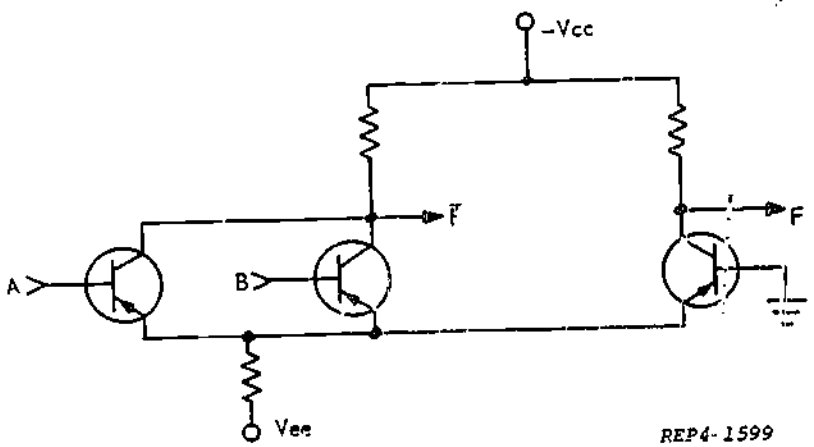


Figure 27

9. Identify the schematic shown in figure 27, and construct its truth table.

10. Draw the logic diagram for the following Boolean equations.

a. $(\overline{AB} + C)(\overline{D}E) = X$

b. $\left[(\overline{AB} + CD)(\overline{E + F})\right] + G + H = X$

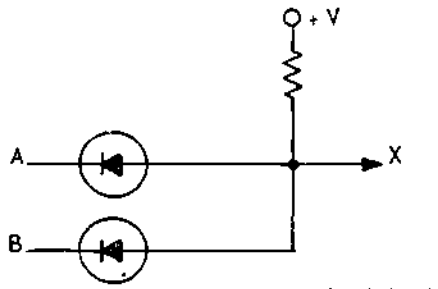
CONFIRM YOUR ANSWERS AT THE BACK OF THIS GUIDANCE PACKAGE.

ANSWERS TO A:

1. X is low.

2. X is high.

3.



REP4-1388

4. False

5.

A	B	X
H	H	H
H	L	L
L	H	L
L	L	L

REP4-1389

If you missed ANY questions, review the material before you continue.

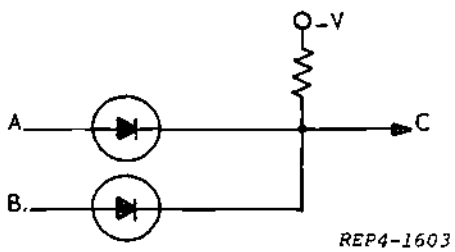
ANSWERS TO B:

1. High

2. High

3. High

4.



REP4-1603

5. b.

6.

A	B	X
H	H	H
H	L	H
L	H	H
L	L	L

REP4-1604

If you missed ANY questions, review the material before you continue.

ANSWERS TO C:

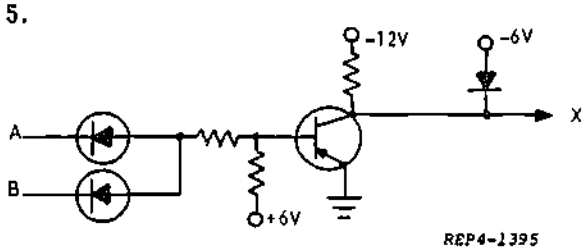
1. c

2. a

3. c

4. X is low.

5.



REP4-1395

6.

A	B	X
H	H	L
H	L	H
L	H	H
L	L	H

REP4-1396

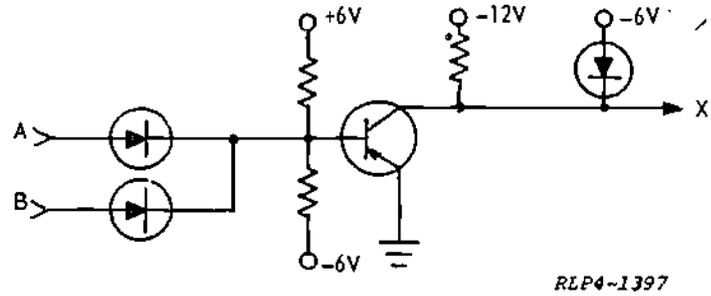
If you missed ANY questions, review the material before you continue.

ANSWERS TO D:

1. X is low.

2. X is high.

3.



RLP4-1397

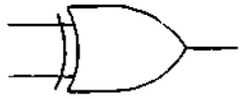
4.

A	B	X
H	H	L
H	L	L
L	H	L
L	L	H

REP4-1398

If you missed ANY questions, review the material before you continue.

ANSWERS TO E:

1. High
2. Low
3. True
4. 

REP4-1588

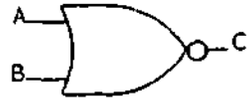
5.

A	B	C
H	H	L
H	L	H
L	H	H
L	L	L

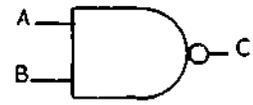
REP4-1589

If you missed ANY questions, review the material before you continue.

ANSWERS TO F:

1. a. 

REP4-1593

b. 

REP4-1593

2. $\overline{F}$ is low.

   F is high.

3.

A	B	$\overline{F}$	F
H	H	L	H
H	L	L	H
L	H	L	H
L	L	H	L

REP4-1594

If you missed ANY questions, review the material before you continue.

ANSWERS TO G:

1. Design of digital equipment
2. AND OR
3. Grouping
4. Vinculum
5. NOT Inverse
6. State indicator

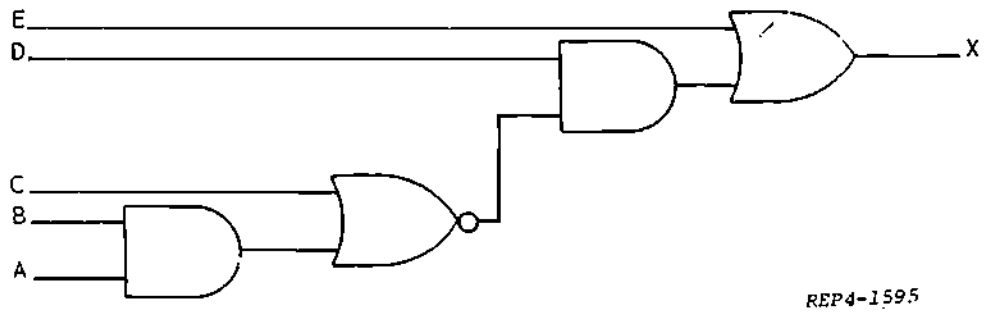
If you missed ANY questions, review the material before you continue.

ANSWERS TO H:

1. Right
2. False
3. True
4. · + -

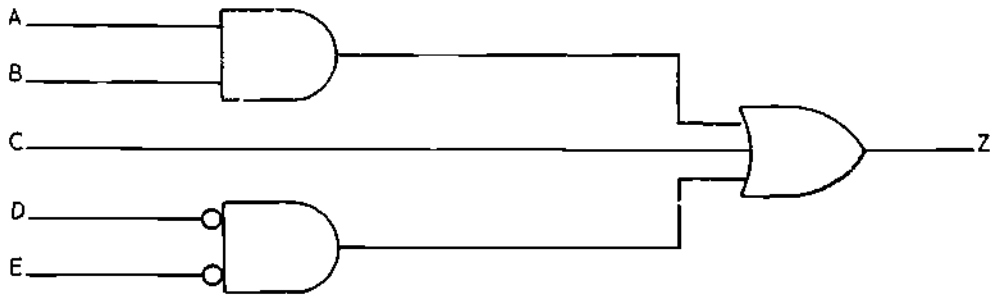
136

5. a.



REP4-1595

b.



REP4-1596

6. a. $(\overline{AB} + C) + D\overline{E} = X)$

b. $\overline{(\overline{A} + B)\,C + (D + \overline{EF})} = X$

If you missed ANY questions, review the material before you continue.

ANSWERS TO MODULE SELF-CHECK:

1. two input AND gate

2. two input OR gate

3. two input AND gate with state indicator in the output

4. two input OR gate with state indicator in the output

5. two input AND gate with state indicator on one input

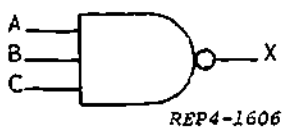
6. two input OR gate with state indicators on both inputs

7. Exclusive OR gate

A	B	X1	X2	X3	X4	X5	X6	X7
L	L	L	L	H	H	L	H	L
L	H	L	H	H	L	H	H	H
H	L	L	H	H	L	L	H	H
H	H	H	H	L	L	L	L	L

REP4-1600

8. Parallel DCTL logic circuit



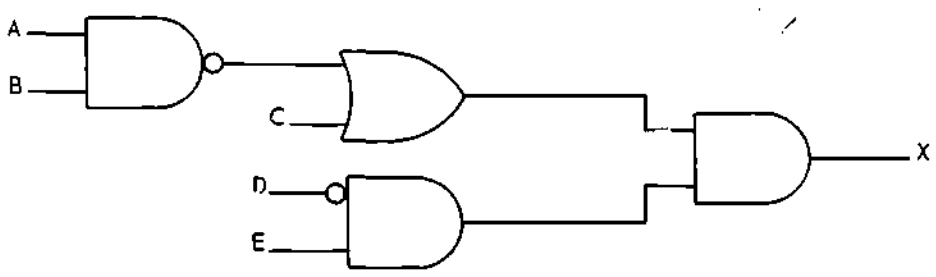
REP4-1606

9. CML, current mode logic

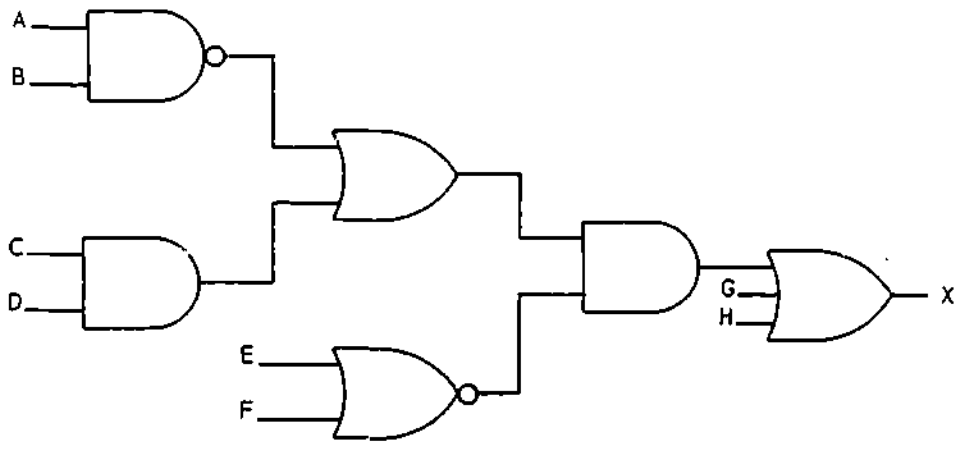
A	B	$\overline{F}$	F
L	L	H	L
L	H	H	L
H	L	H	L
H	H	L	H

REP4-1605

10. a.



b.



HAVE YOU ANSWERED ALL OF THE QUESTIONS CORRECTLY? IF NOT, REVIEW THE MATERIAL OR STUDY ANOTHER RESOURCE UNTIL YOU CAN ANSWER ALL QUESTIONS CORRECTLY. IF YOU HAVE, CONSULT YOUR INSTRUCTOR FOR FURTHER GUIDANCE.

PREPARE THE MAN

ATC GP 3AQR3X020-X
Prepared by Keesler TTC
KEP-GP-53

Technical Training

ELECTRONIC PRINCIPLES (MODULAR SELF-PACED)

MODULE 53

LOGIC CIRCUITS AND DIAGRAMS

1 July 1975

AIR TRAINING COMMAND

7-11

Designed For ATC Course Use

Radar Principles Branch
Keesler Air Force Base, Mississippi

ATC GP 3AQR3X020-X
KEP-GP-53
1 July 1975

ELECTRONIC PRINCIPLES (MODULAR SELF-PACED)

MODULE 53

LOGIC CIRCUITS AND DIAGRAMS

This Guidance Package is designed to guide you through this module of the Electronic Principles Course. This Guidance Package contains specific information, including references to other resources you may study, enabling you to satisfy the learning objectives.

CONTENTS

OVERVIEW

1. SCOPE: The series half adder is a logic circuit which can add two binary digits and develop a sum and a carry output. If a carry from a previous addition is also to be considered, then a series or parallel full adder must be used.

Multivibrators (flip-flops) are used extensively in digital computers; however, they are modified so they can perform specific functions. The Schmitt trigger and the complemented, complementing, and J-K flip-flops are discussed.

2. OBJECTIVES: Upon completion of this module, you should be able to satisfy the following objectives.

a. Given a logic diagram of a serial half or full adder, write all possible sum and carry expressions.

b. Given a logic diagram of a four-bit input parallel full adder, trace data flow and write the state of each sum and carry output.

c. Given a schematic diagram containing a two input AND gate, differentiating network, clipping diode, and set or clear input, identify the correct output waveshape for a given input.

d. Given a schematic diagram of the complemented or complementing flip-flop and of the Schmitt trigger, identify the logic symbols and trace data flow.

e. Given a logic symbol of a J-K flip-flop, construct the truth table.

LIST OF RESOURCES

To satisfy the objectives of this module, you may choose according to your training, experience, and preferences, any or all of the following:

READING MATERIALS:

Digest

Adjunct Guide with Student Text VII

Supersedes Guidance Package, KEP-GP-53, 1 February 1975.

AT THIS POINT, IF YOU FEEL THAT THROUGH PREVIOUS EXPERIENCE OR TRAINING YOU ARE FAMILIAR WITH THIS SUBJECT, YOU MAY TAKE THE MODULE SELF-CHECK.

CONSULT YOUR INSTRUCTOR IF YOU NEED HELP.

ADJUNCT GUIDE

INSTRUCTIONS:

Study the referenced materials as directed.

Return to this guide and answer the questions.

Check your answers against the answers at the back of this Guidance Package.

Contact your instructor if you experience any difficulty.

Begin the program.

A. Turn to Student Text, Volume VII, and read paragraphs 3-1 through 3-14. Study how flip-flops are connected so that binary addition can be performed. Note that the four rules of binary addition are satisfied. Return to this page and answer the following questions.

1. The half adder used in the _____ column only.

2. The half adder has _____ inputs and _____ outputs.

3. The full serial adder has _____ inputs and _____ outputs.

4. The serial full adder consists of _____ half adders.

5. What is the advantage and disadvantage of the serial full adder?

6. What is the advantage and disadvantage of the parallel adder?

CONFIRM YOUR ANSWERS AT THE BACK OF THIS GUIDANCE PACKAGE.

B. Turn to Student Text, Volume VII, and read paragraphs 3-15 through 3-36. Learn how multivibrators are modified for use in digital data processing equipment. Return to this page and answer the following questions.

1. The two general types of multivibrators most often used in digital equipment are _____ and the _____.

2. The monostable multivibrator is called _____ and is often referred to as the _____ in symbols.

3. The monostable multivibrator is used for _____.

4. Two purposes of the Schmitt trigger are _____ and _____.

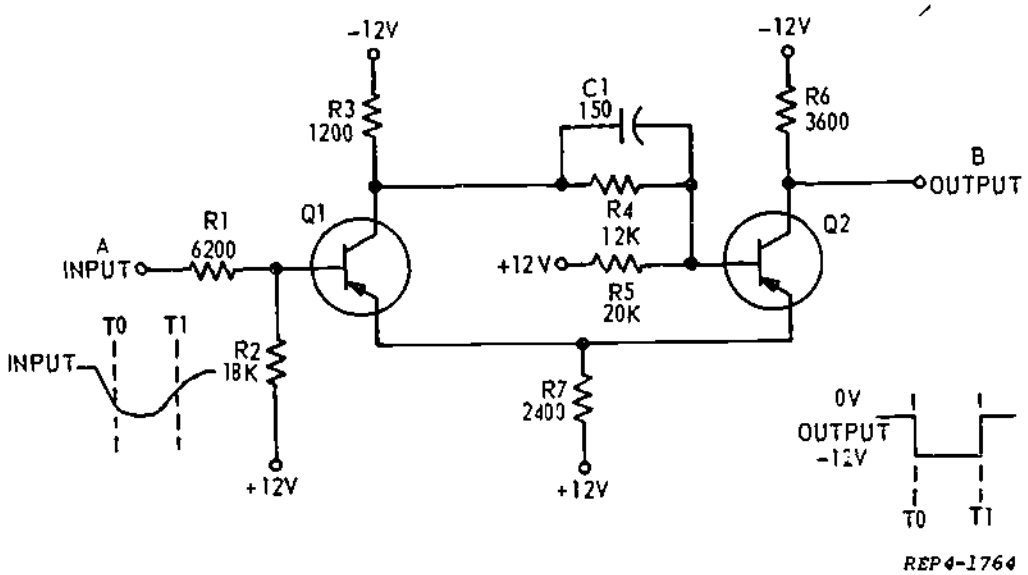


Figure 1. Schmitt Trigger

NOTE: Refer to figure 1 for questions 5 and 6.

5. A negative pulse at the input to the Schmitt trigger will cause transistor _____ to conduct.

6. Q1 will continue to conduct as long as the _____.

CONFIRM YOUR ANSWERS AT THE BACK OF THIS GUIDANCE PACKAGE.

C. Turn to Student Text, Volume VII, and read paragraphs 3-37 through 3-46. Learn how bistable multivibrators are modified to form complemented flip-flops. Return to this page and answer the following questions.

1. The common term for the bistable multivibrator is the _____.

2. Three uses for the FF are _____, _____, and _____.

3. A FF in the ZERO state will have a high at the _____ and a low at the _____.

4. The S input will cause a FF to be in the _____, and the C input will put it in the _____.

5. The T input will _____.

6. In figure 3-10, the purpose of diodes CR1 through CR4 is _____.

7. In figure 3-10, transistors _____ and _____ make up the basic multivibrator.

8. In figure 3-10, the purpose of CR5, CR6, and R7 is _____.

9. The FF changes state on the _____ clock.

CONFIRM YOUR ANSWERS AT THE BACK OF THIS GUIDANCE PACKAGE.

D. Turn to Student Text, Volume VII, and read paragraphs 3-47 through 3-65. Another version of the bistable multivibrator is the complementing flip-flop. Notice the differences between complemented and complementing FFs. Return to this page and answer the following questions.

Refer to figure 3-13 for questions 1 through 3.

1. The purpose of diodes CR1 and CR2 is _____.

2. Negative polarity triggers will cause the FF to _____.

3. Positive polarity triggers will cause the FF to _____.

Refer to figure 3-15 for questions 4 through 7.

4. The DCTL FF is the _____ _____ type.

5. Transistors _____ and _____ make up the basic multivibrator.

6. When C1 is charged, the FF is in the _____ state.

7. Transistors _____ and _____ are conducting when the FF is in the ONE state.

8. Draw the logic symbol for (a) the complemented FF, (b) the complementing FF.

CONFIRM YOUR ANSWERS AT THE BACK OF THIS GUIDANCE PACKAGE.

E. Turn to Student Text, Volume VII, and read paragraphs 3-66 through 3-69. Learn circuit operation of J-K flip-flop and Schmitt trigger, and their use in digital equipment. Return to this page and answer the following questions.

1. Will a high at J or K change the state of the FF with no triggers applied?

2. The complement of the RESET state of the FF is the _____ state.

3. Draw the logic symbol for a J-K flip-flop.

CONFIRM YOUR ANSWERS AT THE BACK OF THIS GUIDANCE PACKAGE.

YOU MAY STUDY ANOTHER RESOURCE OR TAKE THE MODULE SELF-CHECK.

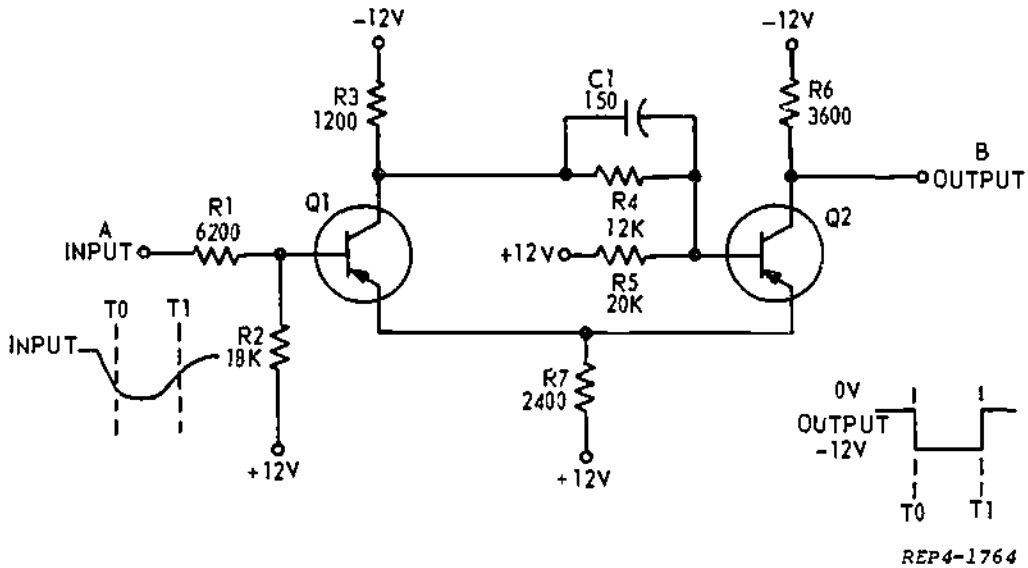


Figure 1. Schmitt Trigger

MODULE SELF-CHECK

Refer to figure 1 for questions 1 and 2.

1. The purpose of the Schmitt trigger is to

___ a. store a binary zero.

___ b. delay a pulse.

___ c. restore the shape of a pulse.

___ d. invert a pulse.

2. With no signal in, Q1 and Q2 are both cut off. A possible trouble is

___ a. R3 open.

___ b. R4 short.

___ c. R5 open.

___ d. C1 open.

3. The purpose of the monostable multivibrator is _____.

4. In digital circuits the bistable multivibrator is known as a _____.

5. The bistable multivibrator is used for _____ and _____.

6. Which circuit is represented by each diagram, A and B, in figure 2?

7. With a high on the J input, and low on the K input, the J-K flip-flop will be in the _____ state after the trigger down clocks.

8. Given the half adder shown in figure 3, write all possible sum and carry expressions.

9. Given the full adder shown in figure 4, write all possible sum and carry expressions.

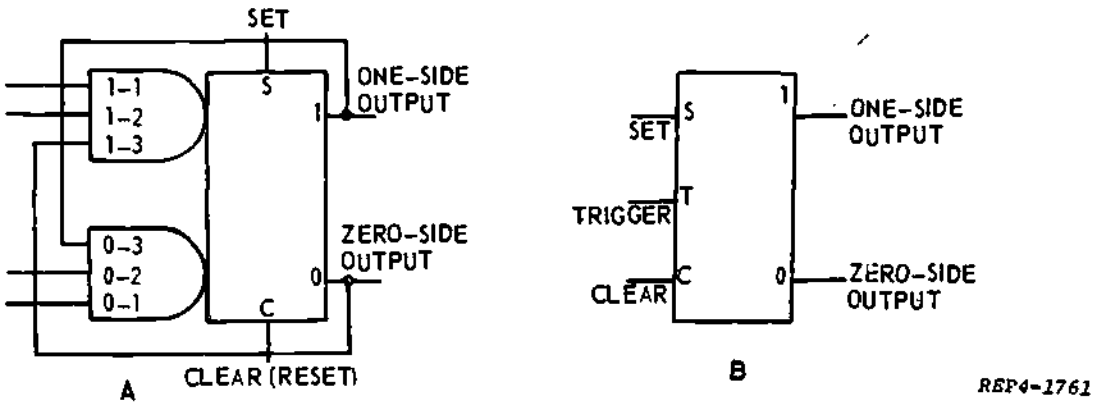


Figure 2

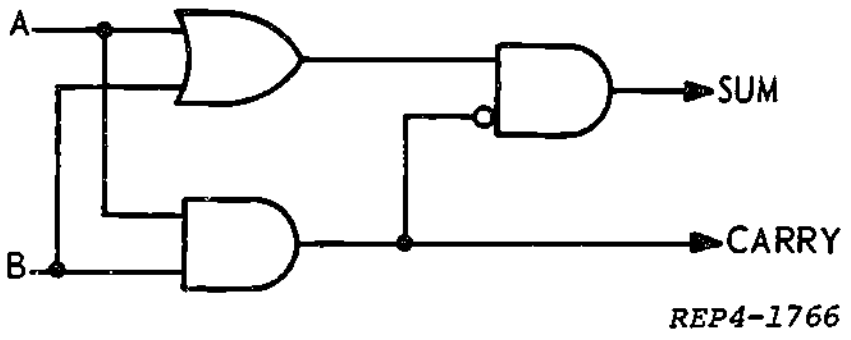


Figure 3

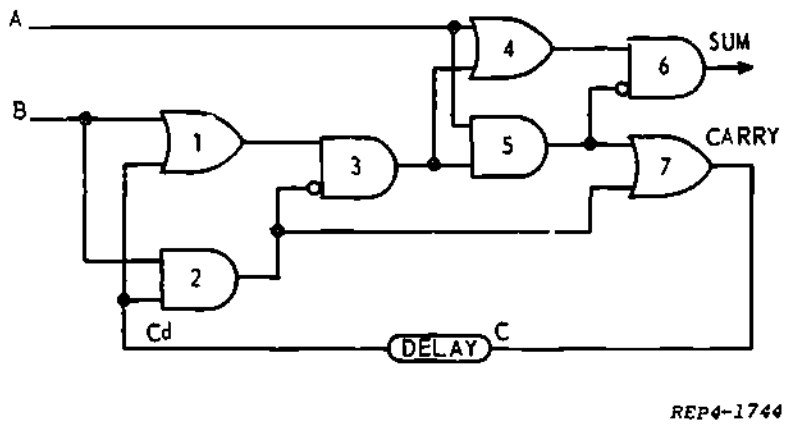


Figure 4

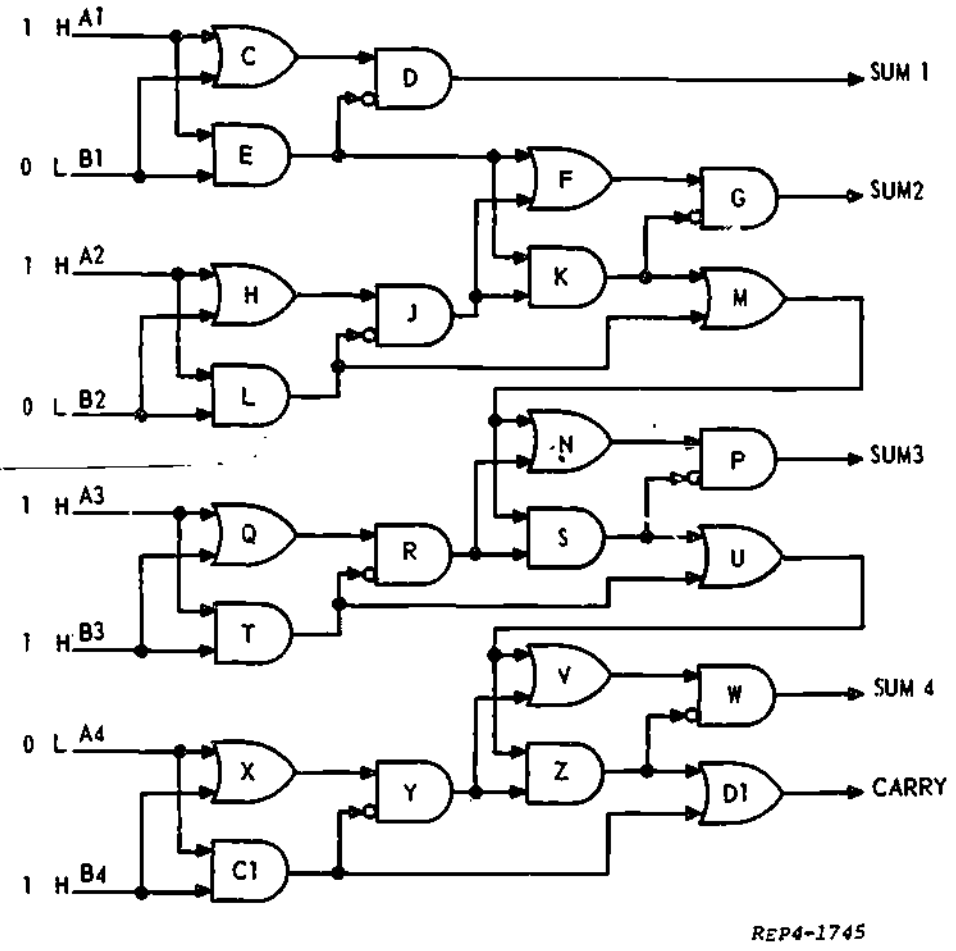


Figure 5

10. With the given inputs to A and B in figure 5, write 1 or 0 for each of the sum and carry outputs. NOTE: 1 = H, 0 = L.

CONFIRM YOUR ANSWERS AT THE BACK OF THIS GUIDANCE PACKAGE.

ANSWERS TO A:

1. LSD

2. Two, two

3. Three, two

4. Two

5. advantage - cheaper
   disadvantage - slower

6. advantage - faster
   disadvantage - more expensive

If you missed ANY questions, review the material before you continue.

ANSWERS TO B:

1. Monostable and bistable

2. Single shot, SS

3. Pulse stretching or shaping, and gate delay and adjust

4. Squaring off a rounded wave, voltage level sensing

5. Q1

6. Signal exceeds the threshold voltage of Q1.

If you missed ANY questions, review the material before you continue.

ANSWERS TO C:

1. flip-flop

2. counters, storage registers, shift registers

3. ZERO side, ONE side

4. ONE state, ZERO state

5. Reverse condition of FF

6. To limit logic voltage level changes to 0V and -10V.

7. Q3, Q4

8. Two input AND gate to C side

9. Down

If you missed ANY questions, review the material before you continue.

ANSWERS TO D:

1. Pulse steering

2. Change states

3. Remain the same

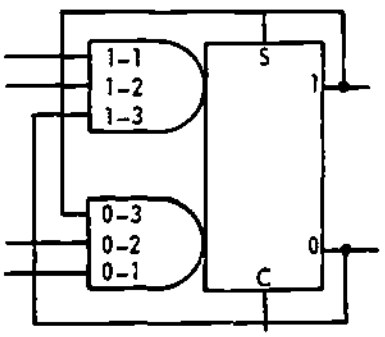
4. Complementing

5. Q6, Q7

6. ONE

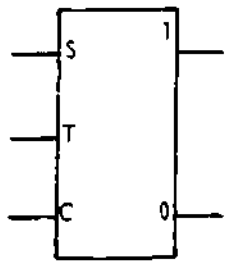
7. Q6, Q4

8. a.



A – COMPLEMENTED FLIP-FLOP

b.



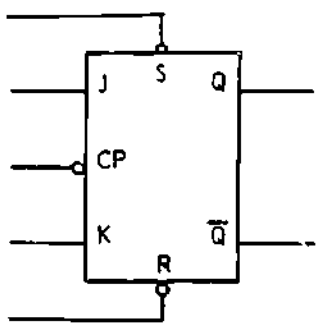
B – COMPLEMENTING FLIP-FLOP

REP4-1761

If you missed ANY questions, review the material before you continue.

ANSWERS TO E:

1. No
2. ONE
3.



REP4-1737

If you missed ANY questions, review the material before you continue.

ANSWERS TO MODULE SELF-CHECK:

1. c
2. a
3. pulse stretching or gate delay
4. flip-flop
5. counters, registers
6. complemented FF, complementing FF
7. Q
8. SUM = $\bar{A}B + A\bar{B}$, CARRY = AB
9. SUM = $\bar{A}\bar{B}C_d + \bar{A}B\bar{C}_d + ABC_d + A\bar{B}\bar{C}_d$

   CARRY = $\bar{A}BC_c + A\bar{B}C_d + ABC_d + ABC_d$
10. SUM 1 = 1, SUM 2 = 1, SUM 3 = 0, SUM 4 = 0, CARRY = 1

HAVE YOU ANSWERED ALL OF THE QUESTIONS CORRECTLY? IF NOT, REVIEW THE MATERIAL OR STUDY ANOTHER RESOURCE UNTIL YOU CAN ANSWER ALL QUESTIONS CORRECTLY. IF YOU HAVE, CONSULT YOUR INSTRUCTOR FOR FURTHER GUIDANCE.

ATC GP 3AQR3X020-X
Prepared by Keesler TTC
KEP-GP-54

Technical Training

ELECTRONIC PRINCIPLES (MODULAR SELF-PACED)

MODULE 54

COUNTERS, REGISTERS, AND STORAGE DEVICES

October 1975

AIR TRAINING COMMAND

7-11

Radar Principles Branch
Keesler AFB, Mississippi

ATC GP 3AQR3X020-X
KEP-GP-54
October 1975

ELECTRONIC PRINCIPLES

MODULE 54

COUNTERS, REGISTERS, AND STORAGE DEVICES

This Guidance Package is designed to guide you through this module of the Electronics Principles Course. This Guidance Package contains specific information, including references to other resources you may study, enabling you to satisfy the learning objectives.

CONTENTS

OVERVIEW

1. SCOPE: Digital data processors require timing for program sequencing. Counters, consisting of cascaded flip-flops, perform this function by monitoring the number of input pulses. The types of counters are the up-counter, down-counter, decade counter, and the ring counter. AND gates may be connected to a counter to detect a particular count.

A storage register is a group of flip-flops used to store information temporarily while other data is being processed. A shift register can also store data, but it has the additional capability of having the information extracted when needed. Magnetic cores, drums, and tapes are used for permanent storage.

2. OBJECTIVES: Upon completion of this module you should be able to satisfy the following objectives.

a. Given a four stage up-counter logic diagram having complemented flip-flops, trace data flow and write in the binary count after a clear pulse and a given clock pulse has passed.

b. Given a four stage serial up counter or down counter logic diagram having complementing flip-flops, write in the binary count after a clear or set pulse and a given clock pulse has passed.

c. Given the logic diagram of a decade counter, trace data flow to construct the truth table.

d. Given a logic diagram of a four stage ring counter and a number of input pulses, write the correct state of each flip-flop.

e. Given the logic diagram of a count detect circuit, select the AND gate connections to indicate a required count.

f. Given the logic diagram of a serial up-counter, with a given count, feeding a parallel storage register, trace data flow and write the binary count stored in the register after a read-in pulse has passed.

Supersedes Guidance Package, KEP-GP-54, 1 September 1974.

g. Given a three stage shift register diagram and a given count, trace data flow and write the state of each flip-flop after a specified number of shift pulses have passed.

h. Given the logic symbols of an amplifier, time delay shift register, and a storage register, identify each symbol.

i. Match the following list of magnetic storage devices to the statement which describes their functional characteristics:

(1) Tape

(2) Drum

(3) Core

LIST OF RESOURCES

To satisfy the objectives of this module, you may choose, according to your training, experience, and preferences, any or all of the following:

READING MATERIALS:

Digest
Adjunct Guide with Student Text, Volume VII

AT THIS POINT, IF YOU FEEL THAT THROUGH PREVIOUS EXPERIENCE OR TRAINING YOU ARE FAMILIAR WITH THIS SUBJECT, YOU MAY TAKE THE MODULE SELF-CHECK.

CONSULT YOUR INSTRUCTOR IF YOU NEED HELP.

ADJUNCT GUIDE

INSTRUCTIONS:

Study the referenced materials as directed.

Return to this guide and answer the questions.

CONFIRM YOUR ANSWERS AT THE BACK OF THIS GUIDANCE PACKAGE.

Contact your instructor if you experience any difficulty.

Begin the program.

A. Turn to Student Text, Volume VII and read paragraphs 4-1 through 4-3. Return to this page and answer the following questions.

1. Counters may be connected to count _____ or _____.

2. When using an up-counter it is usually cleared to all _____ and can be _____ to any number.

3. A counter may be triggered on the up-clock or down-clock. (TRUE) (FALSE)

4. An up-counter could be triggered on the down-clock. (TRUE) (FALSE)

5. The purpose of the up or down-counter is _____.

6. In a special up-counter, each flip-flop makes a transition when the preceding flip-flop goes from the _____ state to the _____ state.

7. Define down-clock.

8. In a basic counter, each flip-flop represents a power of _____.

CONFIRM YOUR ANSWERS

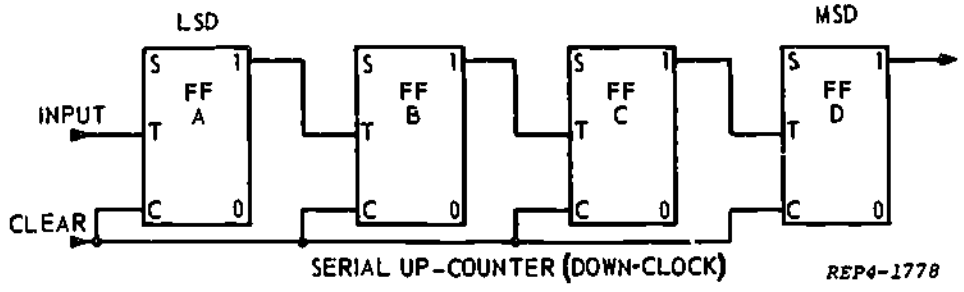


Figure 1

B. Turn to Student Text, Volume VII and read paragraphs 4-9 through 4-25. Return to this page and answer the following questions. Refer to figure 1 (or ST-VII, figure 4-2) for questions 1 thru 4.

1. In the serial up-counter, the input to each flip-flop is taken from the (one) (zero) side of the preceding stage.

2. What is the state of each flip flop of the counter if one clear pulse and six trigger pulses have passed?

FFA _____

FFB _____

FFC _____

FFD _____

3. What is the state of each flip-flop of the counter if a clear pulse and ten triggers have passed?

FFA _____

FFB _____

FFC _____

FFD _____

4. If the up-counter is cleared and twenty trigger pulses are applied, the count will be _____.

Refer to figure 4-4 of ST-VII for questions 5 thru 8.

5. A counter designed to decrease its count by one with each pulse is called a/an _____.

6. The _____ output side is used to trigger the next flip-flop in the down-counter.

7. A four-stage down-counter is set to the maximum count. What takes place in the counter when a pulse is applied?

8. The count in a serial down-counter is ten. How many down-clocks have passed if the count started at 15?

9. In up or down-counters, each flip-flop requires _____ input pulses to produce two triggers to the next stage.

CONFIRM YOUR ANSWERS

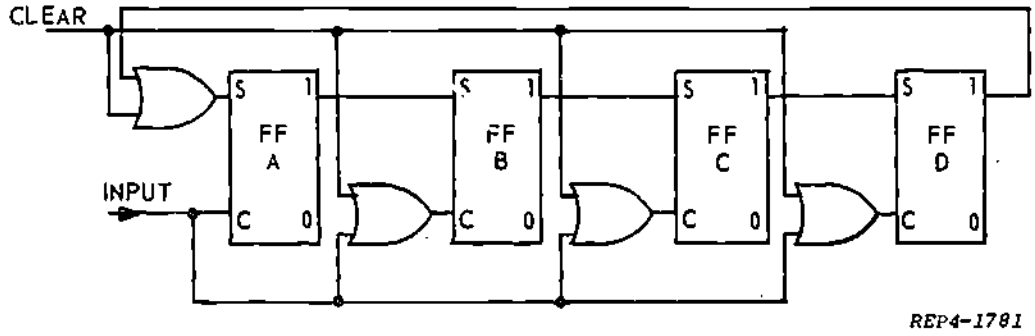


Figure 2. Ring Counter

C. Turn to Student Text, Volume VII and read paragraphs 4-26 through 4-33. Return to this page and answer the following questions.

Refer to figure 2 (or figure 4-5 of ST-VII) for questions 1 thru 5.

1. A ring counter can be used for

   a. sequencing.

   b. permanent storage.

2. How many input pulses are required to return a four stage ring counter to its original state?

3. FFA of the ring counter shown changes states (every) (every other) (every third) (every fourth) time a pulse is applied.

4. To indicate a given count, only the high output of a specific stage is necessary in a ring counter. (TRUE) (FALSE)

5. Write the state of each flip-flop in the ring counter if one clear pulse and seven down-clock pulses have been applied.

6. How many flip-flops can be in the ONE state at a given time?

CONFIRM YOUR ANSWERS

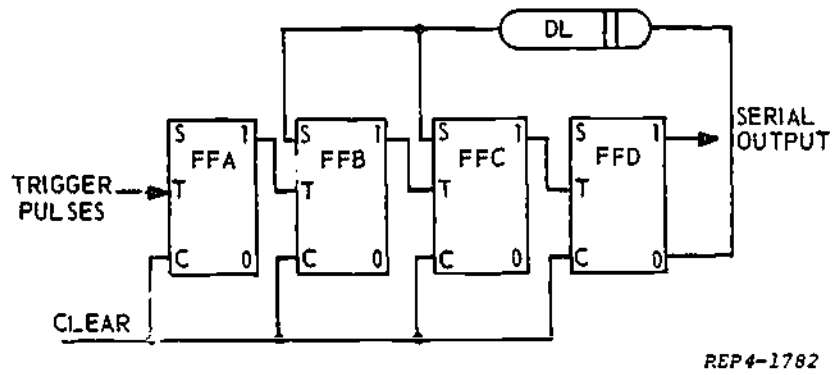


Figure 3. Decade Counter

D. Turn to Student Text, Volume VII and read paragraphs 4-34 through 4-41. Return to this page and answer the following questions.

Refer to figure 3 (or figure 4-6 of ST-VII) for questions 1 thru 4.

1. Write one or zero for the condition of each flip-flop in the decade counter if a clear pulse and five trigger pulses have passed.

2. The decade counter will return to all zeroes every _____ pulse.

3. There are _____ possible conditions for a four stage decade counter.

4. The only time the feedback to flip-flops B and C have any effect on operation of the circuit is on the _____ pulse.

CONFIRM YOUR ANSWERS

E. Turn to Student Text, Volume VII and read paragraphs 4-42 through 4-48. Return to this page and answer the following questions.

Refer to figure 4 (or figure 4-7 of ST-VII) for questions 1 thru 4.

1. A count detect circuit can direct the operation of other equipment when a certain count is reached. (TRUE)(FALSE)

2. Count detect circuits can NOT give you a digital read out. (TRUE)(FALSE)

3. What count will this circuit detect?

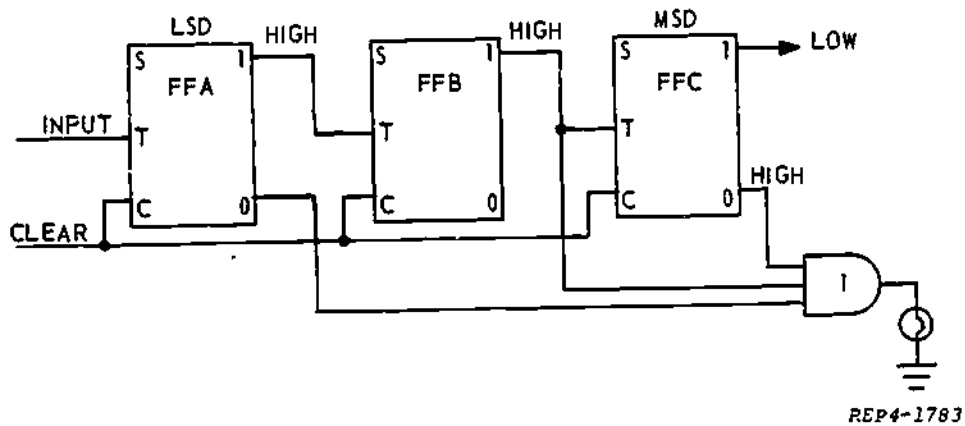


Figure 4. Count Detect

4. Draw an AND gate connected to the counter to make it possible to detect the number five.

CONFIRM YOUR ANSWERS

F. Turn to Student Text, Volume VII and read paragraphs 4-49 through 4-71. Return to this page and answer the following questions.

Refer to figure 5 (or figure 4-10 of ST-VII) for questions 1 thru 7.

1. The purpose of a storage register is

_____

_____

_____

2. What determines the storage capacity of a register?

3. The data in the storage register is

_____ while the counter is working.

4. How many read-in pulses are required to transfer data into a four-stage parallel storage register?

5. Is it necessary to clear the information from storage registers before new information is brought in?

6. Given a count of five, what is the state of each flip-flop (1 or 0) in the storage register after a read pulse passes?

FFE _____

FFF _____

FFG _____

FFH _____

7. The shift register has a _____

input and a _____ tput.

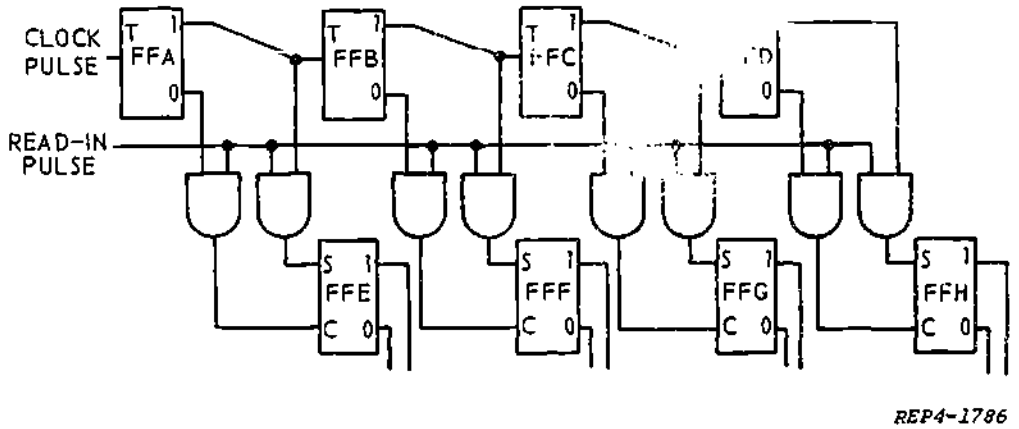


Figure 5. Parallel Storage Register

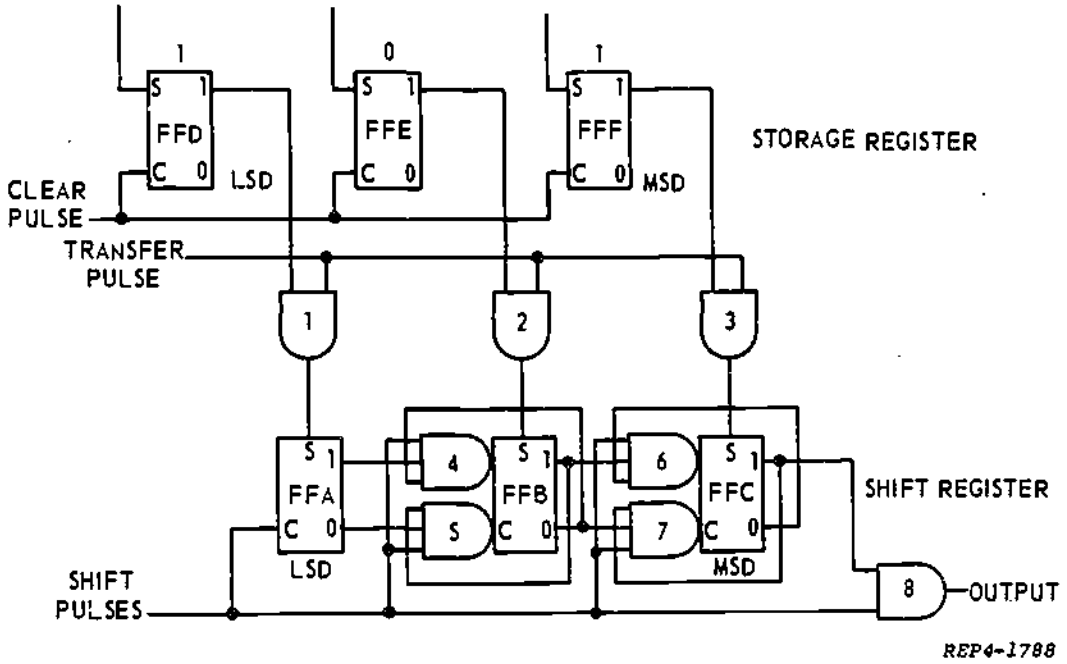


Figure 6. Shift Register

Refer to figure 6 for question 8.

8. How many shift pulses are required to shift out a count of $101_{(2)}$ from the shift register?

9. Two methods of moving data out of a shift register are _____

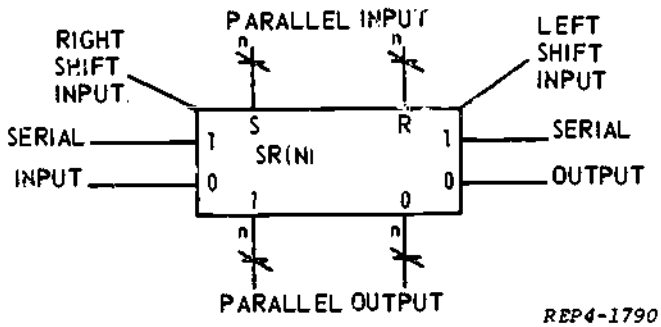
and _____.

CONFIRM YOUR ANSWERS

G. Turn to Student Text, Volume VII and read paragraphs 4-72 through 4-74. Return to this page and answer the following questions.

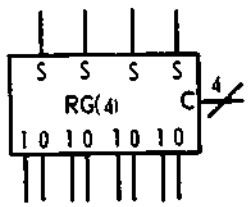
1. Identify the symbols.

CONFIRM YOUR ANSWERS



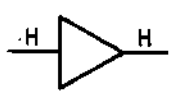
REP4-1790

A _____

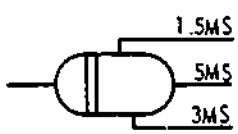


REP4-1789

B _____



C _____



REP4-1791

D _____

Figure 7

H. Turn to Student Text, Volume VII and read paragraphs 4-75 through 4-109. Return to this page and answer the following questions.

1. The two most important characteristics of any memory device are _____ _____ and _____ _____.

2. What is the difference between binary bit and binary word?

3. The two modes of access are _____ and _____.

4. Of the two access modes the fastest average access time is _____.

5. Three examples of erasable storage devices are _____, _____, and _____.

6. Two examples of nonerasable storage devices are _____ and _____.

7. Define volatility.

_____

_____

8. Three storage devices in common use today are the _____, the _____, and the _____.

9. Of the three storage devices, the _____ has the fastest access and the _____ has the largest capacity.

CONFIRM YOUR ANSWERS

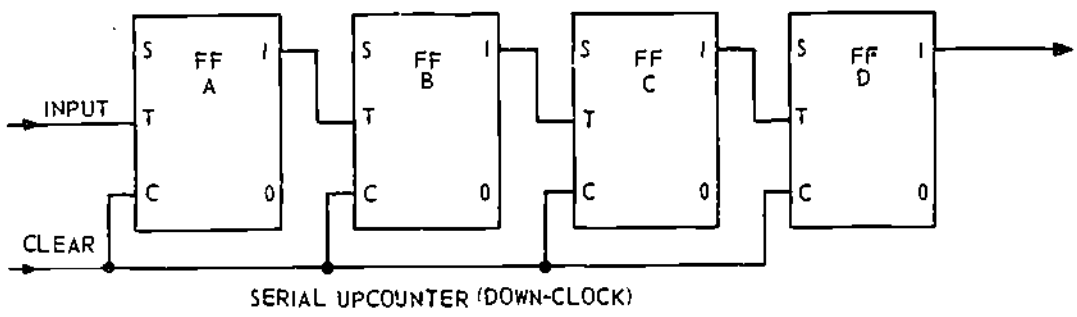
_____

MODULE SELF-CHECK

1. A four stage up or down-counter has _____ possible states.

2. The highest count possible for a four stage up-counter is _____.

3. Write the state of each FF after a clear pulse and ten input clock pulses have passed.



SERIAL UPCOUNTER (DOWN-CLOCK)

REP4-1746

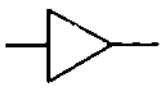
Figure 8

4. There are _____ possible states for a four stage decade counter.

5. A ring counter will have _____ _____ FF set at any one time.

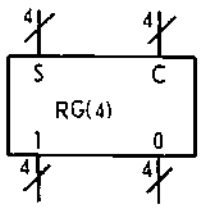
6. Identify the following symbols:

_____ a.



_____ b.

_____ c.



7. Data from an up-counter is brought into a storage register in (series) (parallel).

8. Data in the storage register (changes) (does not change) as the counter continues processing.

9. Data is brought into a shift register in (series)(parallel) and taken out in (series) (parallel).

10. Shifting data out of a three stage shift register requires _____ shift pulses.

11. List two important characteristics to be considered in selecting a memory system.

a. _____

b. _____

CONFIRM YOUR ANSWERS

ANSWERS TO A - ADJUNCT GUIDE

1. up or down
2. zeroes; preset
3. TRUE
4. TRUE
5. to time when operations are to be performed.
6. ONE; ZERO
7. The negative going portion of a square wave.
8. two.

If you missed ANY questions, review the material before you continue.

ANSWERS TO B - ADJUNCT GUIDE

1. one
2. FFA 0, FFB 1, FFC, 1, FFD 0
3. FFA 0, FFB 1, FFC 0, FFD 1
4. four
5. down-counter
6. zero
7. The count will go to 14. FFA to ZERO state, all others stay in the ONE state.
8. five
9. four

If you missed ANY questions, review the material before you continue.

ANSWERS TO C - ADJUNCT GUIDE

1. a
2. four
3. every fourth
4. TRUE
5. FF A, B, & C - zero, and FFD - 1.
6. one

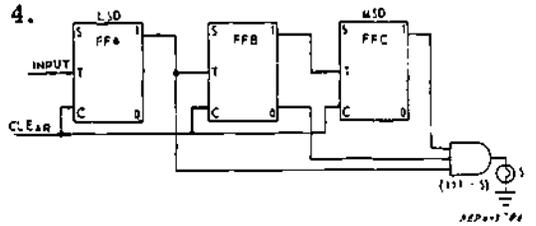
If you missed ANY questions, review the material before you continue.

ANSWERS TO D - ADJUNCT GUIDE

1. FFA 1
   FFB 0
   FFC 1
   FFD 0
2. tenth
3. ten
4. eighth

If you missed ANY questions, review the material before you continue.

ANSWERS TO E - ADJUNCT GUIDE

1. TRUE
2. FALSE
3. 2
4. 

If you missed ANY questions, review the material before you continue.

ANSWERS TO F - ADJUNCT GUIDE

1. To store binary information for future use.
2. The number of flip-flops in the register.
3. not affected.
4. one
5. no
6. FFE = 1, FFF = 0, FFG = 1, FFH = 0
7. parallel; serial
8. three
9. left to right; right to left.

If you missed ANY questions, review the material before you continue.

ANSWERS TO G - ADJUNCT GUIDE

1. a. Shift Register
   b. Storage Register
   c. Amplifier
   d. Delay Line

If you missed ANY questions, review the material before you continue.

ANSWERS TO H - ADJUNCT GUIDE

1. access time and storage capacity.
2. Binary bit is one digit. A binary word consists of several digits.
3. random and sequential.
4. random.
5. magnetic tape, drum, and core.
6. punched cards and tape.
7. If data is lost when the power is lost, the memory system is said to be volatile.
8. magnetic tape, core, drum.
9. core, tape.

If you missed ANY questions review the material before you continue.

YOU MAY STUDY ANOTHER RESOURCE OR TAKE THE MODULE SELF-CHECK.

ANSWERS TO MODULE SELF-CHECK

1. 16
2. 15
3. FFA - 0, FFB - 1, FFC - 0, FFD - 1
4. 10
5. only one
6. a. Amplifier
   b. Delay
   c. Storage Register
7. parallel
8. does not change
9. parallel; series
10. 3
11. access time (or speed) and capacity.

HAVE YOU ANSWERED ALL OF THE QUESTIONS CORRECTLY? IF NOT REVIEW THE MATERIAL OR STUDY ANOTHER RESOURCE UNTIL YOU CAN ANSWER ALL QUESTIONS CORRECTLY. IF YOU HAVE, CONSULT YOUR INSTRUCTOR FOR FURTHER GUIDANCE.

NOTES

ATC GP 3AQR3X020-X
Prepared by Keesler TTC
KEP-GP-55

Technical Training

ELECTRONIC PRINCIPLES (MODULAR SELF-PACED)

MODULE 55

DIGITAL/ANALOG CONVERTERS

March 1976

AIR TRAINING COMMAND

7-11

Radar Principles Branch
Keesler Air Force Base, Mississippi

ATC GP 3AQR3X020-X
KEP-GP-55
March 1976

ELECTRONIC PRINCIPLES (MODULAR SELF-PACED)

MODULE 55

DIGITAL/ANALOG CONVERTERS

CONTENTS

OVERVIEW

1. SCOPE: A digital-to-analog converter is a voltage divider resistive ladder whose output voltage is proportional to the binary count in a counter. The resistance of each leg of the resistive ladder is determined by the state of each FF in the counter. An analog-to-digital converter will change a variable voltage to an equivalent binary count in a digitizer unit.

2. OBJECTIVES: Upon completion of this module you should be able to satisfy the following objectives.

a. Given a circuit diagram of an electromechanical digital to analog converter, write the output voltage for a specified count in the counter.

b. Given a circuit diagram of an analog-to-digital converter using variable time conversion, select the portions of the circuit that perform the sample, hold, compare, and digitize functions.

LIST OF RESOURCES

To satisfy the objectives of this module, you may choose, according to your training, experience, and preferences, any or all of the following:

READING MATERIALS:

Digest

Adjunct Guide with Student Text, Volume VII

AT THIS POINT, IF YOU FEEL THAT THROUGH PREVIOUS EXPERIENCE OR TRAINING YOU ARE FAMILIAR WITH THIS SUBJECT, YOU MAY TAKE THE MODULE SELF-CHECK.

CONSULT YOUR INSTRUCTOR IF YOU NEED HELP.

ADJUNCT GUIDE

INSTRUCTIONS:

Study the referenced materials as directed.

Return to this guide and answer the questions.

Supersedes Guidance Package, KEP-GP-55, 1 August 1975. Stock on hand will be used.

Check your answers against the answers at the back of this Guidance Package.

Contact your instructor if you experience any difficulty.

Begin the program.

A. Turn to Student Text, Volume VII, and read paragraphs 5-1 through 5-17. Return to this page and answer the following questions.

NOTE: Refer to figure 1 for questions 1 and 2.

1. A flip-flop in the SET state will cause the relay to be _____.

2. An energized relay will move the contact arm to the _____ section of the resistive ladder.

3. Using the formula

$$E_{OUT} = \frac{\text{count in counter}}{\text{maximum possible count}} \times \text{supply voltage},$$

compute output voltage assuming a five stage counter with a count of 11001 and the applied voltage is 124 volts.

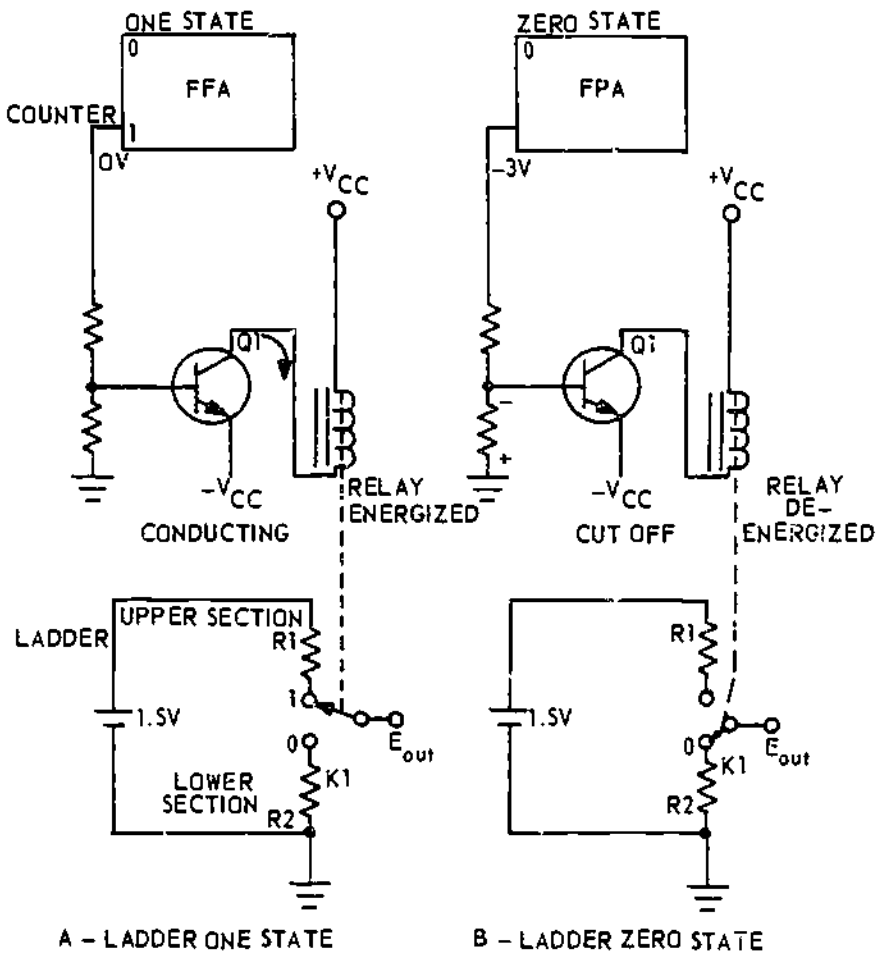


Figure 1

CONFIRM YOUR ANSWERS.

B. Turn to Student Text, Volume VII, and read paragraphs 5-18 through 5-32. Return to this page and answer the following questions.

1. The electronic D/A converter is faster and more reliable than the electromechanical converter because _____.

NOTE: Refer to figure 2 for questions 2 through 5.

2. A flip-flop in the ZERO state will cause its associated transistor to be _____.

3. Diode numbers _____ limit the maximum output voltage.

4. Resistor numbers _____ make up the resistive ladder to develop the analog output voltage.

5. Given a binary count 1001 in figure 2, transistor numbers _____ are cut off and _____ are saturated.

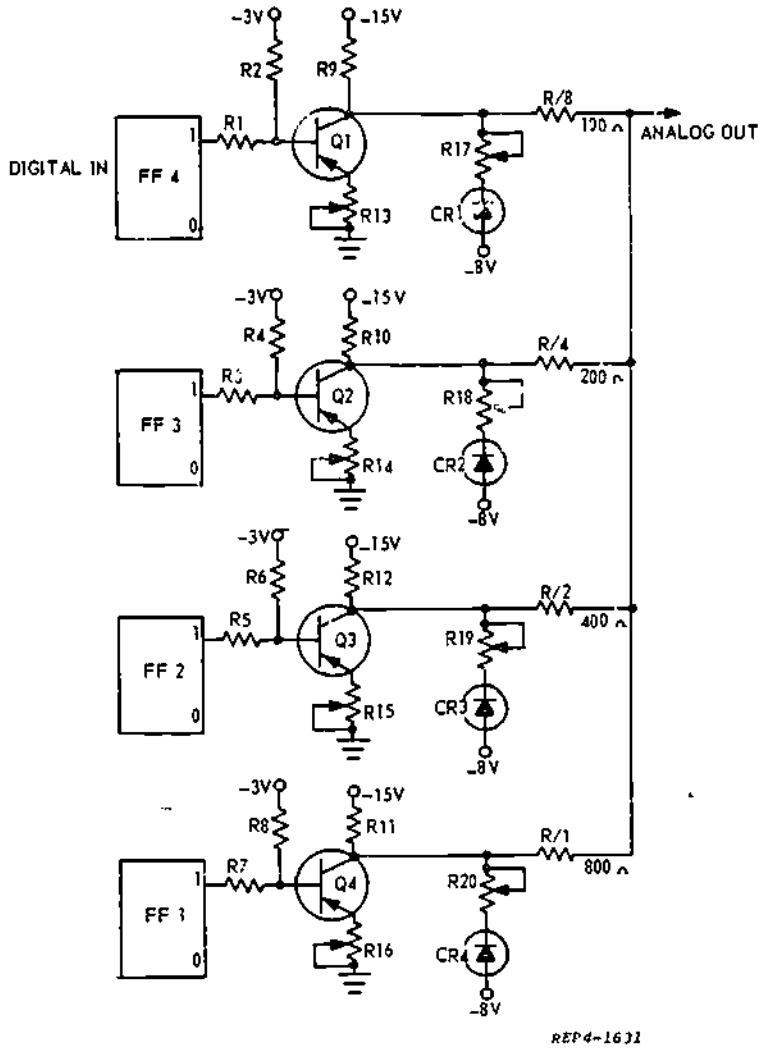


Figure 2

CONFIRM YOUR ANSWERS.

C. Turn to Student Text, Volume VII, and read paragraphs 5-33 through 5-37. Return to this page and answer the following.

1. The four basic functions performed by the A/D converter are _____, _____, _____, and _____.

NOTE: See figure 3 for questions 2 through 5.

2. The component which stores the analog voltage to be converted is _____.

3. The component which performs the compare function is _____.

4. The digitize function takes place in the _____.

5. Identify blocks A, B, C, and D according to function.

CONFIRM YOUR ANSWERS.

A._____ B._____ C._____

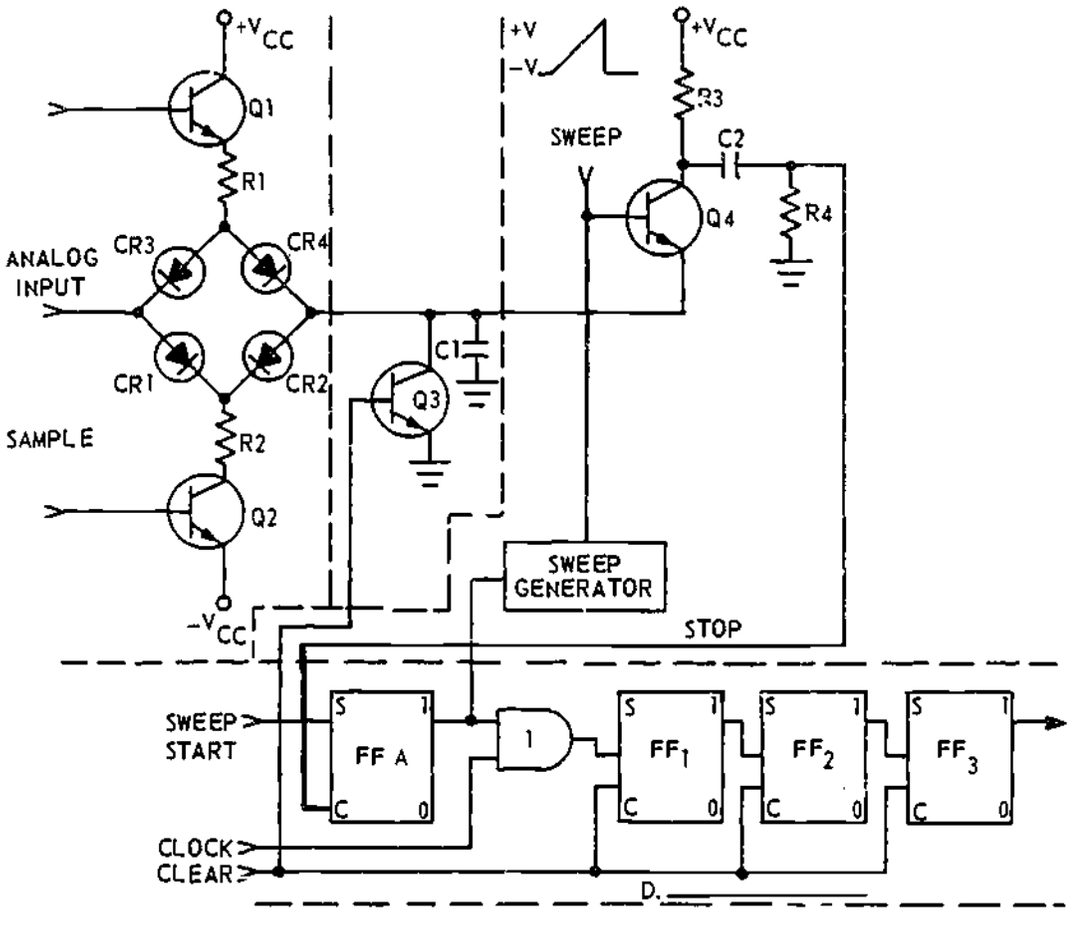


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Figure 3

MODULE SELF-CHECK

1. In D/A conversion the amplitude of the voltage step depends on the _____ and _____.

2. In the resistive ladder of a D/A converter the largest resistors are in the (LSD) (MSD).

3. A D/A converter with a four-stage counter and 75V applied voltage. The count in the counter is _____ when the output voltage is 15V.

4. Expressing a quantity in digital form is known as _____.

5. Analog/digital converter circuit performs _____ basic functions.

CONFIRM YOUR ANSWERS.

NOTES

ANSWERS TO A:

1. energized
2. upper
3. 100V

If you missed ANY questions, review the material before you continue.

ANSWERS TO B:

1. No mechanical parts
2. Saturated
3. Diodes CR1 through CR4
4. Resistors R/1, R/2, R/4, and R/8
5. Q1 and Q4 cut off
   Q2 and Q3 saturated

If you missed ANY questions, review the material before you continue.

ANSWERS TO C:

1. Sample, hold, compare and digitize
2. C1
3. Q4
4. In the serial up counter, flip-flops 1 through 3
5. a. sample
   b. hold
   c. compare
   d. digitize

If you missed ANY questions, review the material before you continue.

ANSWERS TO MODULE SELF-CHECK:

1. applied voltage, maximum count
2. LSD
3. 3
4. digitizing
5. 4

HAVE YOU ANSWERED ALL OF THE QUESTIONS CORRECTLY? IF NOT, REVIEW THE MATERIAL OR STUDY ANOTHER RESOURCE UNTIL YOU CAN ANSWER ALL QUESTIONS CORRECTLY. IF YOU HAVE, CONSULT YOUR INSTRUCTOR FOR FURTHER GUIDANCE.