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AUTHOR Kargo, Donald W.; Steffen, Dale A.
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ABSTRACT

This manual provides documentation for the design, construction, and operation of an interactive electronics training panel developed for a computer assisted performance training carrel. The panel is a plug-in module designed to simulate electronic circuitry and a PMS-6 multimeter as required for a troubleshooting fundamentals lesson in an Air Force Electronics Principles course. Five schematic panels were developed for simulation of all circuitry used in the lesson. (Author/WBC)

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PERFORMANCE TRAINING CARREL FOR ELECTRONICS PRINCIPLES COURSE

By

Donald W. Kargo
Dale A. Steffen

Denver Research Institute
University of Denver
Denver, Colorado 80210

TECHNICAL TRAINING DIVISION
Lowry Air Force Base, Colorado 80230

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MARTY R. ROCKWAY, Technical Director
Technical Training Division

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A prototype performance training carrel was developed to demonstrate a computer managed learning environment. This report describes the simulation panel developed as a part of the carrel. The panel is a plug-in module designed to provide simulation of electronic circuitry and a PSM-6 multimeter as required for a troubleshooting fundamentals lesson in an Air Force Electronics Principles course.

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SUMMARY

Problem

The objective of this effort was to evaluate a computer assisted performance training carrel which was developed in-house at the Air Force Human Resources Laboratory Technical Training Division, Lowry AFB, Colorado. The evaluation was realized by using the training carrel to deliver the troubleshooting fundamentals lesson from the Lowry AFB Technical Training Center's Electronic Principles Course. This manual provides the documentation for the design, construction and theory of operation for the student interactive electronics training panel developed for use in the performance training carrel. The software necessary to perform this task, and the subsequent course evaluation are described in AFHRL-TR-76-62(II) and AFHRL-TR-76-62(III).

Approach

The design approach was to develop a panel that would allow the user the greatest flexibility in implementing the required simulations while maintaining complete hardware compatibility with the existing carrel and its I/O bus control system.

Results

The simulation panel was developed as a plug-in module that could easily be inserted into the carrel.

The module included all of the circuitry required to interface the performance carrel I/O bus, the simulated PSM-6 multimeter, and the interchangeable schematic boards which simulated basic electronic circuitry. The multimeter and the schematic panel area comprised the front face of the module. Training schematics with up to twenty-eight test points were accommodated. Under this effort, five schematic panels were developed for simulation of all circuitry used in the troubleshooting lesson.

Conclusions

The system as developed has proved to be feasible for use in performance training and could be expanded to simulate larger and more complex circuits used in higher level courses. The plug-in concept panel allows the carrel to be readily changed over to different instructional subjects.

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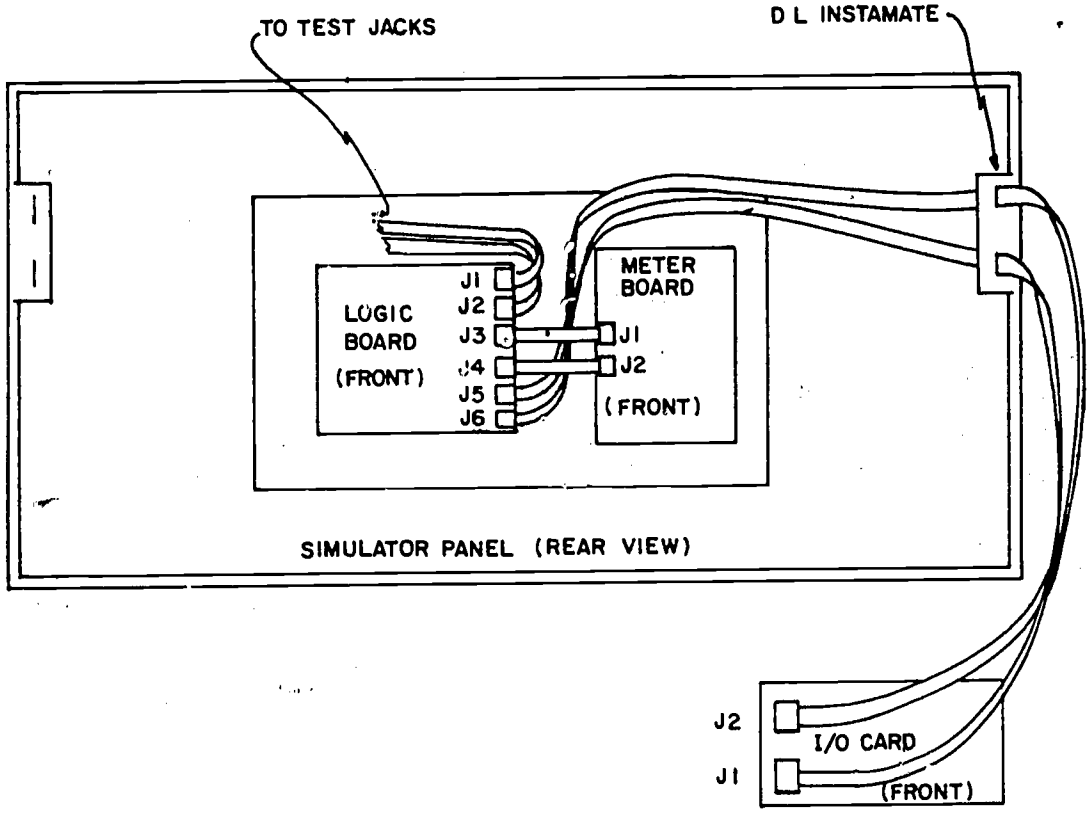
PERFORMANCE TRAINING CARREL FOR ELECTRONICS PRINCIPLES COURSE

I. GENERAL DESCRIPTION

The performance training carrel simulation panel was developed to be installed in the performance training carrel that is undergoing test and evaluation at the Technical Training Division, Air Force Human Resources Laboratory, Lowry Air Force Base, Colorado. It is plugged into and held in place by two ITT Instamate connectors. A rear view of the simulator panel and associated cable routing is shown in Figure 1. All of the electrical connections are made through the left-hand connector only. The panel is designed to operate through the I/O Interface card (DRI EC-12674) of the PLATO IV/PDP-11 I/O bus line control system. Its purpose is to simulate under computer control the multimeter and the instructional circuits that are required for the completion of a particular module of the Electronic Principles Course now being taught by the Department of Avionics Training. The software documentation is included in AFHRL-TR-76-62 (II).



LOGIC BOARD J1 — TEST JACKS
LOGIC BOARD J2 — TEST JACKS
LOGIC BOARD J3 — METER BOARD J1
LOGIC BOARD J4 — METER BOARD J2
LOGIC BOARD J5 — INSTAMATE — I/O J1
LOGIC BOARD J6 — INSTAMATE — I/O J2

Figure 1. Cable routing

The main features of the panel include the simulated PSM-6 multimeter and the interchangeable schematic boards.

The simulated multimeter is a real PSM-6 front panel and meter movement mounted in a cutout in the simulator sub-panel. The entire meter circuitry has been replaced with the new circuits required to interface the meter panel with the computers. This simulated PSM-6 multimeter is used in the same manner as a real meter would be used in troubleshooting real circuits.

A matrix of twenty-eight test jacks occupies most of the remaining sub-panel space. Any or all of the jacks can be used as test points on a "schematic board." The schematic boards are constructed of 3/16-inch plastic sheet with the schematics printed on an overlay of "Scotchcal" photosensitive material. The test points used for a particular schematic are the only ones exposed when the board is installed in its operating position on the sub-panel. A spring loaded clamp holds the boards in place on the sub-panel. When a board is in place, a set of switches are activated which encodes the schematic number for use by the computers.

A simulated power switch S1 and two display lamps DS1 and DS2, are located directly below the test jack matrix. These components are the physical counterparts of the symbols that appear on the schematic boards. All of the schematic boards have the power switch and may or may not have DS1 and/or DS2. The physical switch and lamps are used in the same manner as if they were mounted on the circuit boards in place of their respective symbols.

An additional display lamp is located directly above the meter. This lamp is labeled ON LINE and its function is to show when the computer is polling the panel. Meter readings and lamp status are valid only when the ON LINE lamp is on.

Power requirements are +5VDC and ±15 VDC. All of the power is supplied by the power supplies located in the I/O bus line control system.

II. CIRCUIT ANALYSIS

Block Diagram

Figure 2 is a block diagram of the performance training panel logic. All of the circuits are contained on three circuit boards. A printed circuit board is mounted behind the meter panel. It is referred to as the meter board. Figure 3 shows the circuitry included on this board along with the associated switches, potentiometer, indicator lamps, etc. that are mounted on the meter panel itself or on the sub-panel.

The logic board is a universal wirewrap circuit board mounted behind the test jack matrix on the sub-panel. Figure 4 contains all of the circuitry of this board.

The circuitry used in generating the current to the meter for simulated meter deflections is contained on the "users" portion of the I/O interface card (DRI EC-12674).

Logic Board

The logic board will be discussed first. It contains most of the circuitry required to determine the meter probe positions, ohms adjust potentiometer position and the output multiplexer. An output display is included as an aid in checkout and troubleshooting of the board.

The meter probes are referred to as the red probe (positive) and the black probe (negative). The meter probe position circuitry consists of counters, latches and gating required to continuously monitor the status of the probes.

U1 is a timer (NE555) wired as a free running multivibrator. The frequency of oscillation is approximately 10 kHz. The output of U1 is wired to the divide-by-sixteen binary counter (SN74161) at U2, whose MSB output drives the flip-flop (SN7472) U3. The resulting divide-by-thirty-two binary outputs are used as the inputs to the two one-of-sixteen decoders (SN74154) U4 and U5 and the two latches (9308) U6 and U7. Outputs $\overline{3}$ through $\overline{15}$ of U4 and $\overline{0}$ through $\overline{14}$ of U5 are wired to the twenty-eight test jacks on the schematic sub-panel and provide the probe signals for the latching circuits. A possible thirty-two probe positions are available of which three are reserved for special cases, one is unused and the remaining twenty-eight are the test points. These test points are numbered TP3 through TP30.

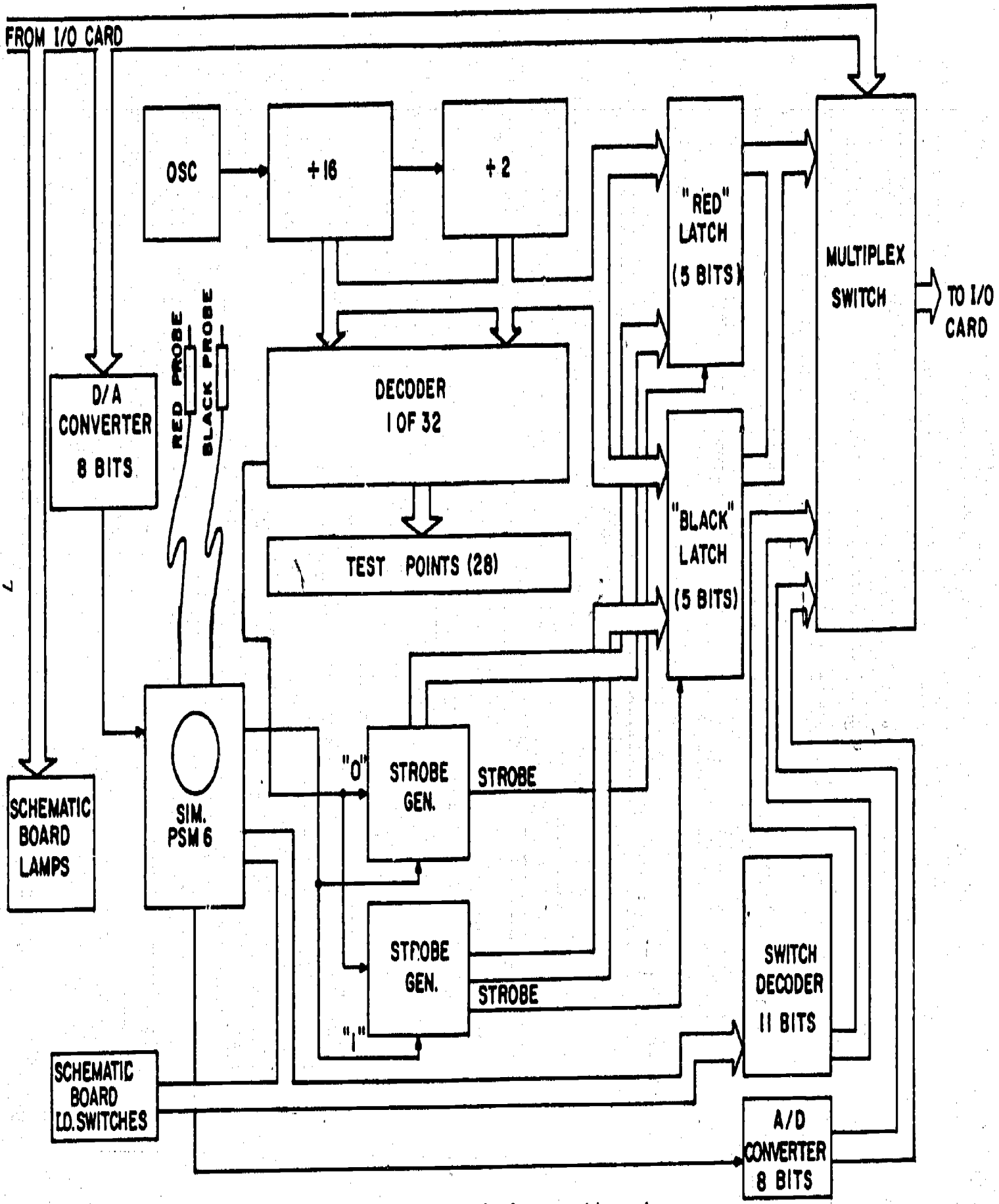


Figure 2. Block diagram of performance training panel

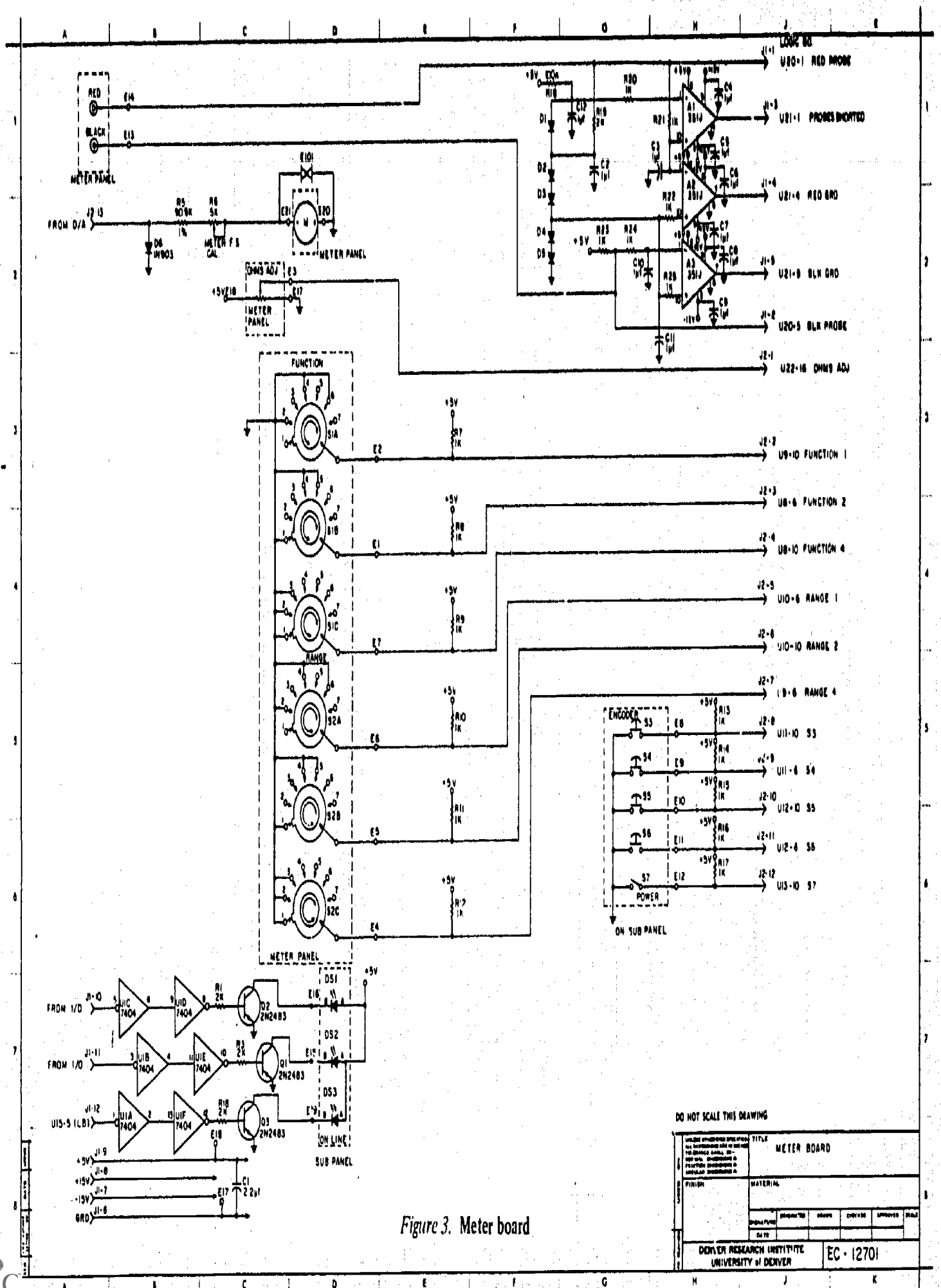


Figure 3. Meter board

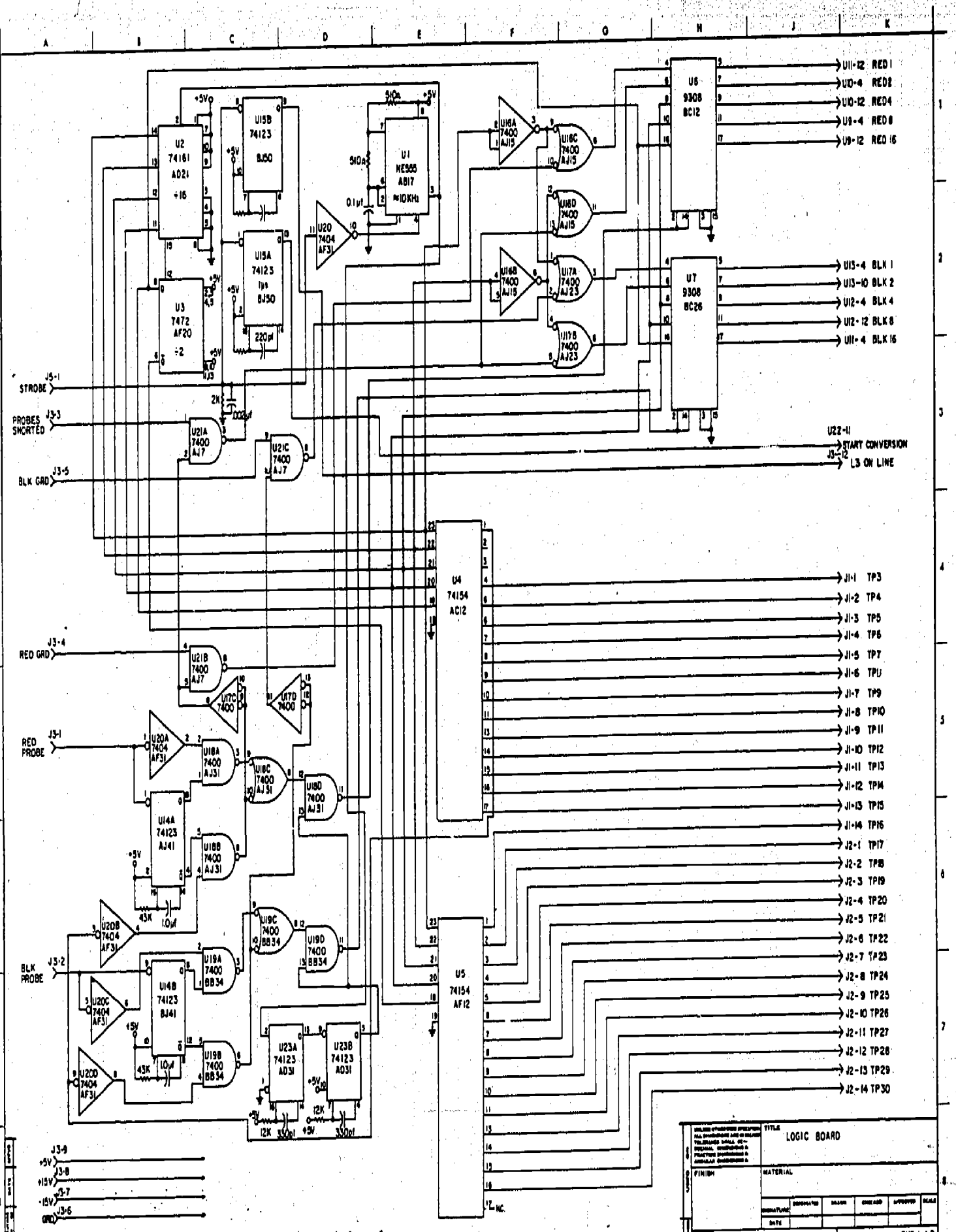


Figure 4. Logic board

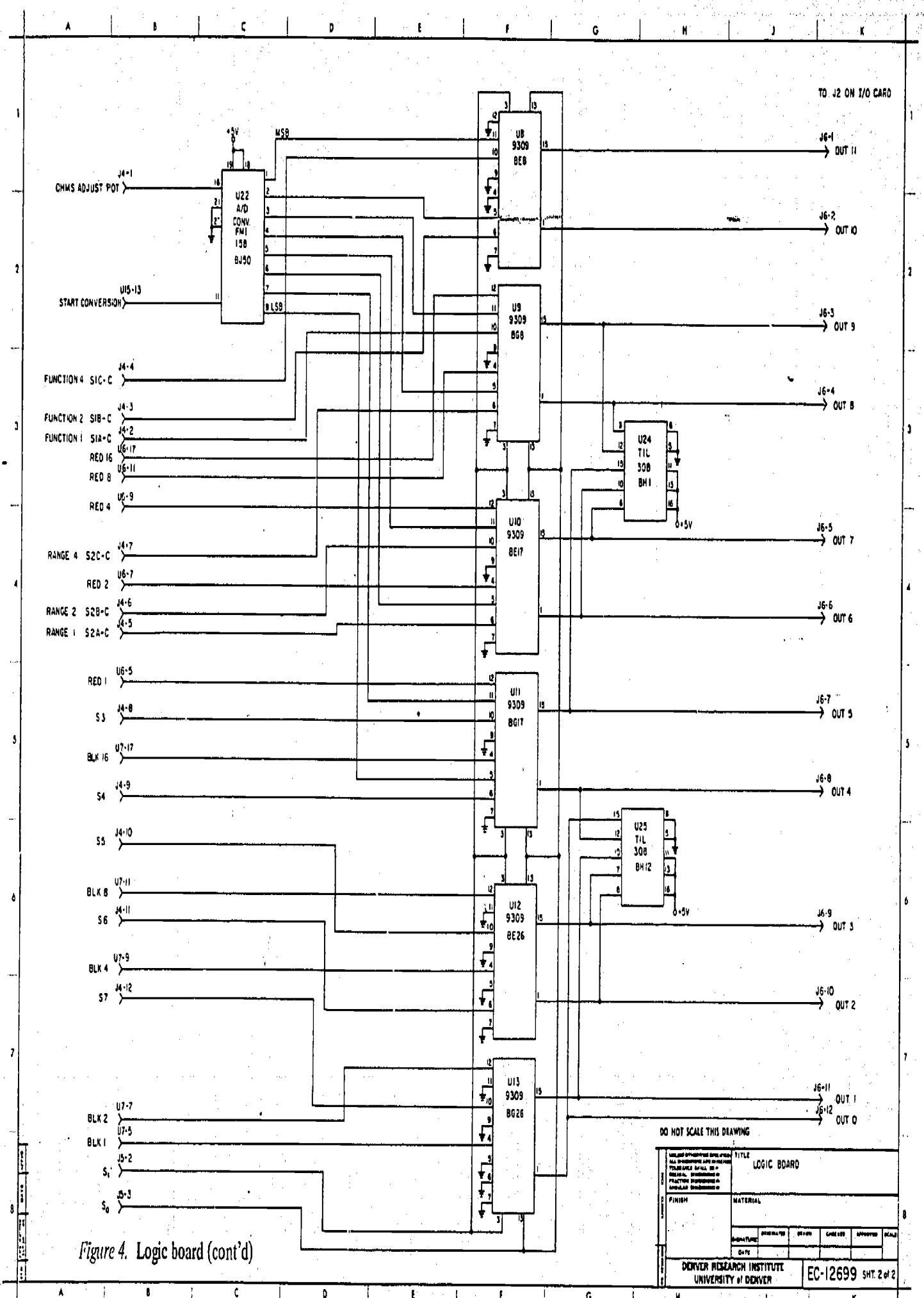


Figure 4. Logic board (cont'd)

To describe the operation of the "probe position" detector, first assume that the red probe is inserted into a TP. A negative going pulse is present at each TP each time the counter is at its respective number. This pulse is fed to U14A-1 and U20A-1. U14 is a retriggerable one-shot which is held in the ON state by the recurrence of the pulse at pin 1. U20 inverts the probe pulse which is then gated at U18A with the Q output of U14A. This signal is gated again at U18D with a delayed strobe pulse from U23B-5 which was originated by the clock input to the counter. This delay insures that the latching strobe occurs during the quiescent state of the counter. The current count held by the counter is then latched into the Dual 4 bit latch U6. Only five of the eight bits are required to hold the position number. The other three bit positions are unused.

This action is repeated at an approximate 300 Hz rate as long as the probe is contacting one of the twenty-eight test points. The latch is always holding the TP number that corresponds with the test point being probed. The output of the latch is fed to one set of inputs of the multiplexer which will be discussed later.

The previous description is identical for the black probe. The same oscillator, counters and decoders are used. The gates, one-shot, and latch are repeated as required.

As mentioned earlier, three position numbers are reserved for special cases. The special cases assigned these numbers are as follows:

0 = Probe open circuited.

1 = Probe grounded to chassis.

2 = Probes shorted together. (This is defined as shorted together only and not touching chassis ground or any TP.)

The "probe open circuited" condition is similar to the previously described action except that now the pulse at U14A-1 is missing and the one-shot reverts to its reset condition. The resultant high level at U18B-5 gates count "0" through as the strobe to the latch and the latch will contain "0." (Count "0" is *always* the strobe to the latches whenever the probes are *not* in contact with a TP.)

The "probe grounded" and "probes shorted together" cases utilize the voltage comparators A1, A2 and A3 located on the meter board (Figure 3). The diode string consisting of D1 through D5 establishes the reference voltages for the comparators and probes.

Originally when the red probe is open or contacting a test point, its DC potential is held at approximately +3V through R19. The inverting input of A2 is connected to the red probe through R21. The noninverting input of A2 is held at approximately +1.5V through R22. The output of A2 is then at ground and the gate at U21B-4 (Figure 4) is held off. The inverting input of A2 will rise to the average DC potential of the probe and the output will remain at ground.

If the red probe is grounded to the chassis, its DC potential goes to 0 volts and the A2 voltage comparator output switches to +5V. This enables the gate U21B, allowing the "0" count to be latched as a "one" through the negative output or (NOR) gate U16C.

The black probe operates in the same manner. The inverting input of voltage comparator A3 is held at +5V through R23 and the resultant switching of the comparator output enables the gate U21C, allowing the black "0" to be latched as a "one."

The last special case is when the probes are shorted together as would be done for zeroing the meter prior to a resistance measurement. In this case the voltage comparator A1 is used. The inverting input of A1 is held at approximately +3.75V and the noninverting input at the same +3V level as the red probe. In any case other than the probes being shorted together the output of A1 is at ground and the gate U21A is held off. When the probes are shorted together, the DC level of the noninverting input rises to approximately +4.25V and the output of A1 switches to its high level. This enables the gate U21A and allows the red "0" to be routed through the NOR gates U16D and U17B where it is latched as a "two" in both the red and black latches.

The strobe pulse whose input is at J5-1 (Figure 4) is generated in the I/O bus line control system each time the PDP-11 computer polls the simulator panel. The polling rate is not synchronous with the oscillator

frequency; therefore the strobe pulse is used to interrupt the oscillator during the interrogation. This insures that the probe position number cannot change during the transfer of data.

The strobe pulse is also used to trigger the two one-shots of U15. U15A triggers on the trailing edge of the strobe and generates the start conversion pulse for the A/D converter U22. The converter will be discussed later. U15B is a retriggerable one-shot whose Q output switches high and stays high as long as the computer is polling the simulator panel at approximately a 30 Hz or faster rate. This output drives L3, the ON LINE indicator, on the sub-panel to tell the student that the computer is monitoring the panel and providing a valid meter deflection.

The multiplexer is comprised of six Fairchild 9309 Dual Four-input Multiplexer integrated circuits. This configuration allows for four words of data transfer to the computer. Each word has a maximum of twelve bits, although in the present system only three words of from eight to eleven bits are used. The word being read is selected by the computer through the two select inputs S0 and S1. Table 1 shows the contents

Table 1. Data Words

DATA WORD FROM PDP11		DATA WORDS TO PDP 11					
		S_0	S_1	S_0	S_1	S_0	S_1
	DATA BIT NO.	L	L	H	L	L	H
		PROBE LOC.		OHMS ADJ. POTENTIOMETER		SWITCH POS.	
METER MSB	15			MSB		FUNCTION SW.4	
	14					" SW.2	
	13	RED PROBE 16				" SW.1	
	12	RED PROBE 8				RANGE SW.4	
	11	RED PROBE 4				" SW.2	
	10	RED PROBE 2				" SW.1	
	9	RED PROBE 1				SCHEM. BD. #8	
LSB	8	BLK PROBE 16		LSB		" " #4	
S_0	7	BLK PROBE 8				" " #2	
S_1	6	BLK PROBE 4				" " #1	
DS1	5	BLK PROBE 2				SIMULATED "PWR" SWITCH	
DS2	4	BLK PROBE 1					
ID3	3	ID3		ID3		ID3	
ID2	2	ID2		ID2		ID2	
ID1	1	ID1		ID1		ID1	
ID0	0	ID0		ID0		ID0	

and bit position of the data for each word. The left-hand column of Table 1 is the data word transmitted to the panel by the computer. The four LSB positions are reserved for the I/O card I.D. number. Data bits 4 and 5 control the status of DS2 and DS1, respectively. Data bits 6 and 7 are the word select bits used by the computer when inputting data. Bits 8 through 15 are the eight bits transmitted to the FMI-8BIN-V D/A converter to control the simulated PSM-6 meter deflection.

Two TIL-308 seven segment displays are wired to the multiplexer output. These displays indicate the probe positions at all times when S0 and S1 are low. They are included for maintenance purposes only. The seven-segment code is semi hexa-decimal and the decimal point is wired to indicate a binary 16. The panel will operate properly without these indicators installed if desired.

Simulated PSM-6

The simulated PSM-6 consists of the front panel of a real PSM-6 multimeter with all of the electronic circuitry replaced.

The function and range switches are three pole, seven position switches which only encode the switch positions. The output of the switches are wired to the multiplexer for transfer to the computer.

The ohm zero potentiometer provides a DC voltage between 0 and 5 volts to the FMI158 eight bit A/D converter located on the logic board. The output of this converter is routed to one of the inputs of the multiplexer. The start conversion pulse, as previously discussed, occurs at the trailing edge of the strobe pulse. This allows the setting of the potentiometer to be read into the computer first and then start the cycle for the next conversion. The time required for the conversion cycle is 50 μsec. Reading the previous result first and then initiating a new conversion cycle provides the necessary time for conversion.

The meter movement is the original PSM-6 50μ ampmeter. The meter protection diode assembly (E101) was retained from the original component board. R6 is used to adjust the meter deflection to full scale during calibration.

The deflection voltage is provided by the D/A converter located on the I/O interface card in the card nest assembly (Figure 5). The converter is wired for bipolar operation so that a reversed meter deflection can be simulated. The inverters and gates at U1-U4 are used to modify the digital input from the computer before it enters the converter. This insures that the meter cannot be overdriven in the reverse direction.

Table 2 illustrates how this conversion is used.

Table 2. Binary Conversion

Binary from Computer	Binary into D/A Converter	Meter Reading (0-100 Scale)
1XXXXX00*	01111100	−3.3
00000000	10000000	0
00111100	10111100	+50
01111000	11111000	+100
01111111	11111111	+105.8

*X = Don't care

Any time the binary number from the computer contains a "1" in the most significant bit (MSB) position the D/A converter output will be −V. The "1" in the MSB position is inverted at U1A and appears as a "1" at five of the other seven binary inputs to the converter and limits the negative excursion of the meter to −3.3 divisions. This is enough to show a reversed meter probe condition but not enough to damage the meter movement. The largest binary number into the converter produces a deflection of about 106 divisions which will show an out-of-range setting of the range switch but again, not enough to damage the meter. The meter deflection is calibrated by first adjusting R1 (Figure 5) for a zero meter reading when the computer is sending a binary zero to the I/O interface card and then adjusting R6 on the meter board (Figure 3) for full-scale deflection when the binary number 01111000 is being transmitted.

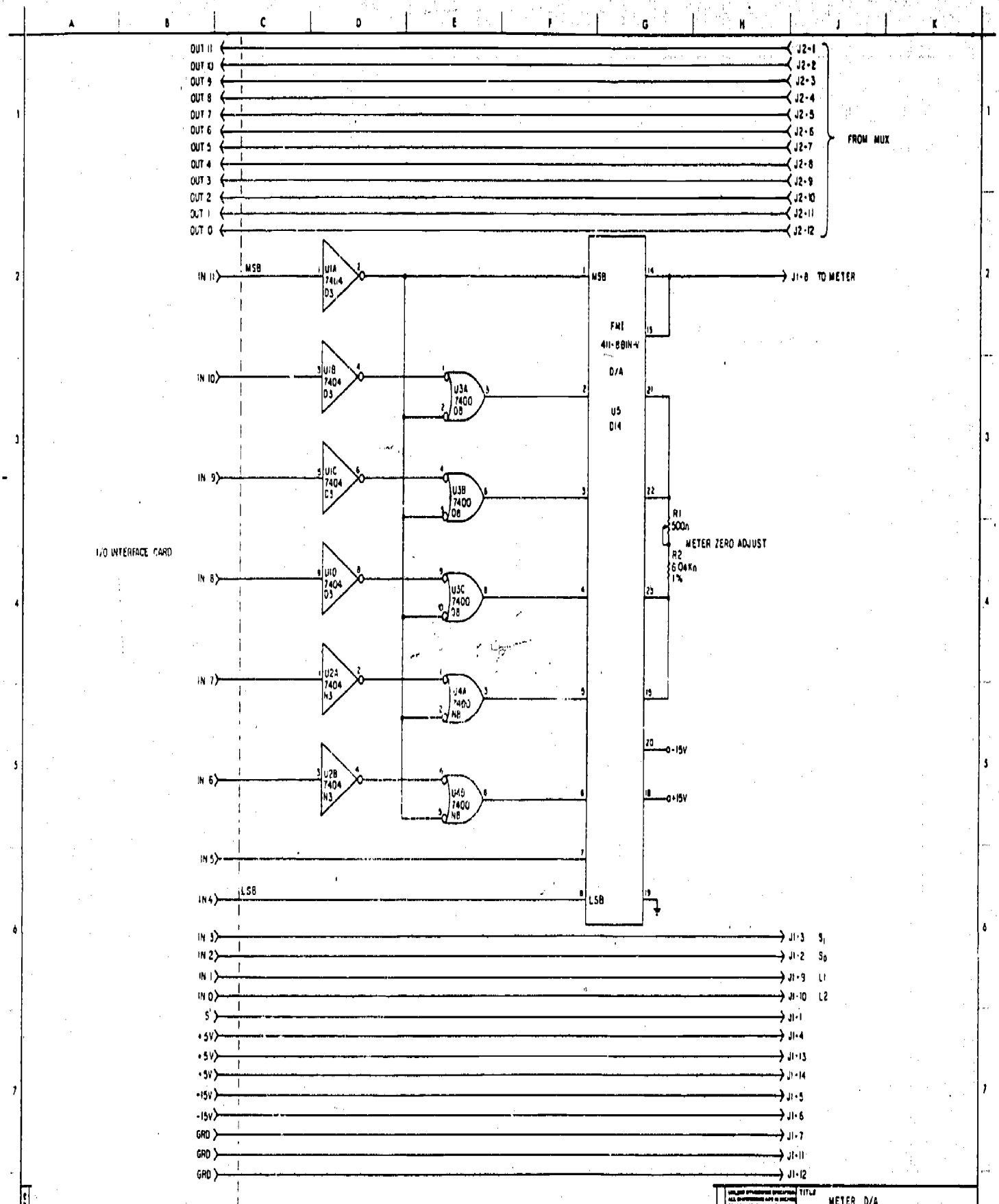


Figure 5. Meter D/A

Meter Board

The remaining circuits shown on the meter board (Figure 3) that have not been previously discussed are the lamp drivers and switches S3 through S7. Q1 and Q2 drive the indicating *LEDs* DS1 and DS2 upon command by the computer through the I/O interface card. Q3 drives the ON LINE indicator by the action of the retriggerable one-shot multivibrator that was discussed in the logic board section.

S3 through S6 are pushbutton switches mounted behind the sub-panel so that the pushbuttons protrude through the panel. These switches are actuated by the schematic board installed in the operating position on the panel. The milled depressions on the back side of each schematic board encode it with its unique identification number. Up to fifteen different schematic boards can be encoded with the four bit code provided. The binary number fifteen is reserved to indicate to the computer that no board is installed on the panel.

S7 is the simulated POWER switch. This switch is the physical counterpart of the switch labeled S1 on each of the schematic boards. Its only operation is to indicate to the computer if the student has turned the power ON or OFF before taking voltage or ohmmeter readings.

III. MAINTENANCE

Only two adjustments are required in the alignment of the system. The procedure for these adjustments are as follows:

1. Use the PDP-11 ODT program to transmit the data word 000001 to address 767742.
2. Adjust R1 on the "users portion" of the I/O interface card for a zero reading on the simulated PSM-6 meter.
3. Transmit the data word 074001 to address 767742 and adjust R6 on the meter board for full scale deflection of the meter.

Linear and digital integrated circuits are used almost exclusively throughout the system and replacement is required if a malfunction occurs. Most of the ICs are mounted in sockets and replacement is easily accomplished. A number of discrete components on the meter board are soldered to the eyeleted board. Good soldering techniques, and the use of appropriate soldering and unsoldering aids, will insure trouble-free replacement.

The +5V power supply is located in the I/O bus line card nest and is adjustable. The adjustment potentiometer is located on the supply printed circuit board. This adjustment should *not* be attempted without a calibrated digital voltmeter. The +15V supply is a sealed unit and must be replaced if found defective.

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